

3-PHASE AC Motor Controller IC

Features

- Floating channel up to +1200V
- “soft” over-current shutdown turns off output
- Integrated desaturation circuit
- Two stage turn on output for di/dt control
- Integrated brake IGBT driver with protection
- Voltage feedback sensing function
- Separate pull-up/pull-down output drive pins
- Matched delay outputs
- Under voltage lockout with hysteresis band
- Programmable deadtime
- Hard shutdown function

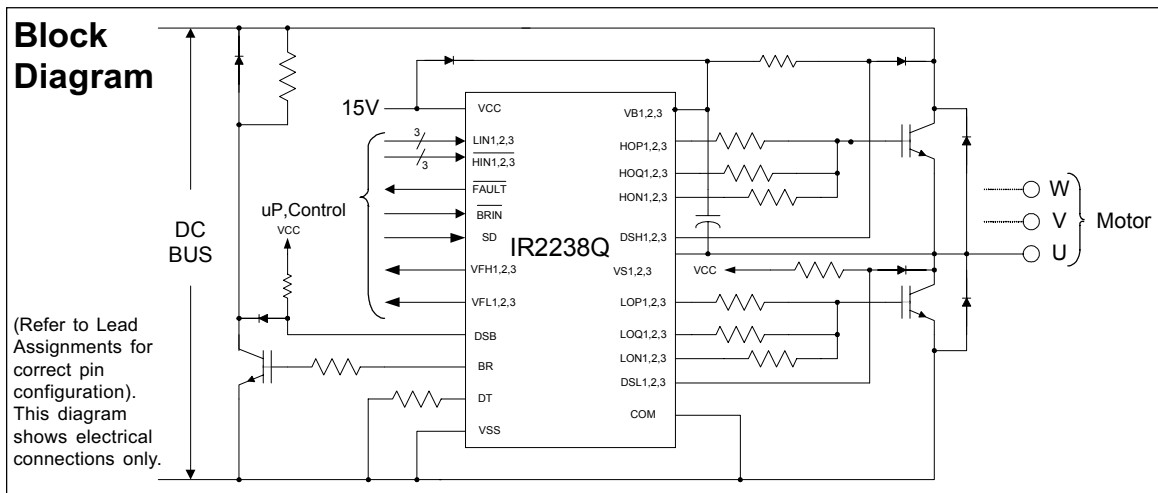
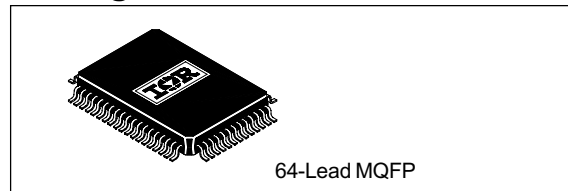
Description

The IR2238Q is a high voltage, 3-phase IGBT driver best suited for AC motor drive applications. Integrated desaturation logic provides all mode of overcurrent protection, including ground fault protection. Soft shutdown is predominantly initiated in the event of overcurrent followed by turn-off of all six outputs. A shutdown input is provided for a customized shutdown function. The DT pin allows external resistor to program the deadtime. Output drivers have separate turn on/off pins with two stage turn-on output to achieve the desired di/dt switching level of IGBT. Voltage feedback provides accurate volts *seconds measurement.

Product Summary

V_{OFFSET}	1200V max.
$I_{O+/-}$ (min.)	220mA/460mA
V_{OUT}	12.5V - 20V
Brake ($I_{O+/-}$ min)	40mA/80mA
Deadtime Asymmetry Skew (max.)	145nsec
Deadtime (typ. with $R_{DT}=39k\Omega$)	1 μ sec
DESAT Blanking time (typ.)	3.0 μ sec
DSH, DSL input voltage threshold (typ.)	8.0V
Soft shutdown duration time (typ.)	6.0 μ sec
Voltage feedback matching delay time (max.)	125nsec

Package



Absolute Maximum Ratings (tentative)

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM, all currents are defined positive into any lead. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min.	Max.	Units
V _S	High side offset voltage	V _{B1,2,3} -25	V _{B1,2,3} +0.3	
V _B	High side floating supply voltage	-0.3	1225	
V _{HO}	High side floating output voltage (HOP, HON, HOQ)	V _{S1,2,3} - 0.3	V _{B1,2,3} + 0.3	
V _{CC}	Low side and logic fixed supply voltage	-0.3	25	
V _{SS}	Logic ground	V _{CC} - 25	V _{CC} + 0.3	
V _{LO}	Low side output voltage (LOP, LON, LOQ)	-0.3	V _{CC} + 0.3	
V _{IN}	Logic input voltage (HIN/N,LIN, BRIN/N, SD)	V _{SS} - 0.3	V _{CC} + 0.3 or V _{SS} + 15 which ever is lower	
V _{FLT}	FAULT output voltage	V _{SS} - 0.3	V _{CC} + 0.3	
V _F	Feedback output voltage	V _{SS} - 0.3	V _{CC} + 0.3	
V _{DSH}	High side desat/feedback input voltage	V _{S1,2,3} - 0.3	V _{B1,2,3} + 0.3	
V _{DSL}	Low side desat/feedback input voltage	- 0.3	V _{CC} + 0.3	
V _{BR}	Brake output voltage	-0.3	V _{CC} + 0.3	
dV _S /dt	Allowable offset voltage slew rate	—	50	V/ns
P _D	Package power dissipation @ T _A ≤ +25°C	—	2.0	W
R _{thJA}	Thermal resistance, junction to ambient	—	60	°C/W
T _J	Junction temperature	—	125	
T _S	Storage temperature	-55	150	
T _L	Lead temperature (soldering, 10 seconds)	—	300	

Recommended Operating Conditions

For proper operation the device should be used within the recommended conditions. All voltage parameters are absolute voltages referenced to COM. The V_S offset rating is tested with all supplies biased at 15V differential.

Symbol	Definition	Min.	Max.	Units
V _{B1,2,3}	High side floating supply voltage	V _{S1,2,3} + 13	V _{S1,2,3} + 20	
V _{S1,2,3}	High side floating supply offset voltage	Note 1	1200	
V _{HO1,2,3}	High side (HOP/HOQ/HON) output voltage	V _{S1,2,3}	V _{B1,2,3}	
V _{LO1,2,3}	Low side (LOP/LOQ/LON) output voltage	V _{COM}	V _{CC}	
V _{IN}	Logic input voltage (HIN/N,LIN, BRIN/N SD)	V _{SS}	V _{SS} + 5	
V _{CC}	Low side supply voltage	12.5	20	V
V _{SS}	Logic ground	-5	+5	
V _{FLT}	FAULT output voltage	V _{SS}	V _{CC}	
V _F	Feedback output voltage	V _{SS}	V _{CC}	
V _{DSH}	High side desat/feedback input voltage	V _{S1,2,3} - 0.3	V _{B1,2,3}	
V _{DSL}	Low side desat/feedback input voltage	- 0.3	V _{CC}	
V _{BR}	BRAKE output voltage	V _{COM}	V _{CC}	
T _A	Ambient temperature	-20	115	°C

Note 1: Logic operational for V_S of COM-5V to COM+1200V. Logic state held for V_S of COM-5V to COM-V_{BS}.

Static Electrical Characteristics

V_{BIAS} (V_{CC} , $V_{BS1,2,3}$) = 15V and T_A = 25°C unless otherwise specified. The V_{IN} , V_{TH} and I_{IN} parameters are referenced to V_{SS} and are applicable to all six channels (HOP/HOQ/HON1,2,3 and LOP/LOQ/LON1,2,3). The V_O and I_O parameters are referenced to COM and $V_{S1,2,3}$ and are applicable to the respective output leads: HO1,2,3 and LO1,2,3. V_{DESAT} and I_{DESAT} parameters are referenced to COM and $V_{S1,2,3}$

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{CCUV+}	V_{CC1} supply undervoltage positive going threshold	10.3	11.2	12.5		
V_{CCUV-}	V_{CC1} supply undervoltage negative going threshold	9.5	10.2	11.3		
V_{CCUVH}	V_{CC1} supply undervoltage lockout hysteresis	—	1.0	—		
V_{BSUV+}	V_{BS} supply undervoltage positive going threshold	10.3	11.2	12.5		
V_{BSUV-}	V_{BS} supply undervoltage negative going threshold	9.5	10.2	11.3		
V_{BSUVH}	V_{BS} supply undervoltage lockout hysteresis	—	1.0	—		
I_{LK}	Offset supply leakage current	—	—	50		$V_{B1,2,3} = V_{S1,2,3} = 1200V$
I_{QBS}	Quiescent V_{BS} supply current	—	150	250		$V_{LIN}=0V, V_{HIN}=5V$
I_{QCC}	Quiescent V_{CC} supply current	—	3	6	mA	$V_{LIN}=0V, V_{HIN}=5V$ $DT = 1\mu sec$
V_{IH}	Logic "0" input voltage (HIN/N, BRIN/N) (OUT=LO)	2.0	—	—		
V_{IL}	Logic "1" input voltage (HIN/N, BRIN/N) (OUT=HI)	—	—	0.8		
V_{t+}	Logic input positive going threshold (HIN/N, LIN, BRIN/N, SD)	1.2	1.6	2.0		
V_{t-}	Logic input negative going threshold (HIN/N, LIN, BRIN/N, SD)	0.8	1.2	1.6		
ΔV_T	Logic input hysteresis (HIN, LIN, BRIN, SD)	—	0.4	—		
V_{OH}	High level output voltage, $V_{BIAS} - V_O$ (normal switching) HOP, HOQ, LOP, LOQ	—	—	100		
V_{OL}	Low level output voltage, V_O (normal switching) HON, LON	—	—	100		
I_{IN+}	Logic "1" input bias current (HIN/N, BRIN/N) Logic "1" input bias current (LIN, SD)	—	5 70	—		$V_{IN} = 0V$ $V_{IN} = 5V$
I_{IN-}	Logic "0" input bias current (HIN/N, BRIN/N) Logic "0" input bias current (LIN, SD)	—	70 5	—		$V_{IN} = 5V$ $V_{IN} = 0V$
I_{DS+}	High DSH, DSL, DSB input bias current	—	15	—		$V_{DESAT} = 15V$
I_{DS-}	Low DSH, DSL, DSB input bias current	—	0.1	—		$V_{DESAT} = 0V$
I_{O1+}	Output high first stage short circuit pulsed current	220	350	—		$V_O = 0V, V_{IN} = 0V$ $PW \leq 200 ns$
I_{O2+}	Output high second stage short circuit pulsed current	120	200	—		$V_O = 0V, V_{IN} = 0V$ $PW \leq 10 \mu s$
I_{O-}	Output low short circuit pulsed current	460	540	—		$V_O = 15V, V_{IN} = 5V$ $PW \leq 10 \mu s$

Static Electrical Characteristics cont.

V_{BIAS} (V_{CC} , $V_{BS1,2,3}$) = 15V and T_A = 25°C unless otherwise specified. The V_{IN} , V_{TH} and I_{IN} parameters are referenced to V_{SS} and are applicable to all six channels (HOP/HOQ/HON1,2,3 and LOP/LOQ/LON1,2,3). The V_O and I_O parameters are referenced to COM and $V_{S1,2,3}$ and are applicable to the respective output leads: HO1,2,3 and LO1,2,3. V_{DESAT} and I_{DESAT} parameters are referenced to COM and $V_{S1,2,3}$

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
I_{OBR+}	BR output high short circuit pulsed current	40	70	—		$V_{BR}=0V$, $V_{BRIN}=0V$ $PW \leq 10 \mu s$
I_{OBR-}	BR output low short circuit pulsed current	80	125	—		$V_{BR}=15V$, $V_{BRIN}=5V$ $PW \leq 10 \mu s$
V_{OHB}	BR high level output voltage, $V_{CC}-V_{BR}$	—	—	300		
V_{OLB}	BR low level output voltage, V_{BR}	—	—	150		
V_{OLVF}	VFH or VFL low level output voltage	—	—	0.8	V	$I_{VF} = 10mA$
$R_{ON,VF}$	VFH or VFL output on resistance	—	60	—		
$R_{ON,SS}$	Soft shutdown on resistance	—	500	—		
$R_{ON,FLT}$	FAULT low on resistance	—	60	—		
V_{DESAT+}	High DSH1,2,3 and DSL1,2,3 and DSB input threshold voltage	—	8.0	—		
V_{DESAT-}	Low DSH1,2,3 and DSL1,2,3 or DSB input threshold voltage	—	7.0	—		
V_{DSTH}	DS input voltage hysteresis	—	1.0	—		

AC Electrical Characteristics

V_{BIAS} (V_{CC} , V_{BS}) = 15V, $V_{S1,2,3} = V_{SS}$, $T_A = 25^\circ C$ and $C_L = 1000$ pF unless otherwise specified.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
Propag						
T_{on1}	Turn-on first stage duration time	—	200	—		$V_{IN} = 0$ & 5V $R_L(HOQ/LOQ) = 10\Omega$
t_{on}	Turn-on propagation delay	250	550	750		
t_{off}	Turn-off propagation delay	250	550	750		
t_r	Turn-on rise time	—	80	—		
t_f	Turn-off fall time	—	25	—		
t_{DESAT1}	DSH to HO soft shutdown propagation delay at HO turn-on	—	3000	—		
t_{DESAT2}	DSH to HO soft shutdown propagation delay after blanking	1000	—	—		
t_{DESAT3}	DSL to LO soft shutdown propagation delay at LO turn-on	—	3000	—		$V_{LIN} = 5V$, $V_{DESAT} = 15V$, Fig.7

AC Electrical Characteristics cont.

V_{BIAS} (V_{CC}, V_{BS}) = 15V, V_{S1,2,3} = V_{SS}, T_A = 25°C and C_L = 1000 pF unless otherwise specified.

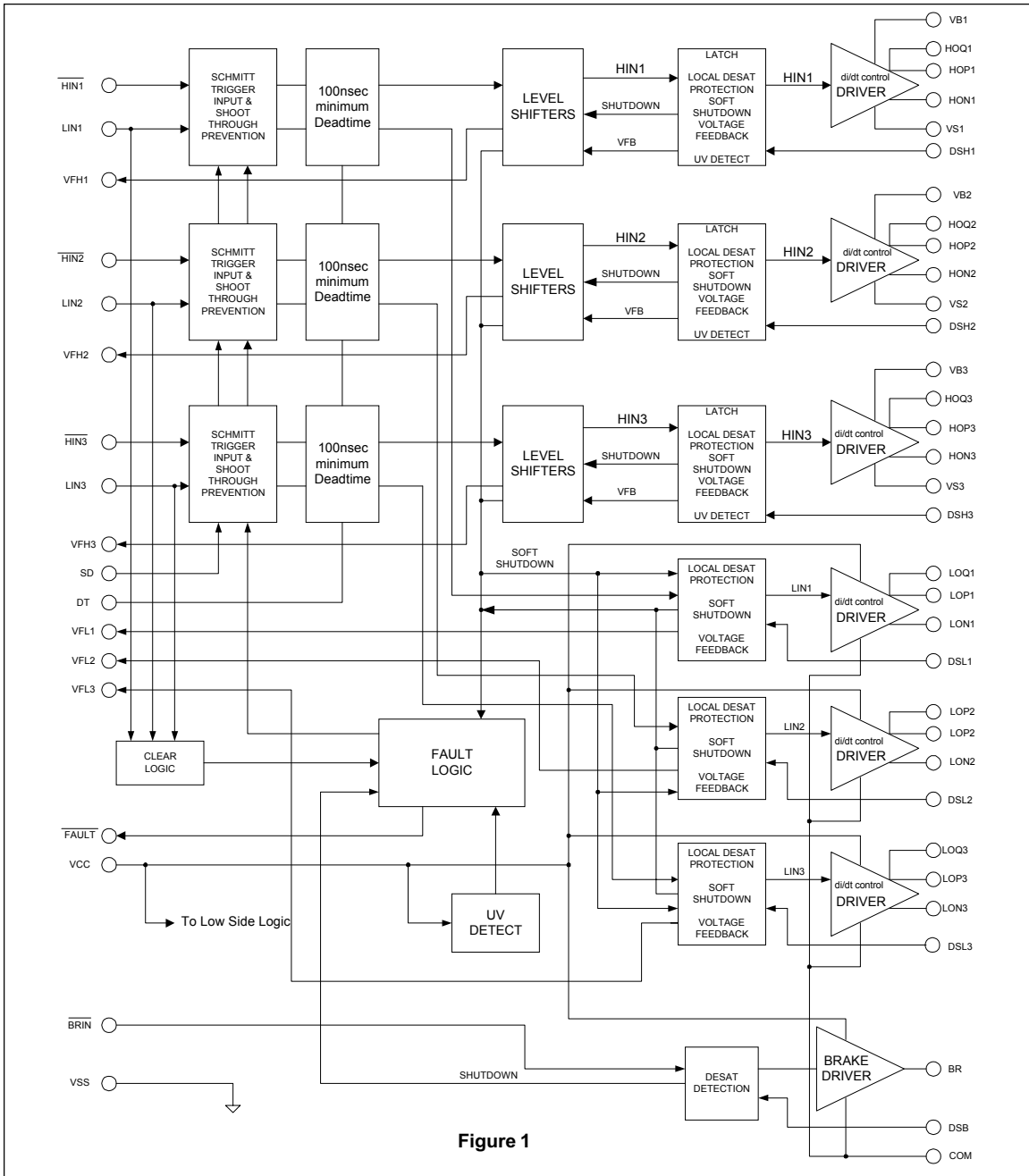
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
Propagation Delay Characteristics						
t _{DESAT4}	DSL to LO soft shutdown propagation delay after blanking	1000	—	—		V _{LIN} = 5V, V _{DESAT} = 15V, Fig. 7
t _{DESAT5}	DSB to HO hard shutdown propagation delay	—	1300	—		V _{HIN} = 0V, V _{DESAT} = 15V, Fig. 7
t _{DESAT6}	DSB to LO hard shutdown propagation delay	—	1300	—		V _{LIN} = 5V, V _{DESAT} = 15V, Fig. 7
t _{DESAT7}	DSB to BR hard shutdown propagation delay	900	—	—		V _{VBRIN} = 0V, V _{DSB} = 15V, Fig. 7
t _{VFHL1,2,3}	VFH high to low propagation delay	—	550	—		V _{DESAT} = 15V to 0V Figure 8
t _{VFHHL1,2,3}	VFH low to high propagation delay	—	550	—		V _{DESAT} = 0V to 15V Figure 8
t _{VFLH1,2,3}	VFL low to high propagation delay	—	550	—		V _{DESAT} = 0V to 15V Figure 8
t _{VFL1,2,3}	VFL high to low propagation delay	—	550	—		V _{DESAT} = 15V to 0V Figure 8
t _{PWVF}	Minimum pulse width of VFH and VFL	—	400	—		V _{DESAT} = 15V to 0V or 0V to 15V fig. 8
t _{DS}	Soft shutdown minimum pulse width of DSx	1000	—	—		
t _{SS}	Soft shutdown duration period	—	6000	—		
t _{FLT,DESAT1}	DSH to FAULT propagation delay at HO turn-on	—	3300	—		
t _{FLT,DESAT2}	DSH to FAULT propagation delay after blanking	—	1300	—		
t _{FLT,DESAT3}	DSL to FAULT propagation delay at LO turn-on	—	3300	—		
t _{FLT,DESAT4}	DSL to FAULT propagation delay after blanking	—	1000	—		
t _{FLTDSB}	DSB to FAULT propagation delay	—	1000	—		BRIN = 0V, V _{DESAT} = 15V, Fig. 7
t _{FLTCLR}	LIN1 = LIN2 = LIN3 = 0 to FAULT	9.0	—	—		V _{DESAT} = 15V, Fig. 7
t _{fault}	Minimum FAULT duration period	9.0	15.0	21.0		V _{DESAT} = 15V, Fig. 11 FLTCLR pending
t _{BL}	DS blanking time at turn-on	—	3000	—		V _{IN} = on, V _{DESAT} = 15V, Fig. 7
t _{SD}	SD to output shutdown propagation delay	—	600	900		V _{IN} = on, V _{DESAT} = 0V, Fig. 10

AC Electrical Characteristics cont.

$V_{BIAS} (V_{CC}, V_{BS}) = 15V$, $V_{S1,2,3} = V_{SS}$, $T_A = 25^\circ C$ and $C_L = 1000 \text{ pF}$ unless otherwise specified.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
Propa						
t_{EN}	SD negation to output enable propagation delay	—	600	900		$V_{IN} = 0V$ $V_{DESAT} = 0V$, Fig.10
t_{onBR}	BR output turn-on propagation	—	110	200		
t_{offBR}	BR output turn-off propagation	—	80	150		
t_{rBR}	BR output turn-on rise time	—	235	400		
t_{fBR}	BR output turn-off fall time	—	130	200		
Dea						
DT	Deadtime	900	1050	1200		Figure 8 external resistor=39k Ω
		76	100	124		Figure 8 external resistor=0k Ω
		4500	5000	5500		Figure 8 external resistor=220k Ω
MDT	Deadtime asymmetry skew, any of DTLoff1,2,3-DTHoff1,2,3	—	—	145		DT=1000nsec. Fig.8
PM	PWM propagation delay matching max {ton/toff} - min {ton/toff}, (ton/toff are applicable to all six channels)	—	—	125		DT=1000nsec. Fig.5
VM	Voltage feedback delay matching, any of $t_{VFHL1,2,3}$, $t_{VFHH1,2,3}$, $t_{VFLL1,2,3}$, $t_{VFLH1,2,3}$ - any of $t_{VFHL1,2,3}$, $t_{VFHH1,2,3}$, $t_{VFLL1,2,3}$, $t_{VFLH1,2,3}$	—	—	125		Input pulse width >400 nsec Figure 9

Functional Block Diagram



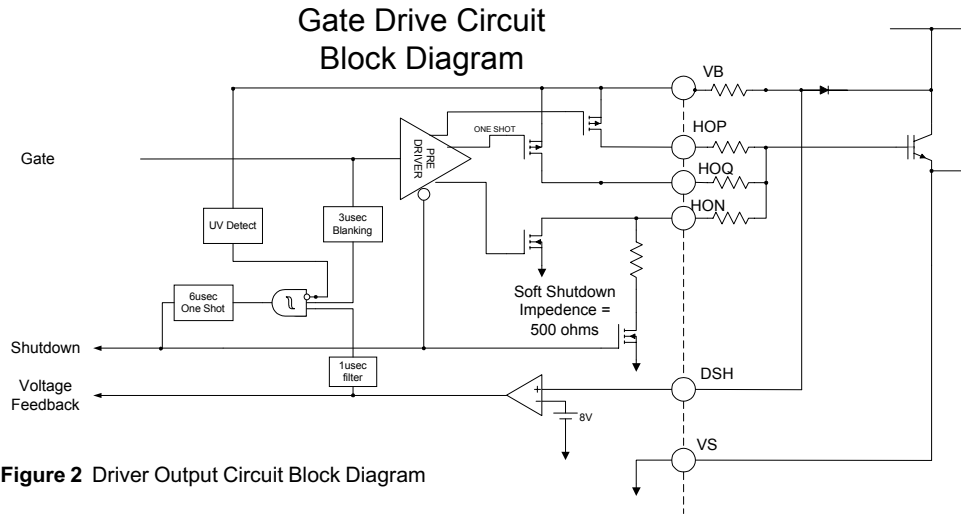


Figure 2 Driver Output Circuit Block Diagram

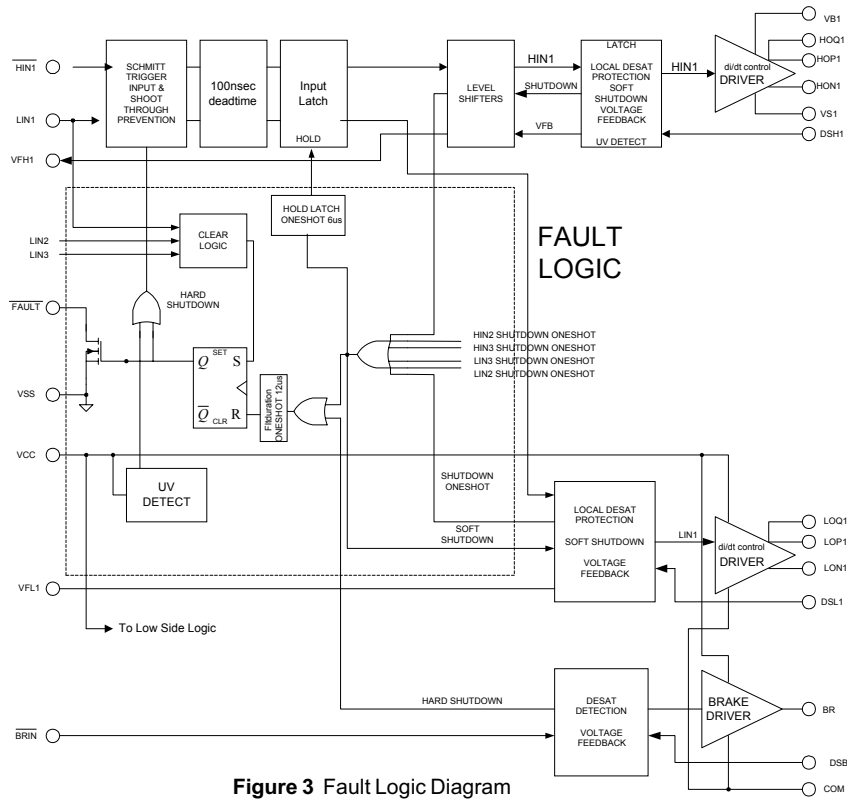


Figure 3 Fault Logic Diagram

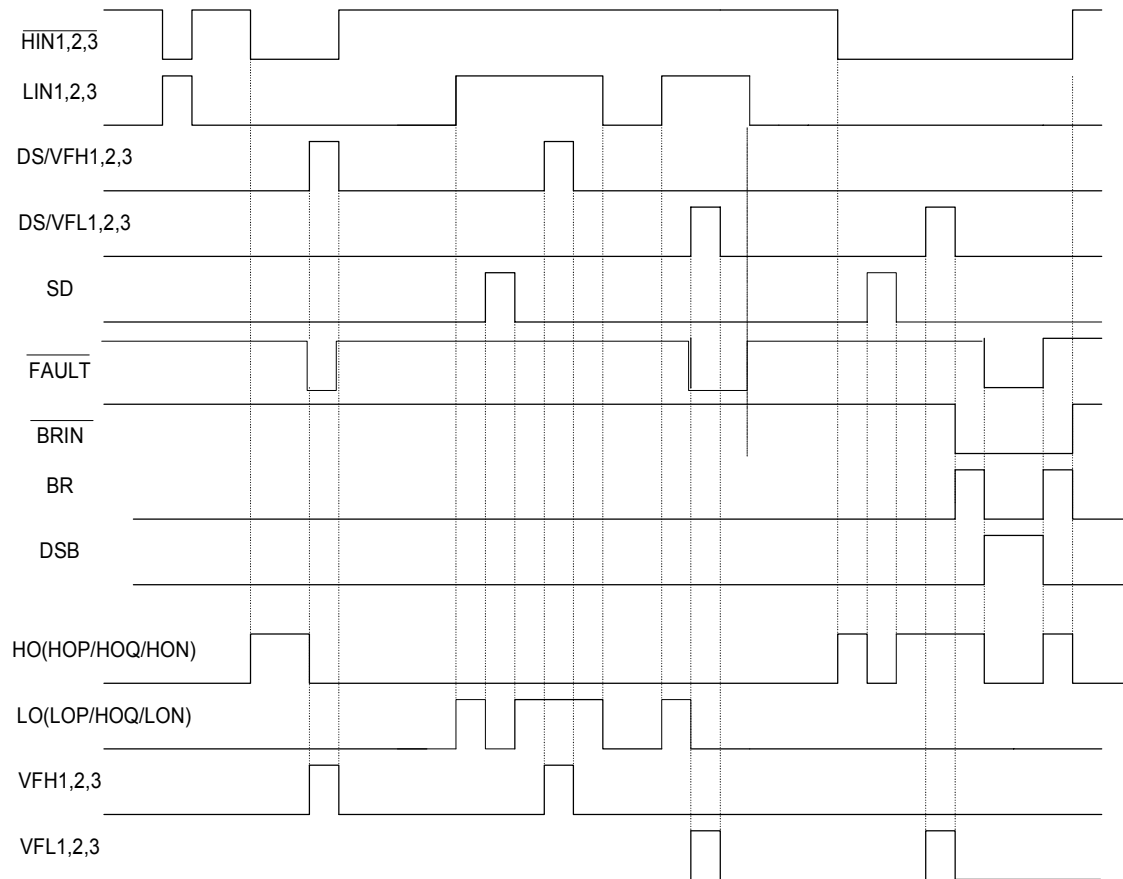


Figure 4 Input/Output Timing Diagram

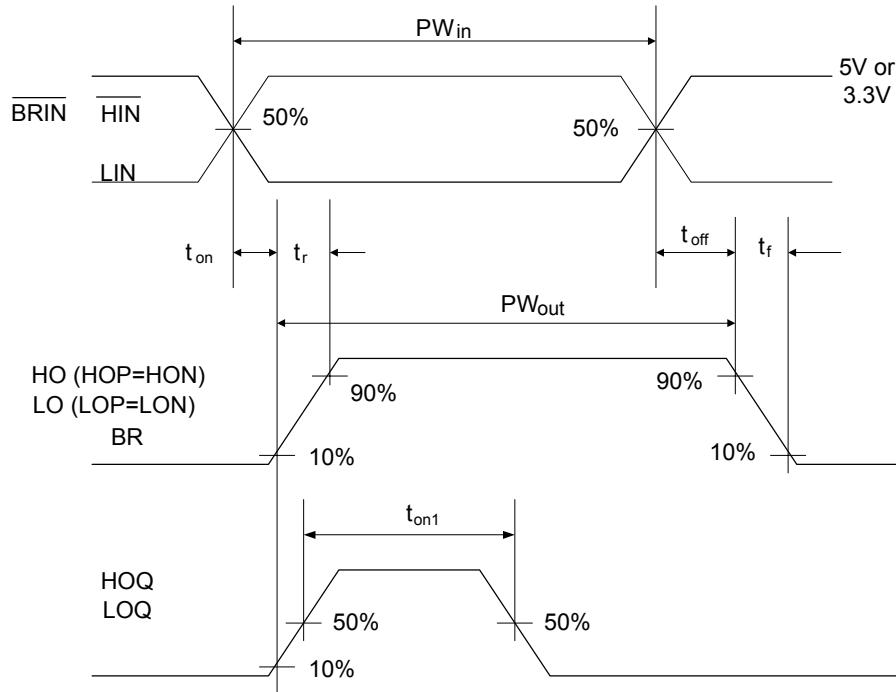


Figure 5 Switching Time Waveforms

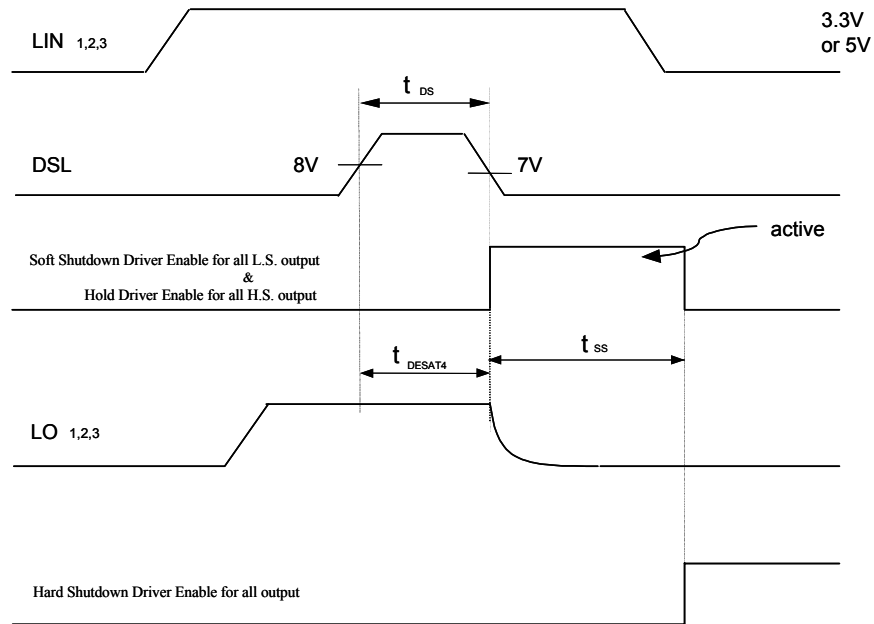


Figure 6.1 Low Side Desat Soft Shutdown Timing Waveform

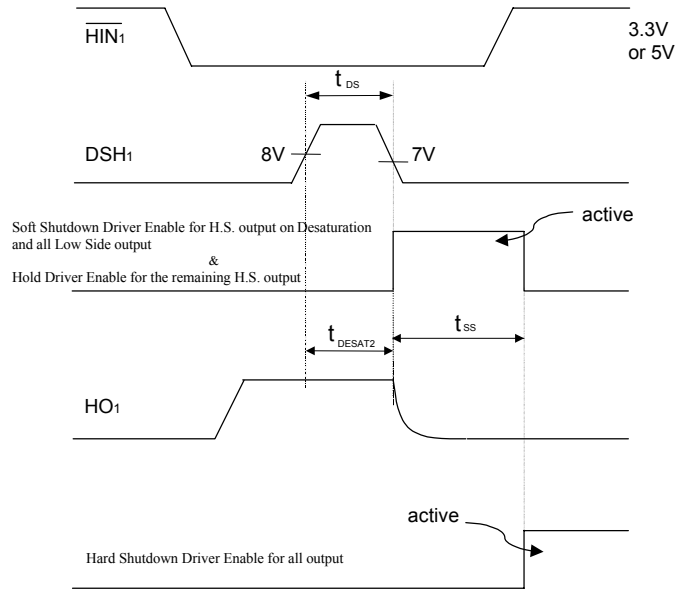


Figure 6.2 High Side Desat Soft Shutdown Timing Waveform

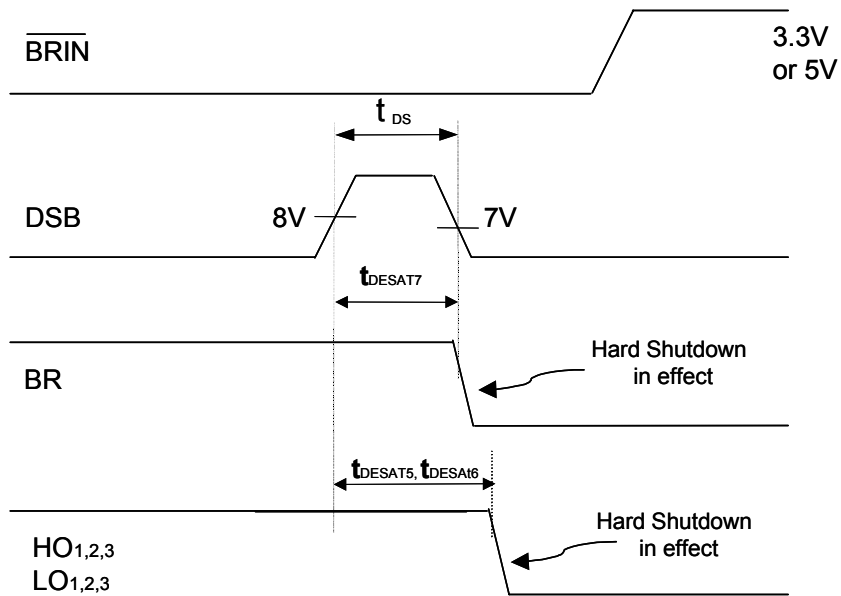


Figure 6.3 Brake Desat Timing Waveform

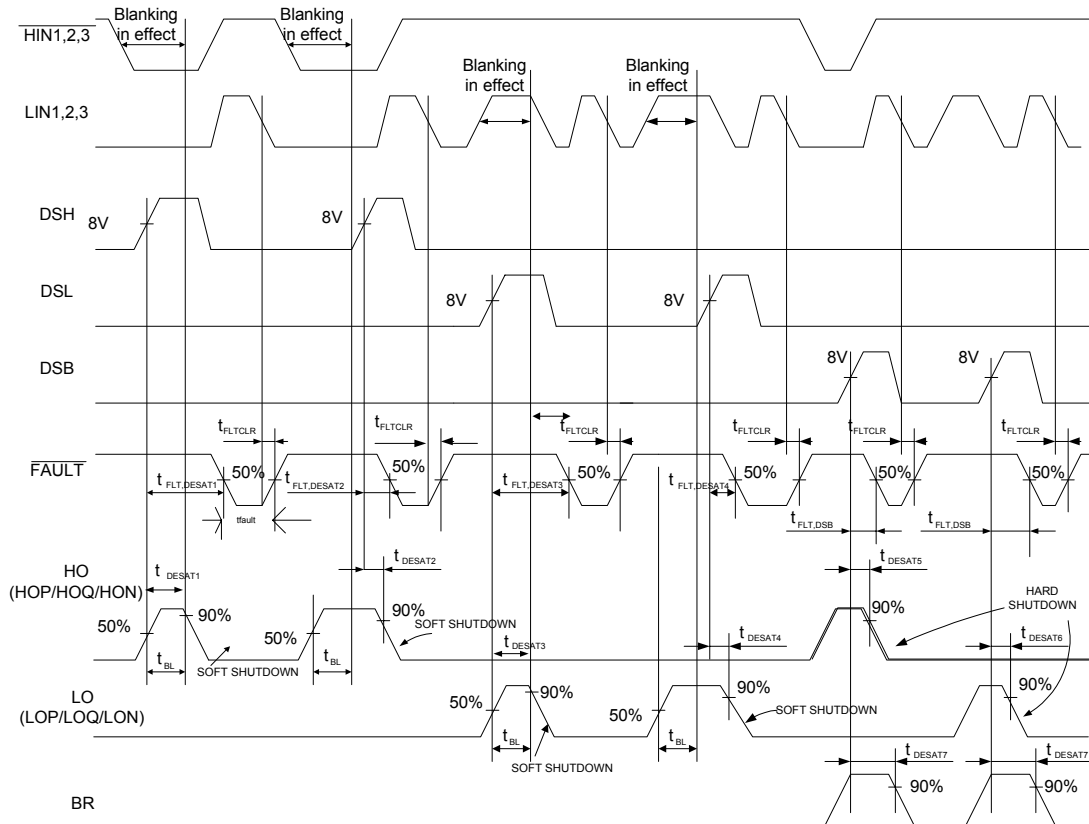


Figure 7 Desat Timing Diagram

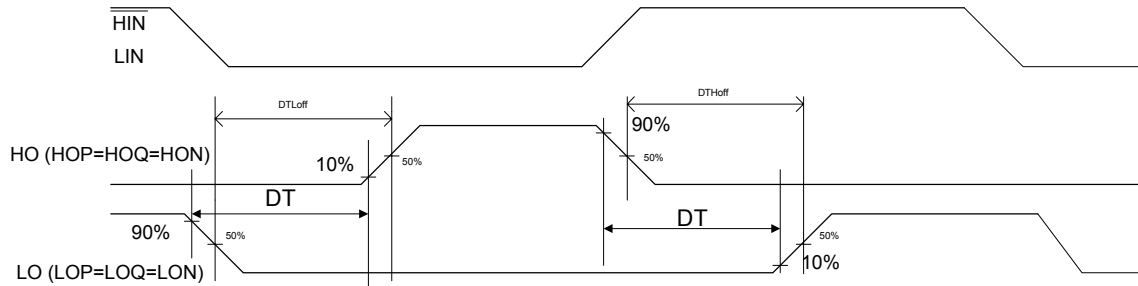


Figure 8 Internal Deadtime Timing

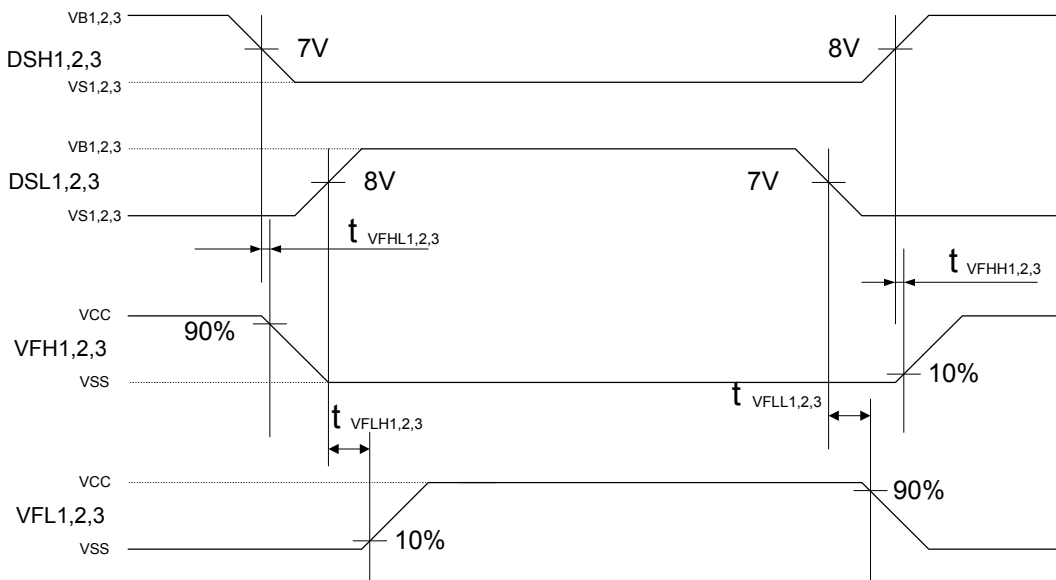


Figure 9 Voltage Feedback Timing

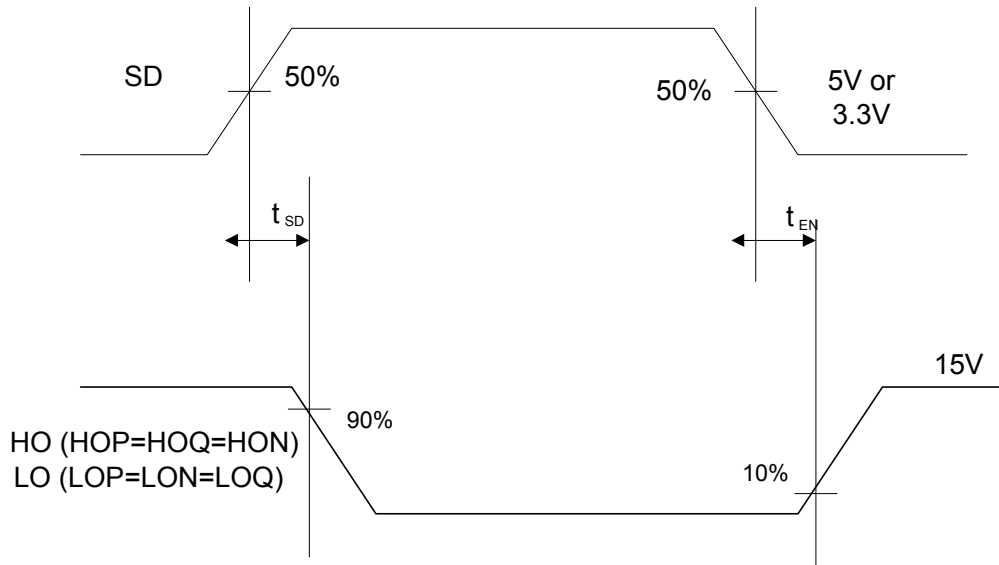


Figure 10 Shutdown Timing

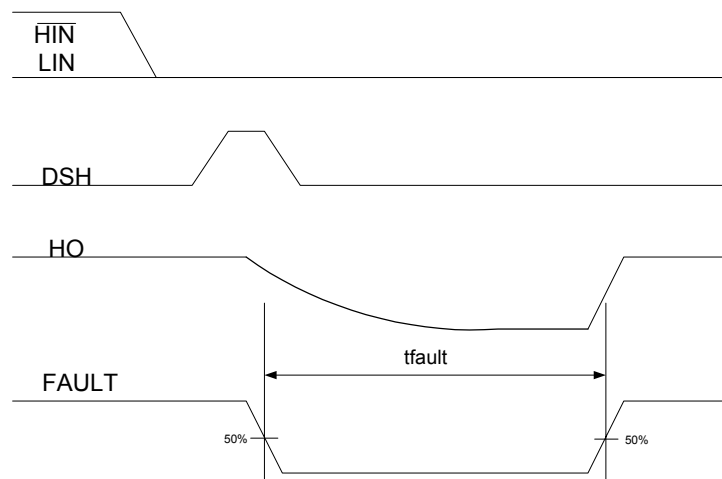


Figure 11 Fault Duration with Pending Faultclear Waveform
(refer to Note LD2 under the lead definition table)

Lead Definitions

Symbol	Description
V _{CC}	Low side supply voltage
V _{SS}	Logic Ground
HIN _{1,2,3}	Logic inputs for high side gate driver outputs (HOP _{1,2,3} /HON _{1,2,3} , out of phase)
LIN _{1,2,3}	Logic inputs for low side gate driver outputs (LOP _{1,2,3} /LON _{1,2,3} , out of phase)
FAULT	Fault output (latched and open drain)
SD	Shutdown input
DT	Deadtime programmable resistor pin
DSB	Brake IGBT desaturation protection input and voltage feedback input
BRIN	Logic input for brake driver
BR	Brake driver output
COM	Low side drivers return
V _B _{1,2,3}	High side gate drive floating supply
HOP _{1,2,3}	High side driver sourcing output
HOQ _{1,2,3}	High side driver boost sourcing output
HON _{1,2,3}	High side driver sinking output
DSH _{1,2,3}	IGBT desaturation protection input and high side voltage feedback input
V _S _{1,2,3}	High voltage floating supply return
LOP _{1,2,3}	Low side driver sourcing output
LON _{1,2,3}	Low side driver sinking output
DSL _{1,2,3}	IGBT desaturation protection input and low side voltage feedback input
VFH _{1,2,3}	High side voltage feedback logic output
VFL _{1,2,3}	Low side voltage feedback logic output

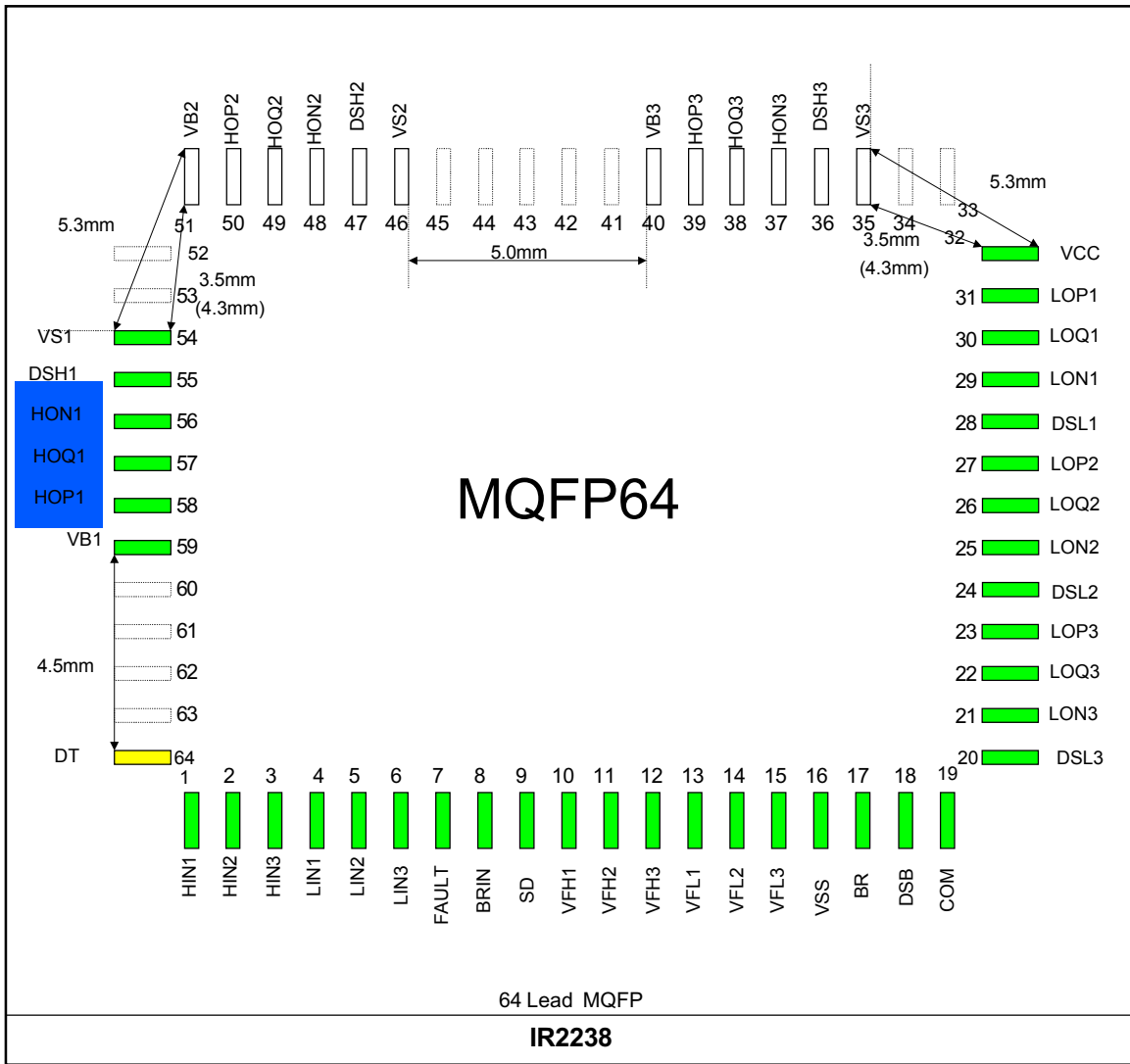
NOTE:

LD1- Low side soft shutdown is initiated locally in an event over current, which is sensed by the DSL pin. It is followed by the synchronized soft shutdown of the rest of the low side outputs; meanwhile it will hold all input information for a period of t_{ss} until the soft shutdown finishes. Then the hard shutdown will be initiated to complete the shut down cycle. (Figure 6.1)

High side soft shutdown is initiated locally in an event over current, which is sensed by the DSH pin. It is followed by the synchronized soft shutdown of all the low side outputs; meanwhile it will hold all input information for a period of t_{ss} until the soft shutdown finishes. Then the hard shutdown will be initiated to complete the shut down cycle. (Figure 6.2)

LD2- Soft shutdown is initiated in an event of overcurrent, which is followed by turn-off all six outputs. The fault condition will remain in a fixed period(t_{fault}) even though the faultclear condition is in effect (Fig11). In the case that faultclear is not in effect, fault duration = $t_{fault} + t_{ftclr}$.

Lead Assignments



Case outline

