

NP90N06VLK

60 V - 90 A - N-channel Power MOS FET

Application: Automotive

R07DS1318EJ0200 Rev.2.00 May 24, 2018

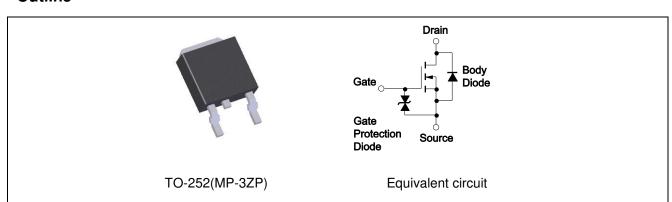
Description

NP90N06VLK is N-channel MOS Field Effect Transistor designed for high current switching applications.

Features

- Super low on-state resistance
 - $R_{DS(on)1} = 5.3$ mΩ MAX. ($V_{GS} = 10$ V, $I_D = 45$ A)
- Low C_{iss} : $C_{iss} = 4000 \text{ pF TYP.} (V_{DS} = 25 \text{ V})$
- Designed for automotive application and AEC-Q101 qualified

Outline



Remark: Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

Ordering Information

Part No.	Lead Plating	Packing		Package	
NP90N06VLK-E1-AY *1	Duro Cn /Tin)	Tape 2500 p/reel	Taping (E1 type)	TO-252(MP-3ZP)	
NP90N06VLK-E2-AY *1	Pure Sn (Tin)	rape 2500 p/reer	Taping (E2 type)	10-232(IVIF-32F)	

Note: *1. Pb-free (This product does not contain Pb in the external electrode)

Absolute Maximum Ratings $(T_A = 25^{\circ}C)$

Item	Symbol	Ratings	Unit
Drain to Source Voltage (V _{GS} = 0 V)	V _{DSS}	60	V
Gate to Source Voltage (V _{DS} = 0 V)	V _{GSS}	±20	V
Drain Current (DC) (T _C = 25°C)	I _{D(DC)}	±90	Α
Drain Current (pulse) *1*3	I _{D(pulse)}	±360	Α
Total Power Dissipation (T _C = 25°C)	P _{T1}	147	W
Total Power Dissipation (T _A = 25°C)	P _{T2}	1.2	W
Channel Temperature	T _{ch}	175	°C
Storage Temperature	T _{stg}	−55 to +175	°C
Repetitive Avalanche Current *2*3	I _{AR}	33	А
Repetitive Avalanche Energy *2*3	E _{AR}	108	mJ

Thermal Resistance

Channel to Case Thermal Resistance $R_{th(ch-C)}$ *3 1.02 °C/W Channel to Ambient Thermal Resistance $R_{th(ch-A)}$ *3 125 °C/W

Notes: *1. T_C = 25°C, PW \leq 10 μ s, Duty Cycle \leq 1%

*2. Rg = 25 Ω , Vgs = 20 V \rightarrow 0 V

*3. Not subject of production test. Verified by design/characterization.

Electrical Characteristics (T_A = 25°C)

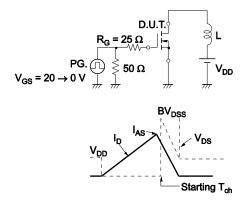
Item	Symbol	Min	Тур	Max	Unit	Test Conditions
Zero Gate Voltage Drain Current	I _{DSS}			1	μΑ	$V_{DS} = 60 \text{ V}, V_{GS} = 0 \text{ V}$
Gate Leakage Current	I _{GSS}			±10	μΑ	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$
Gate to Source Threshold Voltage	$V_{GS(th)}$	1.5	2.1	2.5	V	$V_{DS} = V_{GS}, I_D = 250 \mu A$
Forward Transfer Admittance *1	y _{fs}	40	80		S	$V_{DS} = 5 \text{ V}, I_{D} = 45 \text{ A}$
Drain to Source On-state	R _{DS(on)1}		3.8	5.3	mΩ	$V_{GS} = 10 \text{ V}, I_D = 45 \text{ A}$
Resistance *1	R _{DS(on)2}		4.9	8.2	mΩ	$V_{GS} = 4.5 \text{ V}, I_D = 23 \text{ A}$
Input Capacitance *2	C _{iss}		4000	6000	pF	$V_{DS} = 25 \text{ V},$
Output Capacitance *2	Coss		360	540	pF	$V_{GS} = 0 V$,
Reverse Transfer Capacitance *2	C _{rss}		110	200	pF	f = 1 MHz
Turn-on Delay Time *2	t _{d(on)}		24	60	ns	$V_{DD} = 30 \text{ V}, I_D = 45 \text{ A},$
Rise Time *2	t _r		7	20	ns	V _{GS} = 10 V,
Turn-off Delay Time *2	t _{d(off)}		60	120	ns	$R_G = 0 \Omega$
Fall Time *2	tf		6	20	ns	
Total Gate Charge *2	Q _G		63	95	nC	$V_{DD} = 48 \text{ V},$
Gate to Source Charge	Q _{GS}		15		nC	V _{GS} = 10 V,
Gate to Drain Charge	Q_{GD}		12		nC	I _D = 90 A
Body Diode Forward Voltage *1	V _{F(S-D)}		0.9	1.5	V	I _F = 90 A, V _{GS} = 0 V
Reverse Recovery Time	t _{rr}		40		ns	$I_F = 90 \text{ A}, V_{GS} = 0 \text{ V},$
Reverse Recovery Charge	Qrr		45		nC	di/dt = 100 A/μs

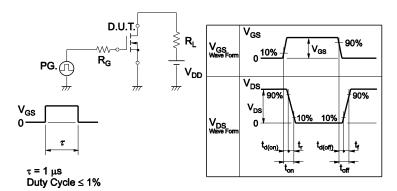
Note: *1. Pulsed test

Note: *2. Not subject of production test. Verified by design/characterization.

TEST CIRCUIT 1 AVALANCHE CAPABILITY

TEST CIRCUIT 2 SWITCHING TIME



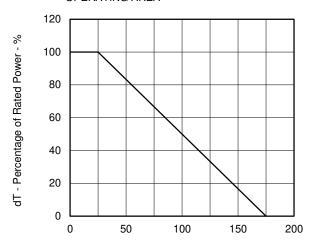


TEST CIRCUIT 3 GATE CHARGE

$$\begin{array}{c|c} \text{D.U.T.} & & \\ I_G = 2 \text{ mA} & & \\ \hline \\ PG. & > 50 \Omega & & \\ \hline \end{array} \begin{array}{c} R_L \\ \hline \\ W \end{array}$$

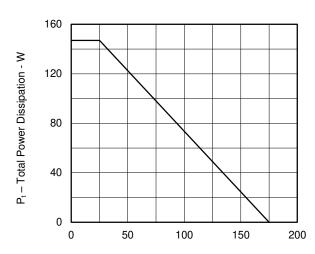
Typical Characteristics (T_A = 25°C)

DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



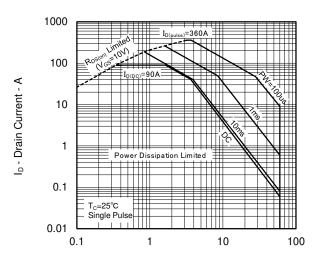
T_C - Case Temperature - °C

TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



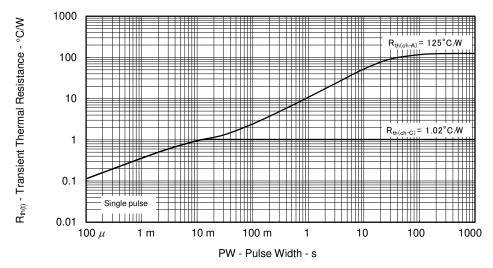
T_C - Case Temperature - °C

FORWARD BIAS SAFE OPERATING AREA

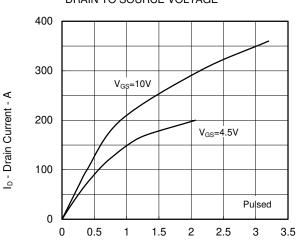


 V_{DS} - Drain to Source Voltage $-\ V$

TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH

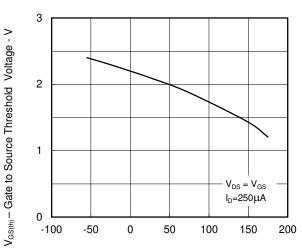


DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



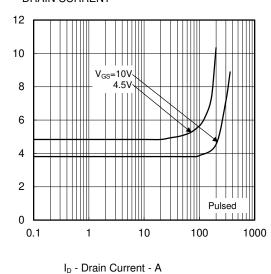
V_{DS} - Drain to Source Voltage - V

GATE TO SOURCE THRESHOLD VOLTAGE vs. CHANNEL TEMPERATURE

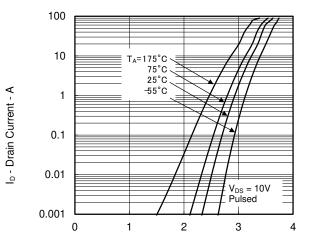


T_{ch} - Channel Temperature - °C

DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT

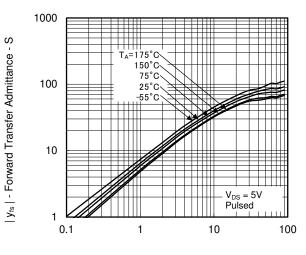


FORWARD TRANSFER CHARACTERISTICS



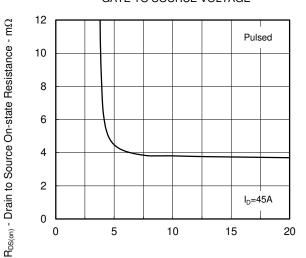
V_{GS} - Gate to Source Voltage - V

FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



I_D - Drain Current - A

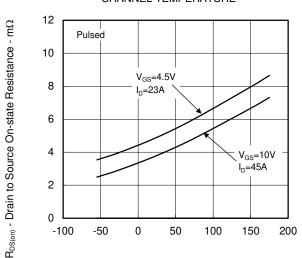
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



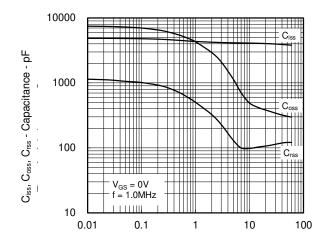
 V_{GS} - Gate to Source Voltage - V

 $R_{\text{DS(on)}}$ - Drain to Source On-state Resistance - $m\Omega$

td(on),tr,td(off),tr - Switching Time - ns

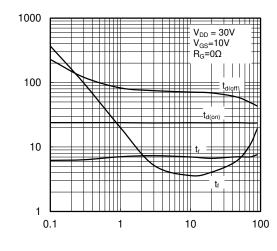


T_{ch} - Channel Temperature - °C



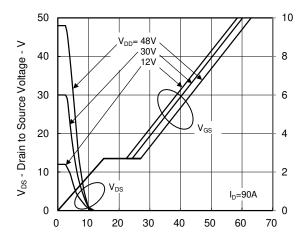
V_{DS} - Drain to Source Voltage - V

SWITCHING CHARACTERISTICS



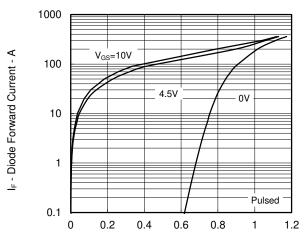
I_D - Drain Current - A

DYNAMIC INPUT CHARACTERISTICS



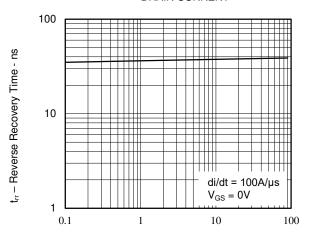
Q_G - Gate Charge - nC

SOURCE TO DRAIN DIODE FORWARD VOLTAGE



 $V_{F(S-D)}$ - Source to Drain Voltage - V

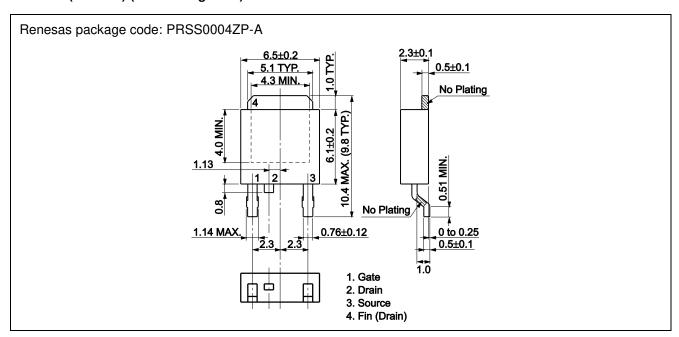
REVERSE RECOVERY TIME vs. DRAIN CURRENT



IF - Drain Current - A

Package Drawings (Unit: mm)

TO-252 (MP-3ZP) (Mass: 0.3 g TYP.)



Revision History

NP90N06VLK Data Sheet

		Description		
Rev.	Date	Page	Summary	
1.00	Jan. 12, 2016	_	First Edition Issued	
2.00	May 24 ,2018	2	Note 3 was added	
		3	Note 2 was added	

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