National Semiconductor

August 1998

100351
Low Power Hex D Flip-Flop

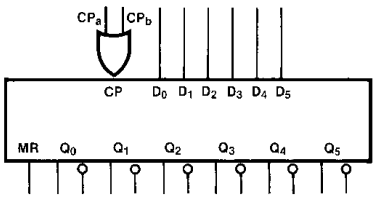
General Description

The 100351 contains six D-type edge-triggered, master/slave flip-flops with true and complement outputs, a pair of common Clock inputs (CP_a and CP_b) and common Master Reset (MR) input. Data enters a master when both CP_a and CP_b are LOW and transfers to the slave when CP_a and CP_b (or both) go HIGH. The MR input overrides all other inputs and makes the Q outputs LOW. All inputs have 50 kΩ pull-down resistors.

Features

- 40% power reduction of the 100151
- 2000V ESD protection
- Pin/function compatible with 100151
- Voltage compensated operating range: −4.2V to −5.7V
- Standard Microcircuit Drawing (SMD) 5962-9457901

Logic Symbol



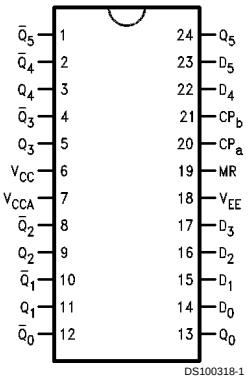
DS100318-11

Pin Names	Description
D_0–D_5	Data Inputs
CP_a, CP_b	Common Clock Inputs
MR	Asynchronous Master Reset Input
Q_0–Q_5	Data Outputs
$\overline{Q}_0$–$\overline{Q}_5$	Complementary Data Outputs

© 1998 National Semiconductor Corporation

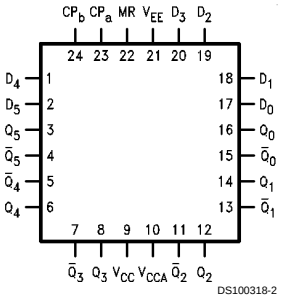
Connection Diagrams

24-Pin DIP



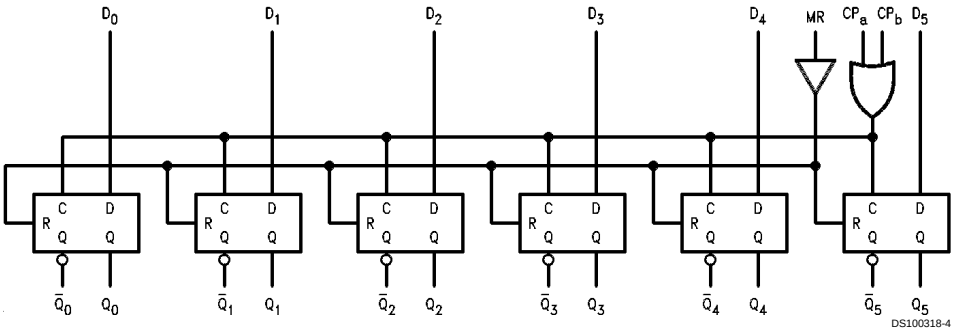
DS100318-1

24-Pin Quad Cerpak



DS100318-2

Logic Diagram



DS100318-4

Truth Tables (Each Flip-flop)

Synchronous Operation

Inputs				Outputs
D_n	CP_a	CP_b	MR	$Q_n(t+1)$
L	↗	L	L	L
H	↗	L	L	H
L	L	↗	L	L
H	L	↗	L	H
X	H	↗	L	$Q_n(t)$
X	↗	H	L	$Q_n(t)$
X	L	L	L	$Q_n(t)$

Asynchronous Operation

Inputs				Outputs
D_n	CP_a	CP_b	MR	$Q_n(t+1)$
X	X	X	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
t = Time before CP positive transition
t+1 = Time after CP positive transition
↗ = LOW-to-HIGH transition

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Above which the useful life may be impaired

Storage Temperature (T_{STG})	−65˚C to +150˚C
Maximum Junction Temperature (T_J)	
Ceramic	+175˚C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	−50 mA
ESD (Note 2)	≥2000V

Recommended Operating Conditions

Case Temperature (T_C)	
Military	−55˚C to +125˚C
Supply Voltage (V_{EE})	−5.7V to −4.2V

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Military Version

DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = −55˚C to +125˚C

Symbol	Parameter	Min	Max	Units	T_C	Conditions		Notes
V_{OH}	Output HIGH Voltage	−1025	−870	mV	0˚C to +125˚C	V_{IN} = V_{IH} (Max) or V_{IL} (Min)	Loading with 50Ω to −2.0V	(Notes 3, 4, 5)
		−1085	−870	mV	−55˚C			
V_{OL}	Output LOW Voltage	−1830	−1620	mV	0˚C to +125˚C			
		−1830	−1555	mV	−55˚C			
V_{OHC}	Output HIGH Voltage	−1035		mV	0˚C to +125˚C	V_{IN} = V_{IH} (Min) or V_{IL} (Max)	Loading with 50Ω to −2.0V	(Notes 3, 4, 5)
		−1085		mV	−55˚C			
V_{OLC}	Output LOW Voltage		−1610	mV	0˚C to +125˚C			
			−1555	mV	−55˚C			
V_{IH}	Input HIGH Voltage	−1165	−870	mV	−55˚C to +125˚C	Guaranteed HIGH Signal for All Inputs		(Notes 3, 4, 5, 6)
V_{IL}	Input LOW Voltage	−1830	−1475	mV	−55˚C to +125˚C	Guaranteed LOW Signal for All Inputs		(Notes 3, 4, 5, 6)
I_{IL}	Input LOW Current	0.50		µA	−55˚C to +125˚C	V_{EE} = −4.2V V_{IN} = V_{IL} (Min)		(Notes 3, 4, 5)
I_{IH}	Input HIGH Current					V_{EE} = −5.7V V_{IN} = V_{IH} (Max)		(Notes 3, 4, 5)
	CP, MR		350	µA	0˚C to +125˚C			
	D_0–D_5		240					
	CP, MR		500	µA	−55˚C			
	D_0–D_5		340					
I_{EE}	Power Supply Current	−135	−50	mA	−55˚C to +125˚C	Inputs Open		(Notes 3, 4, 5)

Note 3: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55˚C), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 4: Screen tested 100% on each device at −55˚C, +25˚C, and +125˚C, Subgroups 1, 2, 3, 7, and 8.

Note 5: Sample tested (Method 5005, Table I) on each manufactured lot at −55˚C, +25˚C, and +125˚C, Subgroups A1, 2, 3, 7, and 8.

Note 6: Guaranteed by applying specified input condition and testing V_{OH}/V_{OL}.

AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = −55˚C		T_C = +25˚C		T_C = +125˚C		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
f_{max}	Toggle Frequency	375		375		375		MHz	*Figures 2, 3*	(Note 10)
t_{PLH}	Propagation Delay	0.40	2.40	0.50	2.20	0.50	2.60	ns	*Figures 1, 3*	
t_{PHL}	CP_a, CP_b to Output									(Notes 7, 8, 9)
t_{PLH}	Propagation Delay	0.60	2.70	0.70	2.60	0.80	2.90	ns	*Figures 1, 4*	
t_{PHL}	MR to Output									
t_{TLH}	Transition Time	0.20	1.60	0.20	1.60	0.20	1.60	ns	*Figures 1, 3*	(Note 10)
t_{THL}	20% to 80%, 80% to 20%									
t_s	Setup Time									
	D_0–D_5	0.90		0.80		0.90		ns	*Figure 5*	
	MR (Release Time)	1.60		1.80		2.60			*Figure 4*	
t_h	Hold Time	1.50		1.40		1.60		ns	*Figure 5*	
	D_0–D_5									
t_{pw}(H)	Pulse Width HIGH	2.00		2.00		2.00		ns	*Figures 3, 4*	
	CP_a, CP_b, MR									

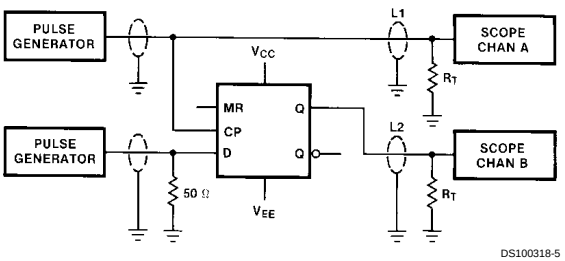
Note 7: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55˚C), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 8: Screen tested 100% on each device at +25˚C, Temperature only, Subgroup A9.

Note 9: Sample tested (Method 5005, Table I) on each Mfg. lot at +25˚C, Subgroup A9, and at +125˚C, and −55˚C Temperature, Subgroups A10 and A11.

Note 10: Not tested at +25˚C, +125˚C and −55˚C Temperature (design characterization data).

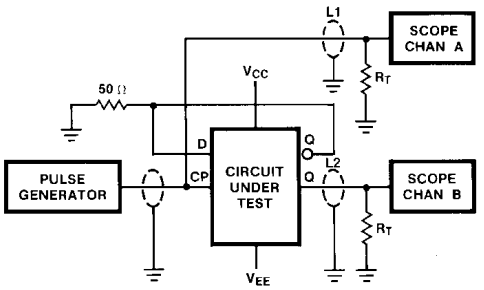
Test Circuitry



Notes:
V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V
L1 and L2 = equal length 50Ω impedance lines
R_T = 50Ω terminator internal to scope
Decoupling 0.1 µF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF

FIGURE 1. AC Test Circuit

Test Circuitry (Continued)



Notes:
V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V
L1 and L2 = equal length 50Ω impedance lines
R_T = 50Ω terminator internal to scope
Decoupling 0.1 µF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50Ω to GND
C_L = Jig and stray capacitance ≤ 3 pF

FIGURE 2. Toggle Frequency Test Circuit

Switching Waveforms

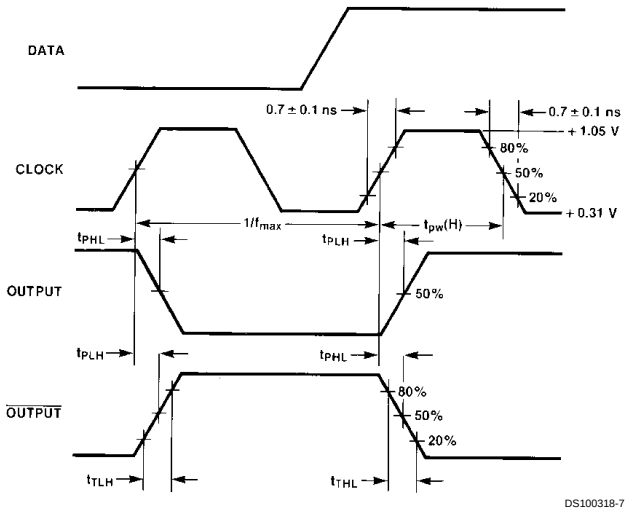


FIGURE 3. Propagation Delay (Clock) and Transition Times

Switching Waveforms (Continued)

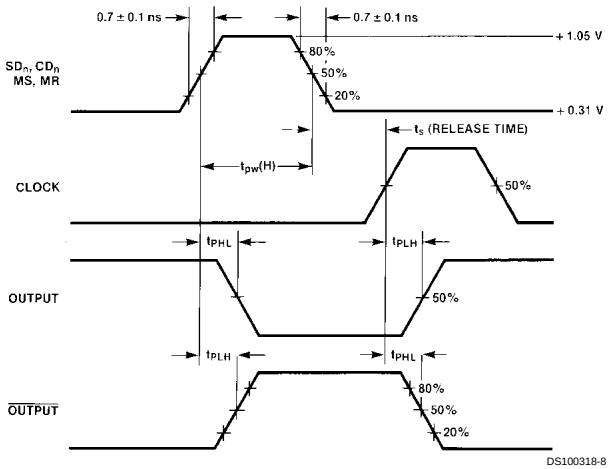
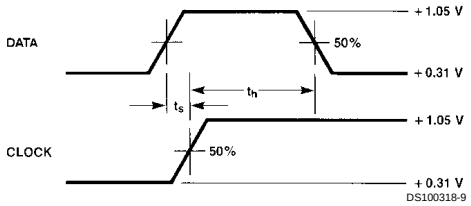


FIGURE 4. Propagation Delay (Reset)



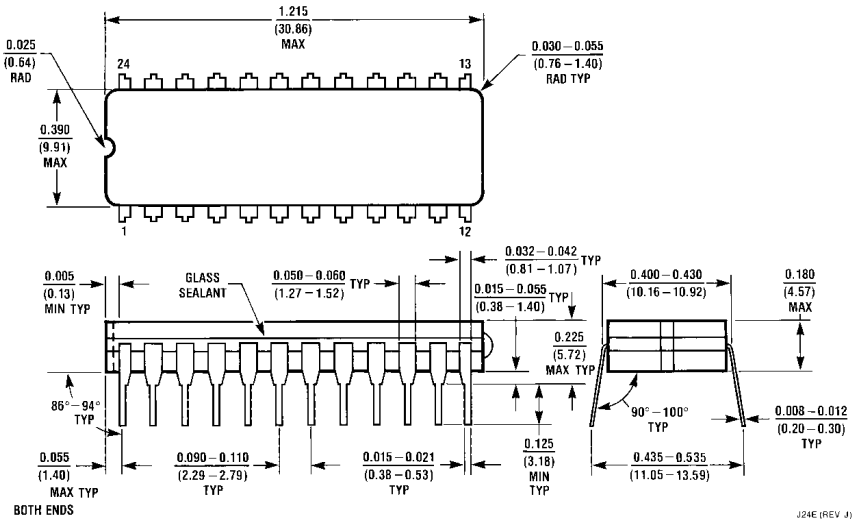
Notes:

t_s is the minimum time before the transition of the clock that information must be present at the data input.

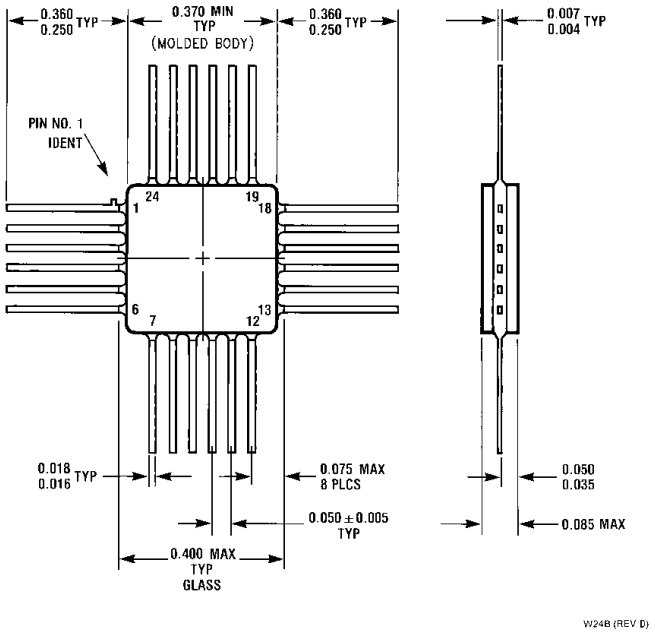
t_h is the minimum time after the transition of the clock that information must remain unchanged at the data input.

FIGURE 5. Setup and Hold Time

Physical Dimensions inches (millimeters) unless otherwise noted



24-Lead Ceramic Dual-In-Line Package (0.400" Wide) (D)
NS Package Number J24E



24-Lead Quad Cerpak (F)
NS Package Number W24B

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

National Semiconductor Corporation
Americas
Tel: 1-800-272-9959
Fax: 1-800-737-7018
Email: support@nsc.com

www.national.com

National Semiconductor Europe
Fax: +49 (0) 1 80-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 1 80-530 85 85
English Tel: +49 (0) 1 80-532 78 32
Français Tel: +49 (0) 1 80-532 93 58
Italiano Tel: +49 (0) 1 80-534 16 80

National Semiconductor Asia Pacific Customer Response Group
Tel: 65-2544466
Fax: 65-2504466
Email: sea.support@nsc.com

National Semiconductor Japan Ltd.
Tel: 81-3-5620-6175
Fax: 81-3-5620-6179

National does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and National reserves the right at any time without notice to change said circuitry and specifications.

100351 Product Folder

Low Power Hex D Flip-Flop

General Description | Features | Datasheet | Package & Models | Samples & Pricing

Datasheet

Title	Size in Kbytes	Date	View Online	Download	Receive via Email
100351 Low Power Hex D Flip-Flop	147 Kbytes	17-Aug-98	View Online	Download	Receive via Email
100351 Mil-Aero Datasheet MN100351-X	106 Kbytes		View Online	Download	Receive via Email

If you have trouble printing or viewing PDF file(s), see Printing Problems.

Package Availability, Models, Samples & Pricing

Part Number	Package			Status	Models		Samples & Electronic Orders	Budgetary Pricing		Std Pack Size	Package Marking
	Type	Pins	MSL		SPICE	IBIS		Qty	$US each		
5962-9457901MXA	CERDIP	24	MSL	Full production	N/A	N/A	Buy Now	50+	$41.6000	rail of 15	[logo]¢Z¢S¢4¢A$E 100351DMQB /Q 5962-9457901MXA
5962-9457901MYA	CERQUAD	24	MSL	Full production	N/A	N/A	Buy Now	50+	$44.0000	rail of 14	[logo]¢Z¢S¢4¢A Q$E 100351 FMQB 5962 -9457901 MYA
5962-9457901VXA	CERDIP	24	MSL	Full production	N/A	N/A		50+	$265.0000	rail of 15	[logo]¢Z¢S¢4¢A$E 100351J-QMLV 5962-9457901VXA
100351WFQMLV	CERQUAD	24	MSL	Preliminary	N/A	N/A				rail of N/A	[logo]¢Z¢S¢4¢A 100351WF QMLV 5962 F9457901 VYA $E
RM100351WFQMLV	CERQUAD	24	MSL	Preliminary	N/A	N/A				rail of N/A	[logo]¢Z¢S¢4¢A RM100351WF QMLV WFR# ¢R $E

100351W-QMLV	CERQUAD	24	MSL	Full production	N/A	N/A		50+	$265.0000	rail of 14	[logo]¢Z¢S¢4¢A 100351W-QMLV 5962-9457901 VYA $E

General Description

The 100351 contains six D-type edge-triggered, master/slave flip-flops with true and complement outputs, a pair of common Clock inputs (CP_a and CP_b) and common Master Reset (MR) input. Data enters a master when both CP_a and CP_b are LOW and transfers to the slave when CP_a and CP_b (or both) go HIGH. The MR input overrides all other inputs and makes the Q outputs LOW. All inputs have 50 k Ohm pull-down resistors.

Features

- 40% power reduction of the 100151
- 2000V ESD protection
- Pin/function compatible with 100151
- Voltage compensated operating range: -4.2V to -5.7V
- Standard Microcircuit Drawing (SMD) 5962-9457901

[Information as of 5-Aug-2002]

Search

Design Purchasing Quality Company Home

About Languages . Website Guide . About "Cookies" . National is QS 9000 Certified . Privacy/Security Statement . Contact Us . Site Terms & Conditions of Use . Copyright 2002 © National Semiconductor Corporation . My Preferences . Feedback