

## Features

- Split Gate Trench MOSFET Technology
- AEC-Q101 Qualified
- Moisture Sensitivity Level 1
- Extremely Low Switching Loss
- Fast Switching and Soft Recovery
- Halogen Free Available Upon Request By Adding Suffix "-HF"
- Epoxy Meets UL 94 V-0 Flammability Rating
- Lead Free Finish/RoHS Compliant ("P" Suffix Designates RoHS Compliant. See Ordering Information)

## Maximum Ratings

- Operating Junction Temperature Range : -55°C to +150°C
- Storage Temperature Range: -55°C to +150°C
- Thermal Resistance: 1.7°C/W Junction to Case (Steady-State)
- Thermal Resistance: 20°C/W Junction to Ambient (t≤10s)<sup>(1)</sup>
- Thermal Resistance: 50°C/W Junction to Ambient (Steady-State)<sup>(1)</sup>

Parameter	Symbol	Rating	Unit
Drain-Source Voltage	V <sub>DS</sub>	100	V
Gate-Source Voltage	V <sub>GS</sub>	±20	V
Continuous Drain Current	I <sub>D</sub>	45	A
Pulsed Drain Current <sup>(2)</sup>	I <sub>DM</sub>	180	A
Total Power Dissipation <sup>(3)</sup>	P <sub>D</sub>	72	W
Single Pulsed Avalanche Energy <sup>(4)</sup>	E <sub>AS</sub>	81	mJ

Note:

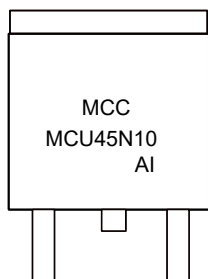
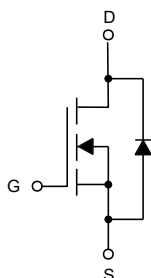
1. The value of R<sub>ΘJA</sub> is measured with the device mounted on 1in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25°C. The Power dissipation P<sub>DSM</sub> is based on R<sub>ΘJA</sub> t≤10s and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design.

2. Repetitive rating; pulse width limited by max. junction temperature.

3. P<sub>D</sub> is based on max. junction temperature, using junction-case thermal resistance.

4. V<sub>DD</sub>=50V, R<sub>G</sub>=25Ω, L=0.5mH, I<sub>AS</sub>=18A.

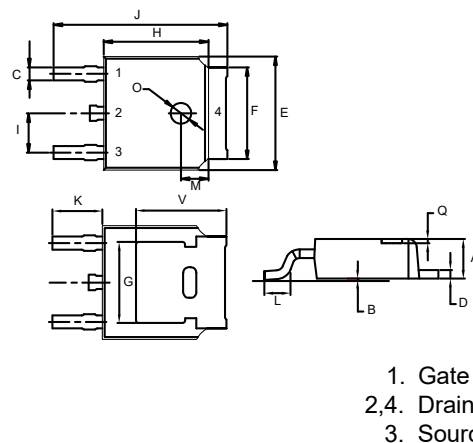
## Internal Structure and Marking Code



AI: 2 codes in total  
A is the year  
I is the month

# N-CHANNEL MOSFET

## DPAK(TO-252)



DIM	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
A	0.087	0.094	2.20	2.40	
B	0.000	0.005	0.00	0.13	
C	0.026	0.034	0.66	0.86	
D	0.018	0.023	0.46	0.58	
E	0.256	0.264	6.50	6.70	
F	0.201	0.215	5.10	5.46	
G	0.190		4.83		TYP.
H	0.236	0.244	6.00	6.20	
I	0.086	0.094	2.18	2.39	
J	0.386	0.409	9.80	10.40	
K	0.114		2.90		TYP.
L	0.055	0.067	1.40	1.70	
M	0.063		1.60		TYP.
O	0.043	0.051	1.10	1.30	
Q	0.000	0.012	0.00	0.30	
V	0.211		5.35		TYP.

**Electrical Characteristics @ 25°C (Unless Otherwise Specified)**

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
<b>Static Characteristics</b>						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\mu A$	100			V
Gate-Source Leakage Current	$I_{GSS}$	$V_{DS}=0V, V_{GS}=\pm 20V$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=100V, V_{GS}=0V$			1	$\mu A$
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1	1.8	2.5	V
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=20A$		14	17	m $\Omega$
		$V_{GS}=4.5V, I_D=20A$		17	21.5	m $\Omega$
Gate Resistance	$R_g$	f=1MHz, Open drain		1		$\Omega$
<b>Diode Characteristics</b>						
Continuous Body Diode Current	$I_S$				40	A
Diode Forward Voltage	$V_{SD}$	$V_{GS}=0V, I_S=20A$			1.3	V
Reverse Recovery Time	$t_{rr}$	$I_S=20A, di_F/dt=100A/\mu s$		39.8		ns
Reverse Recovery Charge	$Q_{rr}$			42		nC
<b>Dynamic Characteristics</b>						
Input Capacitance	$C_{iss}$	$V_{DS}=50V, V_{GS}=0V, f=1MHz$		1135		pF
Output Capacitance	$C_{oss}$			399		
Reverse Transfer Capacitance	$C_{rss}$			18		
Total Gate Charge	$Q_g$	$V_{DS}=50V, V_{GS}=10V, I_D=25A$		16		nC
Gate-Source Charge	$Q_{gs}$			5.6		
Gate-Drain Charge	$Q_{gd}$			2.4		
Turn-On Delay Time	$t_{d(on)}$	$V_{GS}=10V, V_{DD}=50V, I_D=25A$ $R_{GEN}=2.2\Omega$		39.2		ns
Turn-On Rise Time	$t_r$			11		
Turn-Off Delay Time	$t_{d(off)}$			53.2		
Turn-Off Fall Time	$t_f$			15.8		

**Curve Characteristics**

Fig. 1 - Typical Output Characteristics

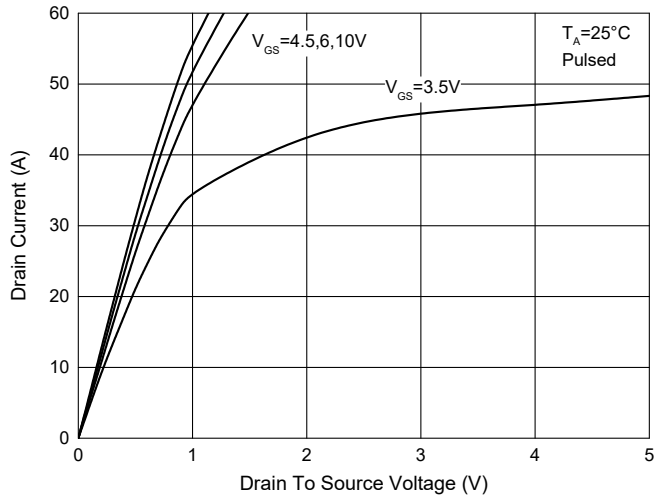


Fig. 2 - Transfer Characteristics

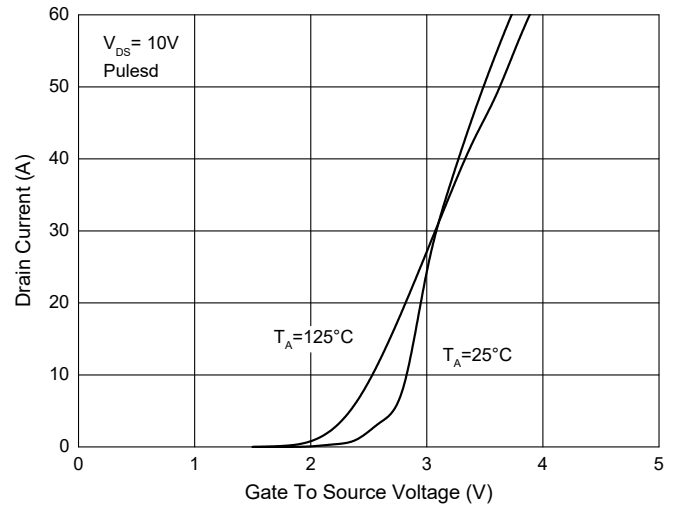


Fig. 3 -  $R_{DS(ON)} - I_D$

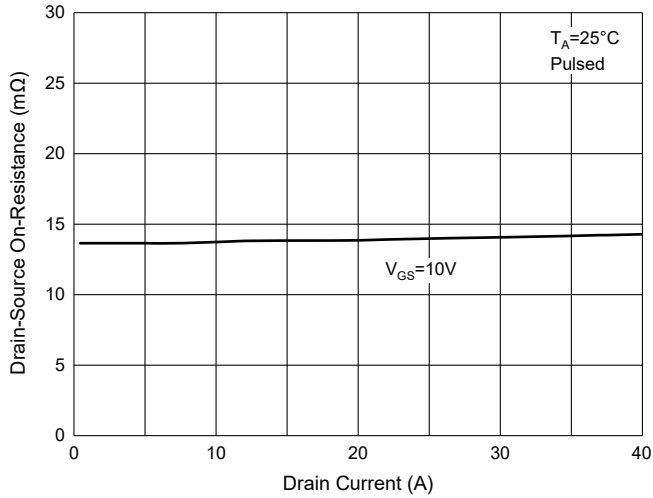


Fig. 4 - Normalized On Resistance Characteristics

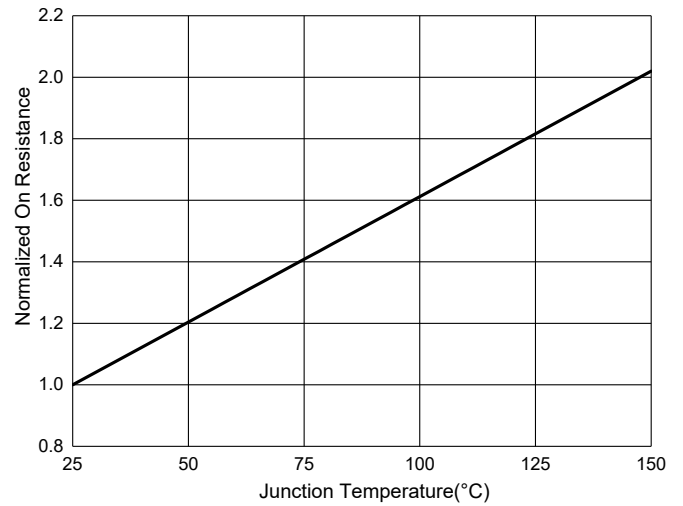


Fig. 5 - Capacitance Characteristics

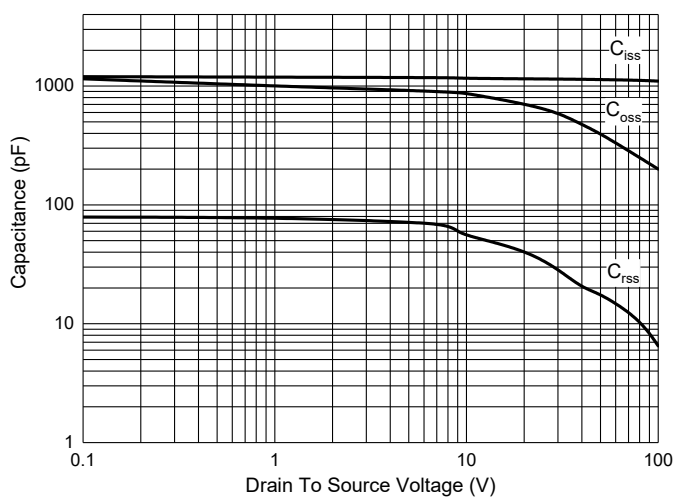
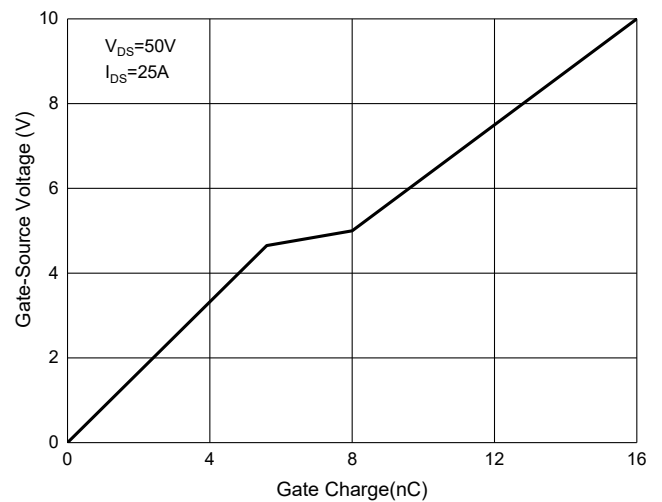


Fig. 6 - Gate Charge



Curve Characteristics

Fig. 7 - Safe Operation Area

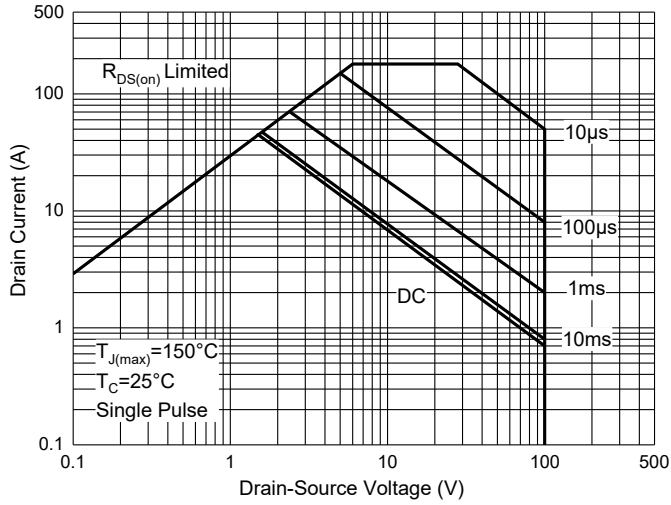


Fig. 8 - Power Derating Curve

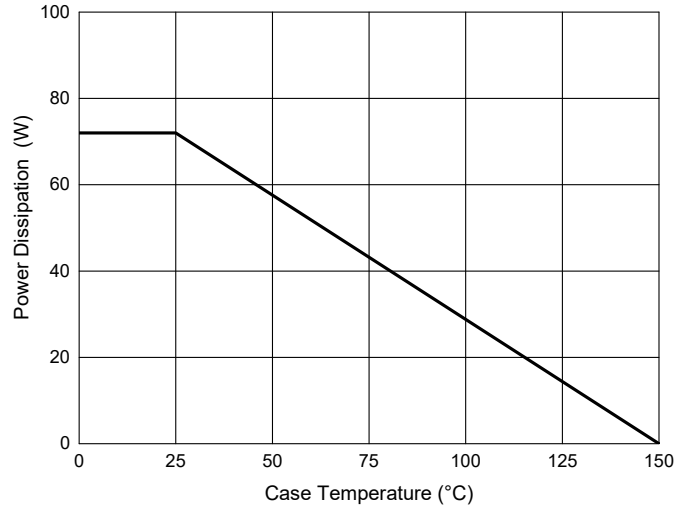
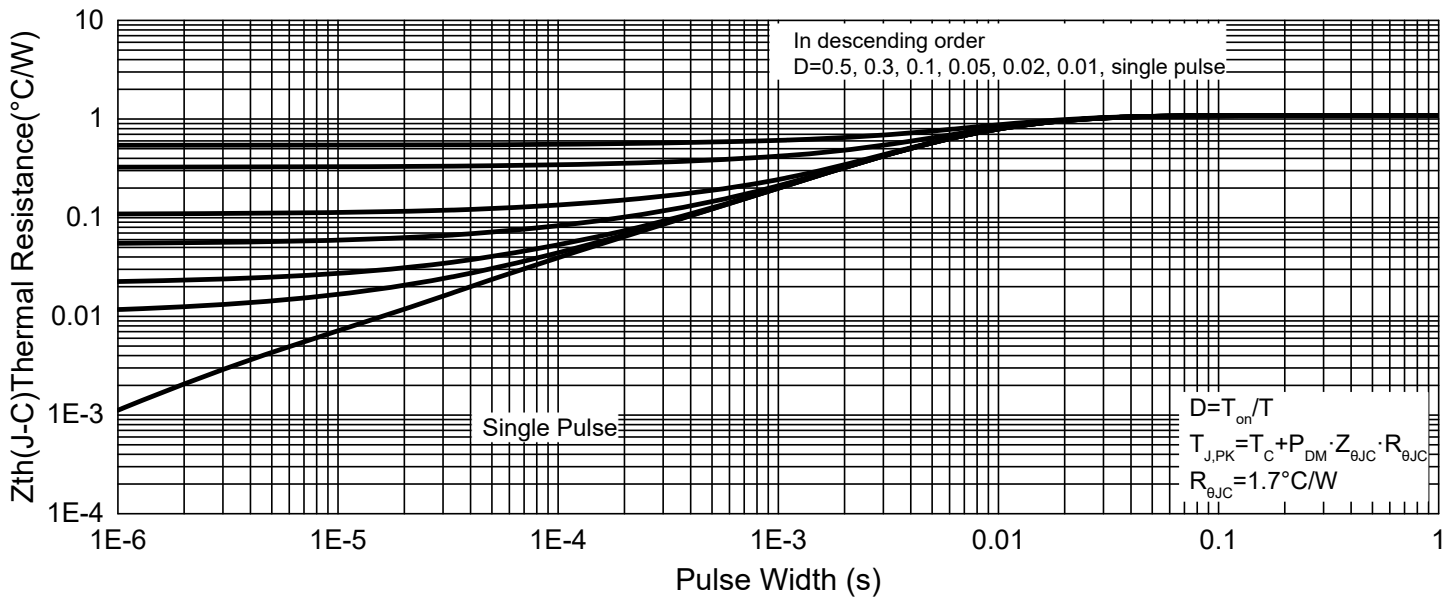


Fig. 9 - Maximum Transient Thermal Impedance



## Ordering Information

Device	Packing
Part Number-TP	Tape&Reel: 2.5Kpcs/Reel

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