

74VHC374 • 74VHCT374

Octal D Flip-Flop with TRI-STATE® Outputs

General Description

The VHC/VHCT374 is an advanced high speed CMOS octal flip-flop with TRI-STATE output fabricated with silicon gate CMOS technology. It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation. This 8-bit D-type flip-flop is controlled by a clock input (CP) and an output enable input (\overline{OE}). When the \overline{OE} input is high, the eight outputs are in a high impedance state.

An input protection circuit ensures that 0V–7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

Features

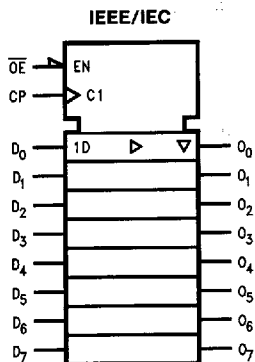
- High noise immunity:
VHC $V_{NIH} = V_{NIL} = 28\% V_{CC}$ (Min)
VHCT $V_{IH} = 2.0V$, $V_{IL} = 0.8V$
- Power down protection:
VHC inputs only
VHCT inputs and outputs
- Low noise:
VHC $V_{OLP} = 0.6V$ (typ)
VHCT $V_{OLP} = 0.8V$ (typ)
- Low power dissipation:
 $I_{CC} = 4 \mu A$ (Max) @ $T_A = 25^\circ C$
- Balanced propagation delays: $t_{PLH} \approx t_{PHL}$
- Pin and function compatible with 74HC/HCT374

Ordering Code: See Section 6

| Commercial | Package Number | Package Description |
|--------------|----------------|-----------------------------------|
| 74VHC374M | M20B | 20-Lead Molded JEDEC SOIC |
| 74VHC374SJ | M20D | 20-Lead Molded EIAJ SOIC |
| 74VHC374MSC | MSC20 | 20-Lead Molded EIAJ Type 1 SSOP |
| 74VHC374MTC | MTC20 | 20-Lead Molded JEDEC Type 1 TSSOP |
| 74VHC374N | N20A | 20-Lead Molded DIP |
| 74VHCT374M | M20B | 20-Lead Molded JEDEC SOIC |
| 74VHCT374SJ | M20D | 20-Lead Molded EIAJ SOIC |
| 74VHCT374MTC | MTC20 | 20-Lead Molded JEDEC Type 1 TSSOP |
| 74VHCT374N | N20A | 20-Lead Molded DIP |

Note: Surface mount packages are also available on Tape and Reel. Specify by appending the suffix letter "X" to the ordering code. EIAJ Type 1 SSOP available on Tape and Reel only, order MSCX.

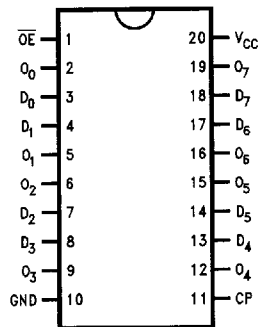
Logic Symbol



TL/F/11538-1

Connection Diagram

Pin Assignment for
DIP, SSOP, TSSOP and SOIC





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| Pin Names | Description |
|-----------------|-------------------------------|
| D_0 – D_7 | Data Inputs |
| CP | Clock Pulse Input |
| \overline{OE} | TRI-STATE Output Enable Input |
| O_0 – O_7 | TRI-STATE Outputs |

Functional Description

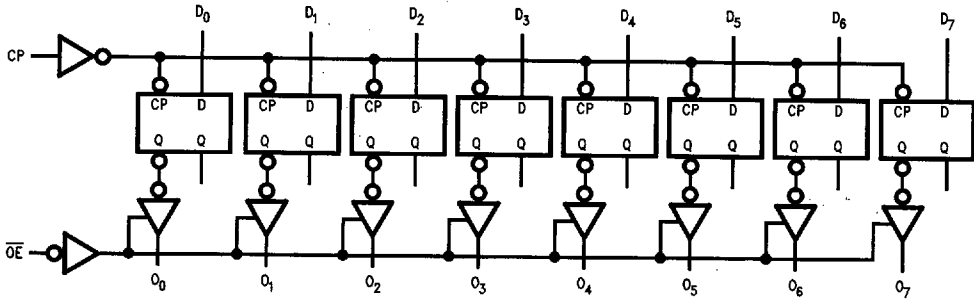
The 'VHC/'VHCT374 consists of eight edge-triggered flip-flops with individual D-type inputs and TRI-STATE true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable (\overline{OE}) LOW, the contents of the eight flip-flops are available at the outputs. When the \overline{OE} is HIGH, the outputs go to the high impedance state. Operation of the \overline{OE} input does not affect the state of the flip-flops.

Truth Table

| Inputs | | | Outputs |
|--------|---|-----------------|---------|
| D_n | CP | \overline{OE} | O_n |
| H |  | L | H |
| L |  | L | L |
| X | X | H | Z |

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial
 Z = High Impedance
 = LOW-to-HIGH Transition

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

| | |
|---------------------------------------|--------------------------|
| Supply Voltage (V_{CC}) | -0.5V to +7.0V |
| DC Input Voltage (V_{IN}) | -0.5V to +7.0V |
| DC Output Voltage (V_{OUT}) | -0.5V to $V_{CC} + 0.5V$ |
| VHC | -0.5V to +7.0V |
| VHCT* | -0.5V to +7.0V |
| Input Diode Current (I_{IK}) | -20 mA |
| Output Diode Current (VHC) | ±20 mA |
| (VHCT) | -20 mA |
| DC Output Current (I_{OUT}) | ±25 mA |
| DC V_{CC} /GND Current (I_{CC}) | ±75 mA |
| Storage Temperature (T_{STG}) | -65°C to +150°C |
| Lead Temperature (T_L) | 260°C |
| (Soldering, 10 seconds) | |

* $V_{OUT} > V_{CC}$ only if output is in H or Z state.

Note 1: *Absolute Maximum Ratings are values beyond which the device may be damaged or have its useful life impaired. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation outside databook specifications.*

Recommended Operating Conditions

| | | |
|---|-------------------------------------|----------------|
| Supply Voltage (V_{CC}) | VHC | 2.0V to +5.5V |
| | VHCT | 4.5V to +5.5V |
| Input Voltage (V_{IN}) | | 0V to +5.5V |
| Output Voltage (V_{OUT}) | | 0V to V_{CC} |
| Operating Temperature (T_{OPR}) | 74 VHC/VHCT | -40°C to +85°C |
| Input Rise and Fall Time (t_r, t_f) | | |
| | $V_{CC} = 3.3V \pm 0.3V$ (VHC only) | 0 ~ 100 ns/V |
| | $V_{CC} = 5.0V \pm 0.5V$ | 0 ~ 20 ns/V |

DC Characteristics for 'VHC Family Devices

| Symbol | Parameter | V_{CC} (V) | 74VHC | | 74VHC | | Units | Conditions | | |
|----------|------------------------------------|-----------------|--------------------|-------|-------|---|-------|------------|--|--|
| | | | $T_A = 25^\circ C$ | | | $T_A = -40^\circ C$ to $+85^\circ C$ | | | | |
| | | | Min | Typ | Max | Min | | | | Max |
| V_{IH} | High Level Input Voltage | 2.0 3.0-5.5 | 1.50 | | | 1.50 | | V | | |
| | | | 0.7 V_{CC} | | | 0.7 V_{CC} | | | | |
| V_{IL} | Low Level Input Voltage | 2.0 3.0-5.5 | | 0.50 | | 0.50 | | V | | |
| | | | 0.3 V_{CC} | | | 0.3 V_{CC} | | | | |
| V_{OH} | High Level Output Voltage | 2.0 | 1.9 | 2.0 | | 1.9 | | V | $V_{IN} = V_{IH}$ or V_{IL} | $I_{OH} = -50 \mu A$ |
| | | 3.0 | 2.9 | 3.0 | | 2.9 | | | | |
| | | 4.5 | 4.4 | 4.5 | | 4.4 | | | | |
| | | 3.0 | 2.58 | | | 2.48 | | V | | $I_{OH} = -4 \text{ mA}$ $I_{OH} = -8 \text{ mA}$ |
| | | 4.5 | 3.94 | | | 3.80 | | | | |
| V_{OL} | Low Level Output Voltage | 2.0 | | 0.0 | 0.1 | | 0.1 | V | $V_{IN} = V_{IH}$ or V_{IL} | $I_{OL} = 50 \mu A$ |
| | | 3.0 | | 0.0 | 0.1 | | 0.1 | | | |
| | | 4.5 | | 0.0 | 0.1 | | 0.1 | | | |
| | | 3.0 | | | 0.36 | | 0.50 | V | | $I_{OL} = 4 \text{ mA}$ $I_{OL} = 8 \text{ mA}$ |
| 4.5 | | | 0.36 | | 0.44 | | | | | |
| I_{OZ} | TRI-STATE Output Off-State Current | 5.5 | | ±0.25 | | ±2.5 | | μA | $V_{IN} = V_{IH}$ or V_{IL} $V_{OUT} = V_{CC}$ or GND | |
| I_{IN} | Input Leakage Current | 0-5.5 | | ±0.1 | | ±1.0 | | μA | $V_{IN} = 5.5V$ or GND | |
| I_{CC} | Quiescent Supply Current | 5.5 | | 4.0 | | 40.0 | | μA | $V_{IN} = V_{CC}$ or GND | |

DC Characteristics for 'VHC Family Devices: See Section 2 for Waveforms (Continued)

| Symbol | Parameter | V _{CC} (V) | 74VHC | | Units | Conditions | Fig. No. |
|---------------------|--|------------------------|-----------------------|--------|-------|------------------------|----------|
| | | | T _A = 25°C | | | | |
| | | | Typ | Limits | | | |
| **V _{OLP} | Quiet Output Maximum Dynamic V _{OL} | 5.0 | 0.6 | 0.9 | V | C _L = 50 pF | 2-11, 12 |
| **V _{OLV} | Quiet Output Minimum Dynamic V _{OL} | 5.0 | -0.6 | -0.9 | V | C _L = 50 pF | 2-11, 12 |
| **V _{IHD} | Minimum High Level Dynamic Input Voltage | 5.0 | | 3.5 | V | C _L = 50 pF | 2-11, 12 |
| **V _{I LD} | Maximum Low Level Dynamic Input Voltage | 5.0 | | 1.5 | V | C _L = 50 pF | 2-11, 12 |

**Parameter guaranteed by design.

DC Characteristics for 'VHCT Family Devices

| Symbol | Parameter | V _{CC} (V) | 74VHCT | | | 74VHCT | | Units | Conditions |
|-------------------|---|------------------------|-----------------------|------|-------|---------------------------------|------|---|------------|
| | | | T _A = 25°C | | | T _A = -40°C to +85°C | | | |
| | | | Min | Typ | Max | Min | Max | | |
| V _{IH} | High Level Input Voltage | 4.5 5.5 | 2.0 | | | 2.0 | | | |
| V _{IL} | Low Level Input Voltage | 4.5 5.5 | | | 0.8 | 0.8 | | | |
| V _{OH} | High Level Output Voltage | 4.5 | 3.15 | 3.65 | | 3.15 | | V _{IN} = V _{IH} or V _{IL} I _{OH} = -50 μA I _{OH} = -8 mA | |
| | | | 2.5 | | | 2.4 | | | |
| V _{OL} | Low Level Output Voltage | 4.5 | | 0.0 | 0.1 | | 0.1 | V _{IN} = V _{IH} or V _{IL} I _{OH} = -50 μA I _{OH} = -8 mA | |
| | | | | | 0.36 | | 0.44 | | |
| I _{OZ} | TRI-STATE Output Off-State Current | 5.5 | | | ±0.25 | | ±2.5 | V _{IN} = V _{IH} or V _{IL} V _{OUT} = V _{CC} or GND | |
| I _{IN} | Input Leakage Current | 0-5.5 | | | ±0.1 | | ±1.0 | V _{IN} = 5.5V or GND | |
| I _{CC} | Quiescent Supply Current | 5.5 | | | 4.0 | | 40.0 | V _{IN} = V _{CC} or GND | |
| I _{CC T} | Maximum I _{CC} /Input | 5.5 | | | 1.35 | | 1.50 | V _{IN} = 3.4V Other Inputs = V _{CC} or GND | |
| I _{OPD} | Output Leakage Current (Power Down State) | 0.0 | | | ±0.5 | | +5.0 | V _{OUT} = 5.5V | |

DC Characteristics for 'VHCT Family Devices: See Section 2 for Waveforms (Continued)

| Symbol | Parameter | V _{CC} (V) | 74VHCT | | Units | Conditions | Fig. No. |
|--------------------|--|------------------------|-----------------------|--------|-------|------------------------|-------------|
| | | | T _A = 25°C | | | | |
| | | | Typ | Limits | | | |
| **V _{OLP} | Quiet Output Maximum Dynamic V _{OL} | 5.0 | 0.8 | 1.2 | V | C _L = 50 pF | 2-11, 12 |
| **V _{OLV} | Quiet Output Minimum Dynamic V _{OL} | 5.0 | -0.8 | -1.2 | V | C _L = 50 pF | 2-11, 12 |
| **V _{IHD} | Minimum High Level Dynamic Input Voltage | 5.0 | | 2.0 | V | C _L = 50 pF | 2-11, 12 |
| **V _{ILD} | Maximum Low Level Dynamic Input Voltage | 5.0 | | 0.8 | V | C _L = 50 pF | 2-11, 12 |

**Parameter guaranteed by design.

AC Electrical Characteristics for 'VHC Family Devices : See Section 2 for Waveforms

| Symbol | Parameter | V _{CC} (V) | 74VHC | | 74VHC | | Units | Conditions | Fig. No. | |
|--|---|------------------------|-----------------------|------|-------|------------------------------------|-------|------------------------|------------------------|--------|
| | | | T _A = 25°C | | | T _A = -40°C to +85°C | | | | |
| | | | Min | Typ | Max | Min | | | | Max |
| t _{PLH} t _{PHL} | Propagation Delay Time (CP to O _n) | 3.3 ± 0.3 | 8.1 | 12.7 | 1.0 | 15.0 | ns | C _L = 15 pF | 2-5, 6 | |
| | | | 10.6 | 16.2 | 1.0 | 18.5 | | C _L = 50 pF | | |
| | | 5.0 ± 0.5 | 5.4 | 8.1 | 1.0 | 9.5 | ns | C _L = 15 pF | 2-5, 6 | |
| | | | 6.9 | 10.1 | 1.0 | 11.5 | | C _L = 50 pF | | |
| t _{PZL} t _{PZH} | TRI-STATE Output Enable Time | 3.3 ± 0.3 | 7.1 | 11.0 | 1.0 | 13.0 | ns | R _L = 1 kΩ | C _L = 15 pF | 2-7, 8 |
| | | | 9.6 | 14.5 | 1.0 | 16.5 | | C _L = 50 pF | | |
| | | 5.0 ± 0.5 | 5.1 | 7.6 | 1.0 | 9.0 | ns | | C _L = 15 pF | 2-7, 8 |
| | | | 6.6 | 9.6 | 1.0 | 11.0 | | C _L = 50 pF | | |
| t _{PLZ} t _{PHZ} | TRI-STATE Output Disable Time | 3.3 ± 0.3 | 10.2 | 14.0 | 1.0 | 16.0 | ns | R _L = 1 kΩ | C _L = 50 pF | 2-7, 8 |
| | | 5.0 ± 0.5 | 6.1 | 8.8 | 1.0 | 10.0 | | C _L = 50 pF | 2-7, 8 | |
| t _{OSLH} t _{OSSL} | Output to Output Skew | 3.3 ± 0.3 | | 1.5 | | 1.5 | ns | (Note 1) | C _L = 50 pF | |
| | | 5.0 ± 0.5 | | 1.0 | | 1.0 | | | C _L = 50 pF | |
| f _{MAX} | Maximum Clock Frequency | 3.3 ± 0.3 | 80 | 130 | 70 | MHz | | C _L = 15 pF | | |
| | | | 55 | 85 | 50 | | | C _L = 50 pF | | |
| | | 5.0 ± 0.5 | 130 | 185 | 110 | | | C _L = 15 pF | | |
| | | | 85 | 120 | 75 | | | C _L = 50 pF | | |
| C _{IN} | Input Capacitance | | 4 | 10 | | 10 | pF | V _{CC} = Open | | |

AC Electrical Characteristics for 'VHC Family Devices (Continued)

| Symbol | Parameter | V _{CC} (V) | 74VHC | | | Units | Conditions | Fig. No. |
|------------------|-------------------------------|------------------------|-----------------------|-----|-----|-------|------------------------|-------------|
| | | | T _A = 25°C | | | | | |
| | | | Min | Typ | Max | | | |
| C _{OUT} | Output Capacitance | | 6 | | | pF | V _{CC} = 5.0V | |
| C _{PD} | Power Dissipation Capacitance | | 32 | | | pF | (Note 2) | |

Note 1: Parameter guaranteed by design. $t_{OSLH} = |t_{PLH\ max} - t_{PLH\ min}|$; $t_{OSHL} = |t_{PHL\ max} - t_{PHL\ min}|$

Note 2: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC\ (opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8$ (per F/F). The total C_{PD} when n pcs. of the Octal D Flip-Flop operates can be calculated by the equation: $C_{PD\ (total)} = 20 + 12n$.

AC Operating Requirements for 'VHC Family Devices: See Section 2 for Waveforms

| Symbol | Parameter | V _{CC} (V) | 74VHC | | | 74VHC | | Units | Conditions | Fig. No. |
|--|--------------------------|------------------------|-----------------------|-----|-----|------------------------------------|-----|-------|------------|-------------|
| | | | T _A = 25°C | | | T _A = -40°C to +85°C | | | | |
| | | | Min | Typ | Max | Min | Max | | | |
| t _{w(H)} t _{w(L)} | Minimum Pulse Width (CP) | 3.3 ± 0.3 | 5.0 | | 5.5 | | ns | | 2-6 | |
| | | 5.0 ± 0.5 | 5.0 | | 5.0 | | | | | |
| t _S | Minimum Set-Up Time | 3.3 ± 0.3 | 4.5 | | 4.5 | | ns | | 2-9 | |
| | | 5.0 ± 0.5 | 3.0 | | 3.0 | | | | | |
| t _H | Minimum Hold Time | 3.3 ± 0.3 | 2.0 | | 2.0 | | ns | | 2-9 | |
| | | 5.0 ± 0.5 | 2.0 | | 2.0 | | | | | |

AC Electrical Characteristics for 'VHCT Family Devices: See Section 2 for Waveforms

| Symbol | Parameter | V _{CC} (V) | 74VHCT | | | 74VHCT | | Units | Conditions | Fig. No. |
|--|-------------------------------------|------------------------|-----------------------|------|-----|------------------------------------|-----|------------------------|------------------------|-------------|
| | | | T _A = 25°C | | | T _A = -40°C to +85°C | | | | |
| | | | Min | Typ | Max | Min | Max | | | |
| t _{PLH} t _{PHL} | Propagation Delay Time | 5.0 ± 0.5 | 5.6 | 9.4 | 1.0 | 10.5 | ns | C _L = 15 pF | 2-5, 6 | |
| | | | 6.4 | 10.4 | 1.0 | 11.5 | | C _L = 50 pF | 2-5, 6 | |
| t _{PZL} t _{PZH} | TRI-STATE Output Enable Time | 5.0 ± 0.5 | 6.5 | 10.2 | 1.0 | 11.5 | ns | R _L = 1 kΩ | C _L = 15 pF | 2-7, 8 |
| | | | 7.3 | 11.2 | 1.0 | 12.5 | | C _L = 50 pF | 2-7, 8 | |
| t _{PLZ} t _{PHZ} | TRI-STATE Output Disable Time | 5.0 ± 0.5 | 7.0 | 11.2 | 1.0 | 12.0 | ns | R _L = 1 kΩ | C _L = 50 pF | 2-7, 8 |
| | | | | | | | | | | |
| t _{OSLH} t _{OSHL} | Output to Output Skew | 5.0 ± 0.5 | 1.0 | | 1.0 | | | (Note 1) | | |
| f _{MAX} | Maximum Clock Frequency | 5.0 ± 0.5 | 90 | 140 | 80 | | MHz | C _L = 15 pF | | |
| | | | 85 | 130 | 75 | | | C _L = 50 pF | | |
| C _{IN} | Input Capacitance | | 4 | 10 | 10 | | pF | V _{CC} = Open | | |

AC Electrical Characteristics for 'VHCT Family Devices (Continued)

| Symbol | Parameter | V _{CC} (V) | 74VHCT | | | Units | Conditions | Fig. No. |
|------------------|-------------------------------|------------------------|-----------------------|-----|-----|-------|------------------------|-------------|
| | | | T _A = 25°C | | | | | |
| | | | Min | Typ | Max | | | |
| C _{OUT} | Output Capacitance | | 9 | | | pF | V _{CC} = 5.0V | |
| C _{PD} | Power Dissipation Capacitance | | 27 | | | pF | (Note 2) | |

Note 1: Parameter guaranteed by design. $t_{OSLH} = |t_{PLH\ max} - t_{PLH\ min}|$; $t_{OSHL} = |t_{PHL\ max} - t_{PHL\ min}|$

Note 2: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC\ (opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8$ (per F/F).

AC Operating Requirements for 'VHCT Family Devices: See Section 2 for Waveforms

| Symbol | Parameter | V _{CC} (V) | 74VHCT | | | 74VHCT | | Units | Conditions | Fig. No. |
|--|-----------------------------|------------------------|-----------------------|-----|-----|------------------------------------|-----|-------|------------|-------------|
| | | | T _A = 25°C | | | T _A = -40°C to +85°C | | | | |
| | | | Min | Typ | Max | Min | Max | | | |
| t _{W(H)} t _{W(L)} | Minimum Pulse Width (CP) | 5.0 ± 0.5 | 6.5 | | | 6.5 | | ns | | 2-6 |
| t _S | Minimum Set-up Time | 5.0 ± 0.5 | 2.5 | | | 2.5 | | ns | | 2-9 |
| t _H | Minimum Hold Time | 5.0 ± 0.5 | 2.5 | | | 2.5 | | | | |