

9316/DM9316 Synchronous 4-Bit Counters

General Description

These synchronous, presettable counters feature an internal carry look-ahead for application in high-speed counting designs. The 9316 is a 4-bit binary counter. The carry output is decoded by means of a NOR gate, thus preventing spikes during the normal counting mode of operation. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enables inputs and internal gating. This mode of operating eliminates the output counting spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock input waveform.

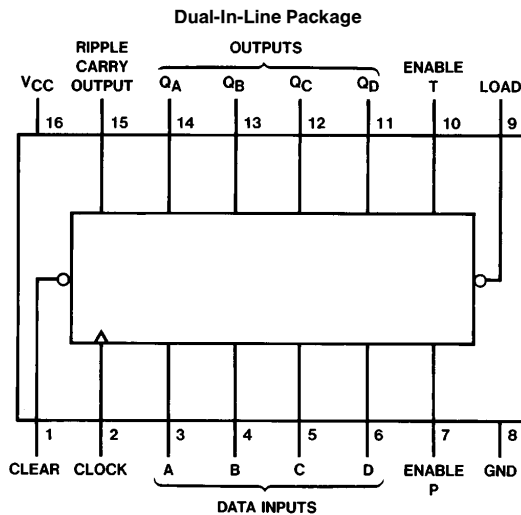
These counters are fully programmable; that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable input. Low-to-high transitions at the load input are perfectly acceptable regardless of the logic levels on the clock or enable inputs. The clear function is asynchronous and a low level at the clear input sets of the flip-flop outputs low regardless of the levels of clock, load, or enable inputs.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a ripple carry output. Both count-enable inputs (P and T) must be high to count, and input T is fed-forward to enable the ripple carry output. The ripple carry output thus enabled will produce a high-level output pulse with a duration approximately equal to the high-level portion of the Q_A output. This high-level overflow ripple carry pulse can be used to enable successive cascaded stages. High-to-low level transitions at the enable P or T inputs may occur regardless of the logic level in the clock.

Features

- Internal look-ahead for fast counting
- Carry output for n-bit cascading
- Synchronous counting
- Load control line
- Diode-clamped inputs
- Typical clock frequency 35 MHz
- Pin-for-pin replacements popular 54/74 counters 5416A/7416A (binary)
- Alternate Military/Aerospace device (9316) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

Connection Diagram



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Order Number 9316DMQB, 9316FMQB, DM9316J
 DM9316W or DM9316N
 See NS Package Number J16A, N16E or W16A

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
Military	–55°C to +125°C
Commercial	0°C to +70°C
Storage Temperature Range	–65°C to +150°C

Note: The “Absolute Maximum Ratings” are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the “Electrical Characteristics” table are not guaranteed at the absolute maximum ratings. The “Recommended Operating Conditions” table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	Military			Commercial			Units
		Min	Nom	Max	Min	Nom	Max	
V _{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH}	High Level Input Voltage	2			2			V
V _{IL}	Low Level Input Voltage			0.8			0.8	V
I _{OH}	High Level Output Current			–0.8			–0.8	mA
I _{OL}	Low Level Output Current			16			16	mA
f _{CLK}	Clock Frequency (Note 6)	0		25	0		25	MHz
t _w	Pulse Width (Note 6)	Clock	25		25			ns
		Clear	20		20			
t _{SU}	Setup Time (Note 6)	Data	20		20			ns
		Enable P	20		20			
		Load	25		25			
		Clear	20		20			
t _H	Any Hold Time (Notes 1 & 6)	0			0			ns
T _A	Free Air Operating Temperature	–55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
V _I	Input Clamp Voltage	V _{CC} = Min, I _I = –12 mA			–1.5	V
V _{OH}	High Level Output Voltage	V _{CC} = Min, I _{OH} = Max V _{IL} = Max, V _{IH} = Min	2.4	3.4		V
V _{OL}	Low Level Output Voltage	V _{CC} = Min, I _{OL} = Max V _{IH} = Min, V _{IL} = Max		0.2	0.4	V
I _I	Input Current @ Max Input Voltage	V _{CC} = Max, V _I = 5.5V			1	mA
I _{IH}	High Level Input Current	V _{CC} = Max V _I = 2.4 V	Clock		80	μA
			Enable T		80	
			Other		40	
I _{IL}	Low Level Input Current	V _{CC} = Max V _I = 0.4V	Clock		–3.2	μA
			Enable T		–3.2	
			Other		–1.6	
I _{OS}	Short Circuit Output Current	V _{CC} = Max (Note 3)	MIL	–20	–57	mA
			COM	–18	–57	
I _{CCH}	Supply Current with Outputs High	V _{CC} = Max (Note 4)	MIL	59	85	mA
			COM	59	94	
I _{CCL}	Supply Current with Outputs Low	V _{CC} = Max (Note 5)	MIL	63	91	mA
			COM	63	101	

Note 1: The minimum HOLD time is as specified or as long as the CLOCK input takes to rise from 0.8V to 2V, whichever is longer.

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 3: Not more than one output should be shorted at a time.

Note 4: I_{CCH} is measured with the LOAD input high, then again with the LOAD input low, with all other inputs high and all outputs open.

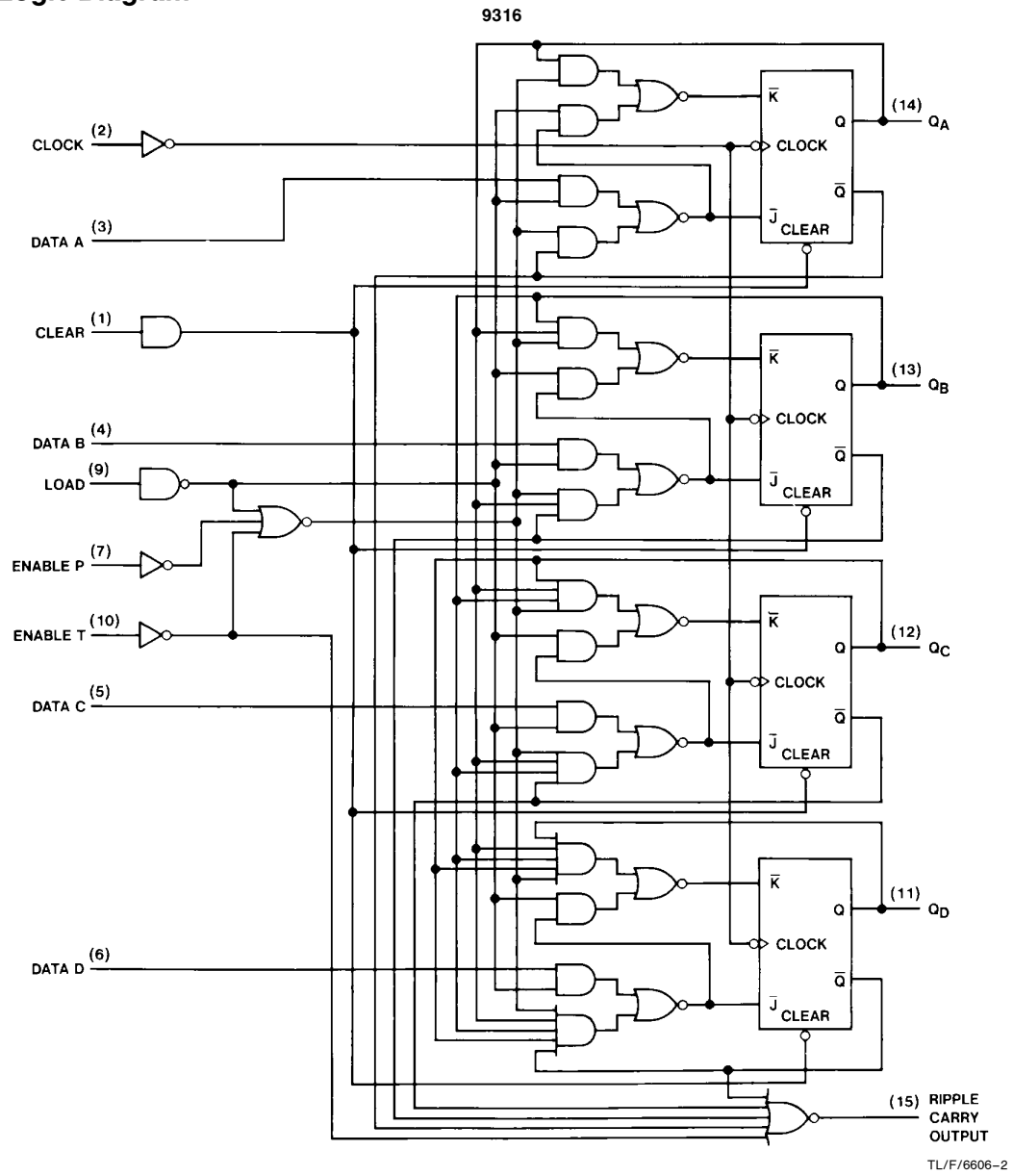
Note 5: I_{CCL} is measured with the CLOCK input high, then again with the CLOCK input low, with all other inputs low and all outputs open.

Note 6: T_A = 25°C and V_{CC} = 5V.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25^\circ C$ (See Section 1 for Test Waveforms and Output Load)

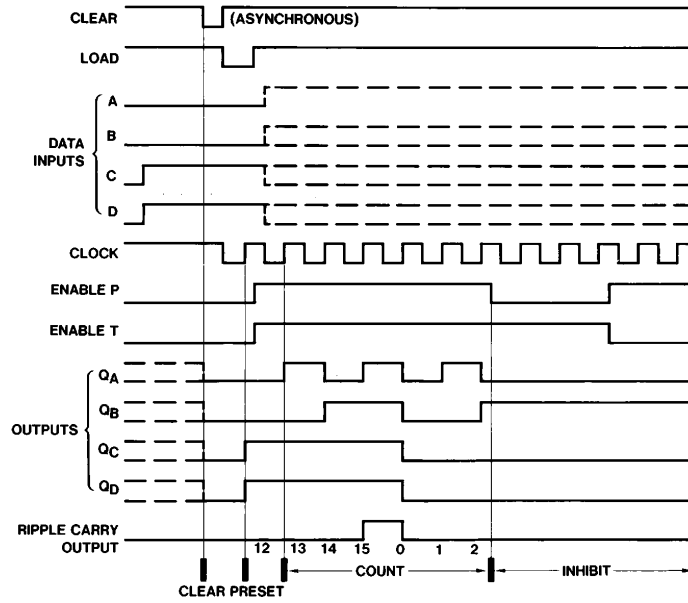
Symbol	Parameter	From (Input) To (Output)	$R_L = 400\Omega, C_L = 15\text{ pF}$		Units
			Min	Max	
f_{MAX}	Maximum Clock Frequency		25		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to RC		27	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to RC		24	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Q		20	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Q		23	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Q		21	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Q		25	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	ENT to RC		15	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	ENT to RC		16	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Q		36	ns

Logic Diagram



Timing Diagram

9316 Synchronous Binary Counters Typical Clear, Preset, Count and Inhibit Sequences

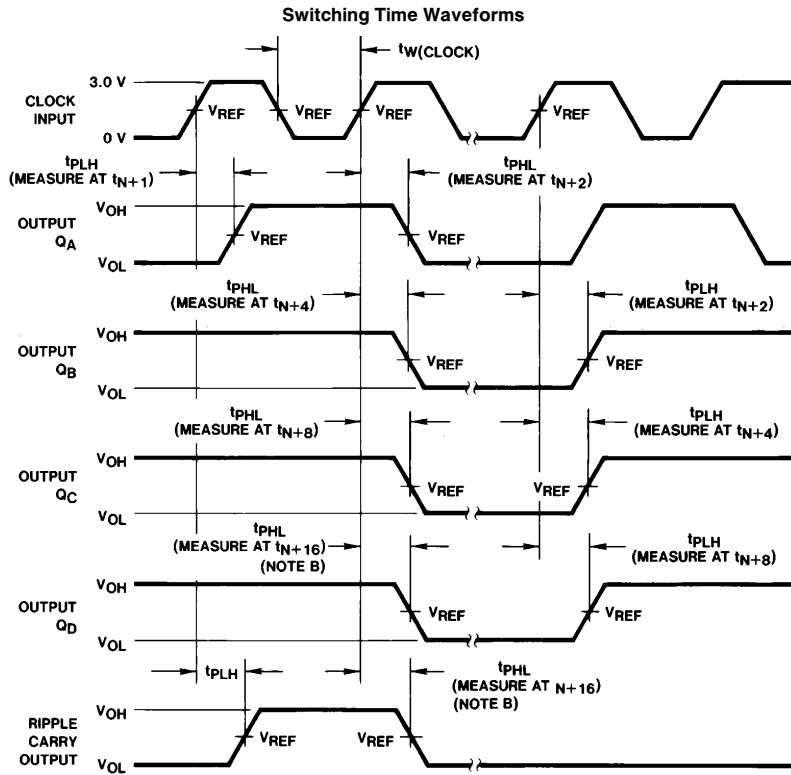


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Sequence:

- (1) Clear outputs to zero.
- (2) Preset to binary twelve.
- (3) Count to thirteen, fourteen, fifteen, zero, one, and two.
- (4) Inhibit

Parameter Measurement Information



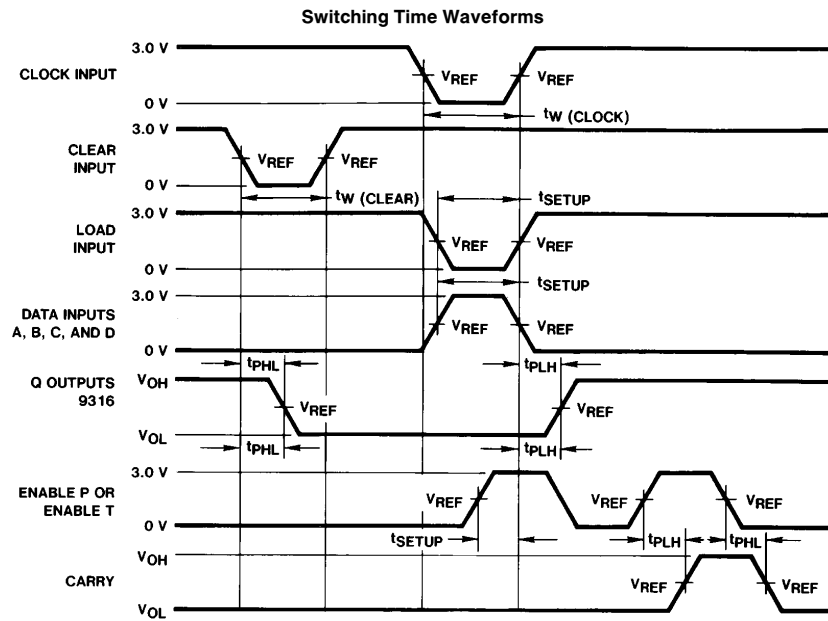
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Note A: The input pulses are supplied by a generator having the following characteristics: $\text{PRR} \leq 1 \text{ MHz}$, duty cycle $\leq 50\%$, $Z_{\text{OUT}} \approx 50 \Omega$, $t_r \leq 10 \text{ ns}$, $t_f \leq 10 \text{ ns}$. Vary PRR to measure t_{MAX} .

Note B: Outputs Q_D and carry are tested at t_{n+16} for 9316/8316, where t_n is the bit time when all outputs are low.

Note C: $V_{\text{REF}} = 1.5\text{V}$.

Parameter Measurement Information (Continued)



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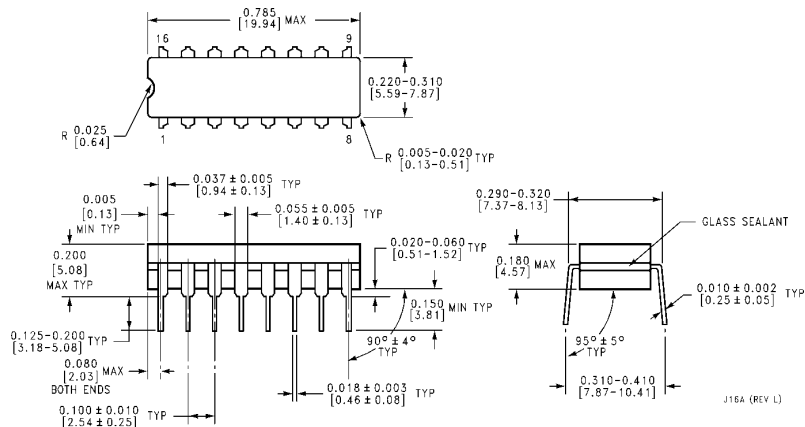
Note A: The input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, duty cycle $\leq 50\%$, $Z_{OUT} \approx 50\Omega$, $t_r \leq 10$ ns, $t_f \leq 10$ ns.

Note B: Enable P and Enable T setup times are measured at $t_n + 16$ for 8316/9316.

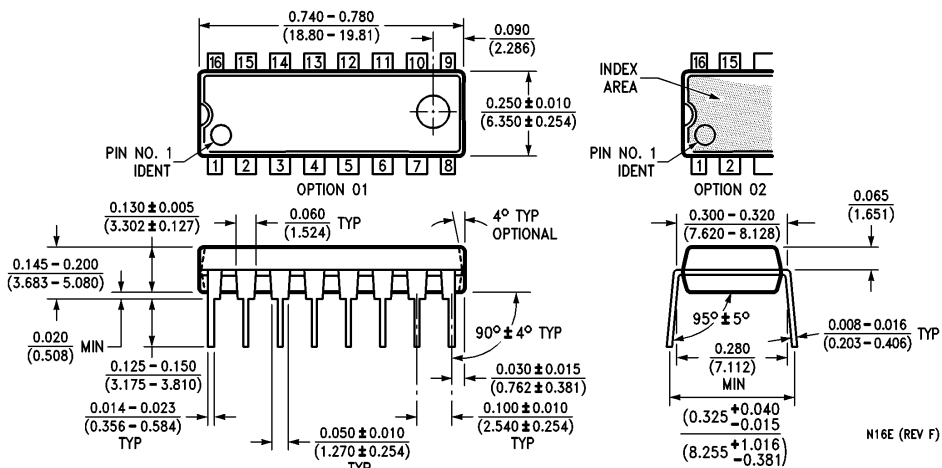
Note C: $V_{REF} = 1.5V$.



Physical Dimensions inches (millimeters)

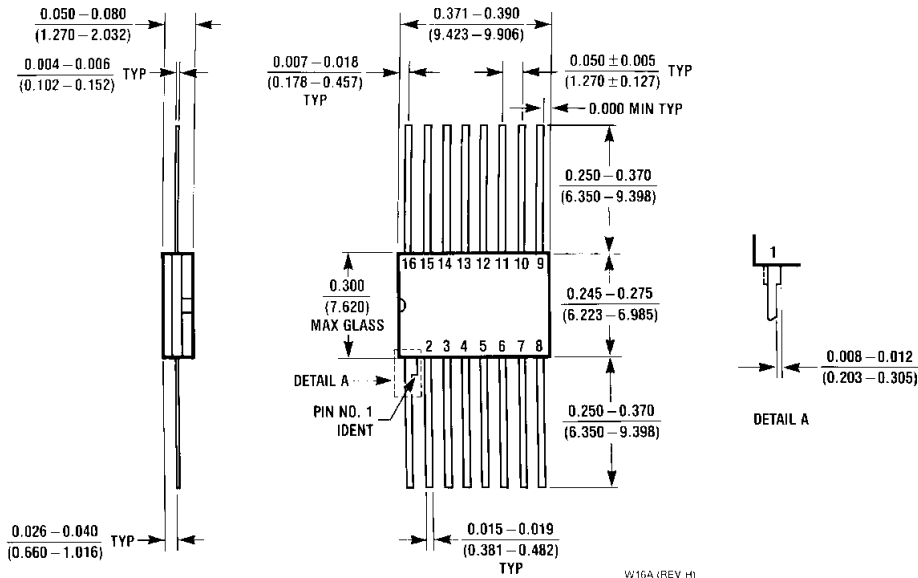


16-Lead Ceramic Dual-In-Line Package (J)
Order Number 9316DMQB or DM9316J
NS Package Number J16A



16-Lead Molded Dual-In-Line Package (N)
Order Number DM9316N
NS Package Number N16E

Physical Dimensions inches (millimeters) (Continued)



16-Lead Ceramic Flat Package (W)
Order Number 9316FMQB or DM9316W
NS Package Number W16A

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