TS63210K – 1.4Ω On Resistance GaN Broadband RF Switch SP2T

1.0 Features

- Ultra low 1.4Ω on resistance
- 0.40pF C_{off}
- RF peak voltage handling of 100V
- Each state can be controlled independently
- 4 independent state configuration
- No external DC blocking capacitors on RF lines
- Versatile 2.6~5.5V power supply
- 1.2~5.0V digital control

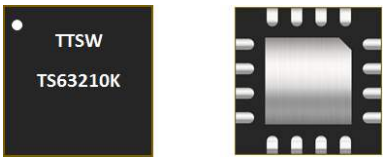


Figure 1 Device Image
(16 Pin 3×3×0.8mm QFN Package)

2.0 Applications

- Filter and antenna tuning
- Dynamic matching
- Private mobile radio handsets
- Public safety handsets
- Cellular infrastructure
- Satellite terminals

RoHS/REACH/Halogen Free Compliance

3.0 Description

The TS63210K is a reflective open Single Pole Two Throw (SP2T) switch designed for antenna or filter tuning applications where high RF peak voltage handling is desired. TS63210K is suitable for frequency range from 1MHz to 1GHz. The TS63210K has a very low 1.4Ω on resistance and off capacitance of 0.4pF. This switch can select up to 4 independent states.

The TS63210K is packaged in a compact Quad Flat No lead (QFN) 3x3mm 16 leads plastic package.

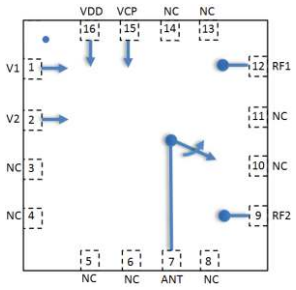


Figure 2 Function Block Diagram
(Top View)

4.0 Ordering Information

Table 1 Ordering Information

Base Part Number	Package Type	Form	Qty	Reel Diameter	Reel Width	Orderable Part Number
TS63210K	16 Pin 3×3×0.8mm QFN	Tape and Reel	3000	13” (330mm)	18mm	TS63210KMTRPBF
Evaluation Board						TS63210K-EVB

5.0 Pin Description

Table 2 Pin Definition

Pin Number	Pin Name	Description
1	V1	Switch control input 1
2	V2	Switch control input 2
3,4,5,6,8,10,11,13,14	NC	No internal connection, can be grounded
7	ANT	Antenna port
9	RF2	RF port 2
12	RF1	RF port 1
15	VCP	Internal charge pump voltage output. Connect a 1nF capacitor to GND on this pin to improve switching time.
16	VDD	DC power supply

Note: The backside ground (thermal) pad of the package must be grounded directly to the ground plane of PCB with multiple vias to ensure proper operation and thermal management.

6.0 Absolute Maximum Ratings

Table 3 Absolute Maximum Ratings @T_A=+25°C Unless Otherwise Specified

Parameter	Symbol	Value	Unit
Electrical Ratings			
Power Supply Voltage	VDD	2.6 to 5.5	V
Storage Temperature Range	T_{st}	-55 to +125	°C
Operating Temperature Range	T_{op}	-40 to +85	°C
Maximum Junction Temperature	T_J	+140	°C
RF Input Power CW, 800MHz	RFx	42	dBm
Thermal Ratings			
Thermal Resistance (junction-to-case) – Bottom side	$R_{\theta JC}$	15	°C/W
Thermal Resistance (junction-to-top)	$R_{\theta JT}$	≤ 39	°C/W
Soldering Temperature	T_{SOLD}	260	°C
ESD Ratings			
Human Body Model (HBM)	Level 1B	500 to <1000	V
Charged Device Model (CDM)	Level C3	≥1000	V
Moisture Rating			
Moisture Sensitivity Level	MSL	1	-

Attention:
Maximum ratings are absolute ratings. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Exceeding one or a combination of the absolute maximum ratings may cause permanent and irreversible damage to the device and/or to surrounding circuit.

7.0 Electrical Specifications

Table 4 Electrical Specifications @T_A=+25°C Unless Otherwise Specified; VDD=+2.7V; 50Ω Source/Load.

Parameter	Condition	Minimum	Typical	Maximum	Unit
Operating Frequency		1		1000	MHz
ON Resistance	On state, DC measurement		1.4		Ω
OFF Capacitance	Total capacitance of each OFF path		0.4		pF
RF Peak Voltage	Measured at 10MHz		100		V
Insertion Loss, RFx	100MHz		0.17		dB
	500MHz		0.26		
	1.0GHz		0.37		
Isolation ANT-RFx	100MHz		36		dB
	500MHz		23		
	1.0GHz		18		
Return Loss ANT-RFx	100MHz		30		dB
	500MHz		20		
	1.0GHz		15		
H2	800MHz, Pin=35dBm		82		dBc
H3	800MHz, Pin=35dBm		86		dBc
IIP3	800MHz		70		dBm
P0.1dB[1]	1~10MHz		40		dBm
	10~1000MHz		42		dBm
Switching Time	50% ctrl to 10/90% of the RF value is settled. C1=1nF to Gnd on VCP		TBD		μs
Start-up Time	50% ctrl to 10/90% of the RF value is settled. C1=1nF to Gnd on VCP		TBD		μs
Control Voltage	Power supply VDD	2.6	2.7	5.5	V
	All control pins high, V_{ih}	1.0	2.7	5.25	V
	All control pins low, V_{il}	-0.3		0.5	V
Control Current	All control pins low, I_{il}		0		μA
	All control pins high, I_{ih}			7.5	μA
Current Consumption, IDD	Active mode		160	200	μA

Note:

[1] P0.1dB is a figure of merit.

[2] No external DC blocking capacitors required on RF pins unless DC voltage is applied on a RF pin.

[3] Start-up time is the time from VDD ON to RF signal settled on a throw or transition time from low power mode to active mode.

8.0 Switch Truth Table

Table 5 Switch Truth Table

V1	V2	Active RF Path
0	0	All OFF state
0	1	ANT-RF2 ON
1	0	ANT-RF1 ON
1	1	All ON state

Attention:

[1] VDD should be applied first before V1 and V2, otherwise may cause damage to the device.

[2] There are internal pull-downs to ground on both V1 and V2 control pins, the state at start-up without any control voltage applied will be All OFF.

9.0 Evaluation Board/Model

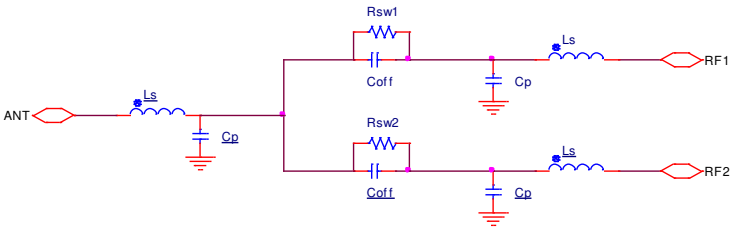


Figure 3 Schematic Model

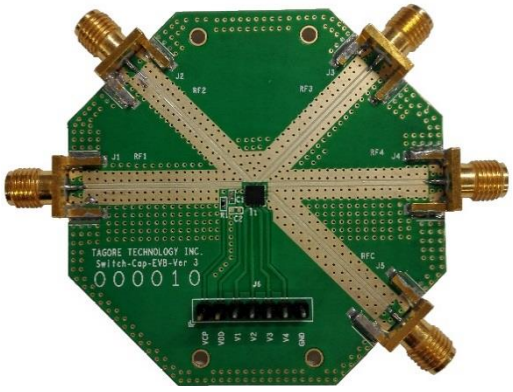


Figure 4 Evaluation Board Image

Table 6 Recommended Values

Component	Value	Unit
Cp	0.25	pF
Coff	0.40	pF
Rswx	1.4 if ON	Ω
	500K if OFF	Ω
Ls	0.4	nH

Note: Ron/Off is measured at DC. This model will not accurately predict losses in a tunable filter or antenna design

10.0 Typical Characteristics

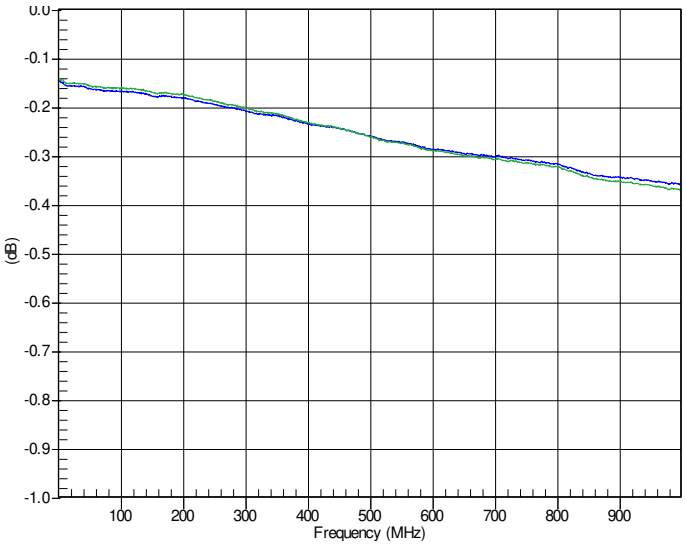


Figure 5 RF1, RF2 Insertion Loss

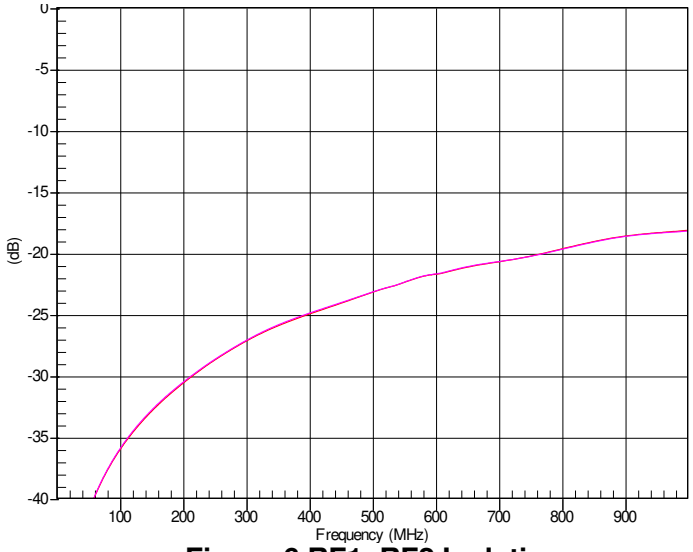


Figure 6 RF1, RF2 Isolation

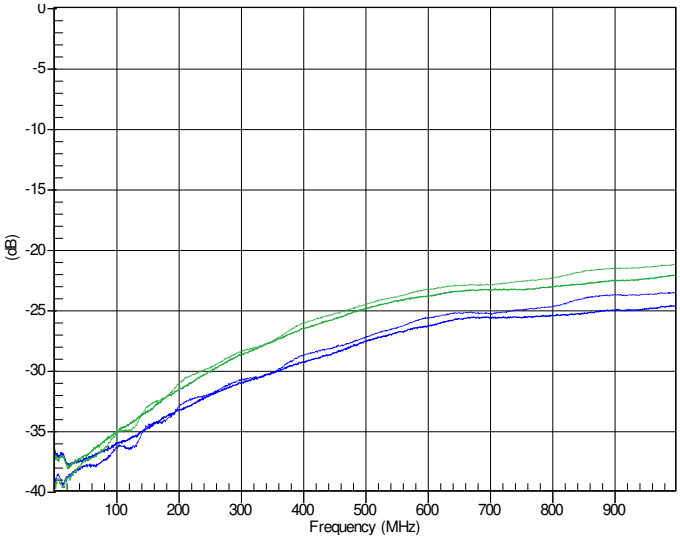


Figure 7 Return Loss

11.0 Device Package Information

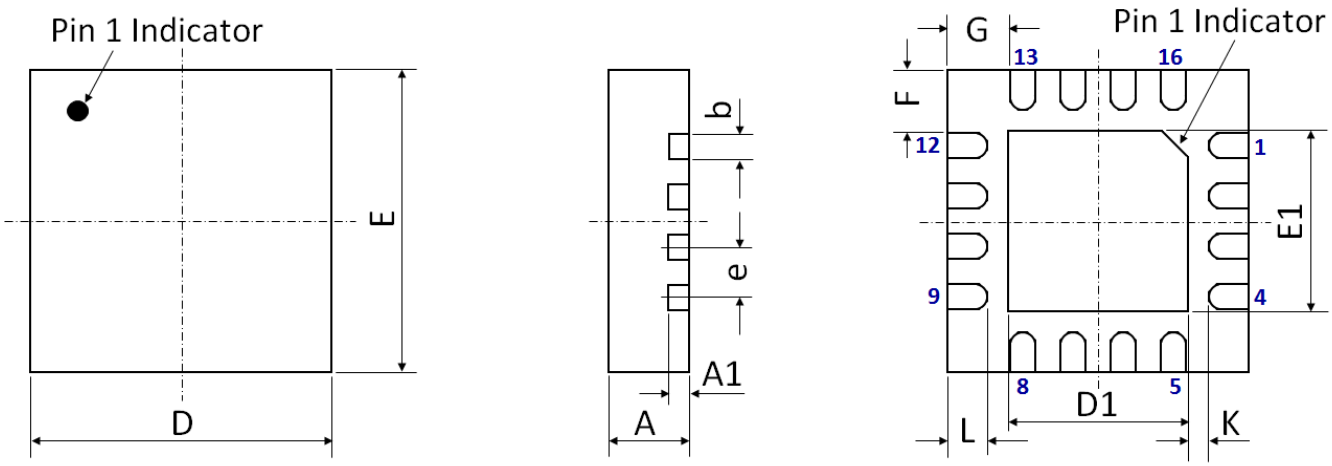


Figure 8 Device Package Drawing
(All dimensions are in mm)

Table 7 Device Package Dimensions

Dimension (mm)	**Value** (mm)	**Tolerance** (mm)	**Dimension** (mm)	**Value** (mm)	**Tolerance** (mm)
A	0.80	±0.05	E	3.00 BSC	±0.05
A1	0.203	±0.02	E1	1.70	±0.05
b	0.25	+0.05/-0.07	F	0.625	±0.05
D	3.00 BSC	±0.05	G	0.625	±0.05
D1	1.70	±0.05	L	0.25	±0.05
e	0.50 BSC	±0.05	K	0.40	±0.05

Note: Lead finish: Pure Sn without underlayer; Thickness: 7.5μm ~ 20μm (Typical 10μm ~ 12μm)

Attention:
Please refer to application notes *TN-001* and *TN-002* at http://www.tagoretech.com for PCB and soldering related guidelines.

12.0 PCB Land Design

Guidelines:
[1] 4 layer PCB is recommended.
[2] Via diameter is recommended to be 0.2mm to prevent solder wicking inside the vias.
[3] Thermal vias shall only be placed on the center pad.
[4] The maximum via number for the center pad is 3(X)×3(Y)=9.

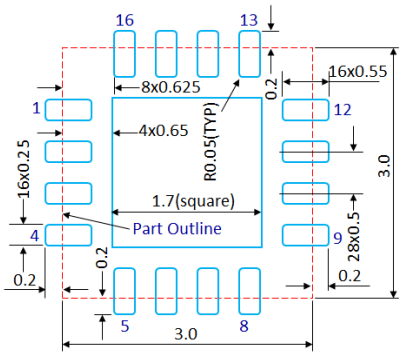
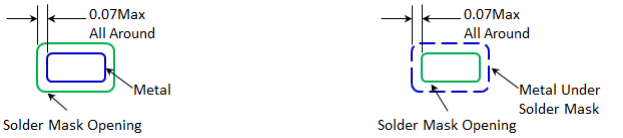


Figure 9 PCB Land Pattern
(Dimensions are in mm)



Non-Solder Mask Defined (Preferred)

Solder Mask Defined

Figure 10 Solder Mask Pattern
(Dimensions are in mm)

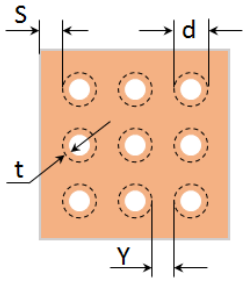


Figure 11 Thermal Via Pattern
(Recommended Values: S≥0.15mm; Y≥0.20mm; d=0.2mm; Plating Thickness t=25μm or 50μm)

13.0 PCB Stencil Design

Guidelines:

[1] Laser-cut, stainless steel stencil is recommended with electro-polished trapezoidal walls to improve the paste release.

[2] Stencil thickness is recommended to be 125μm.

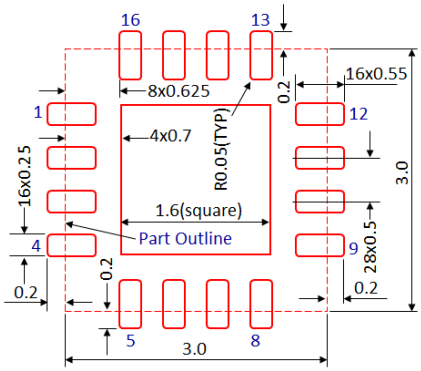


Figure 12 Stencil Openings
(Dimensions are in mm)

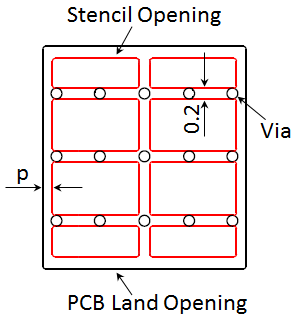


Figure 13 Stencil Openings Shall not Cover Via Areas If Possible
(Dimensions are in mm)

14.0 Tape and Reel Information

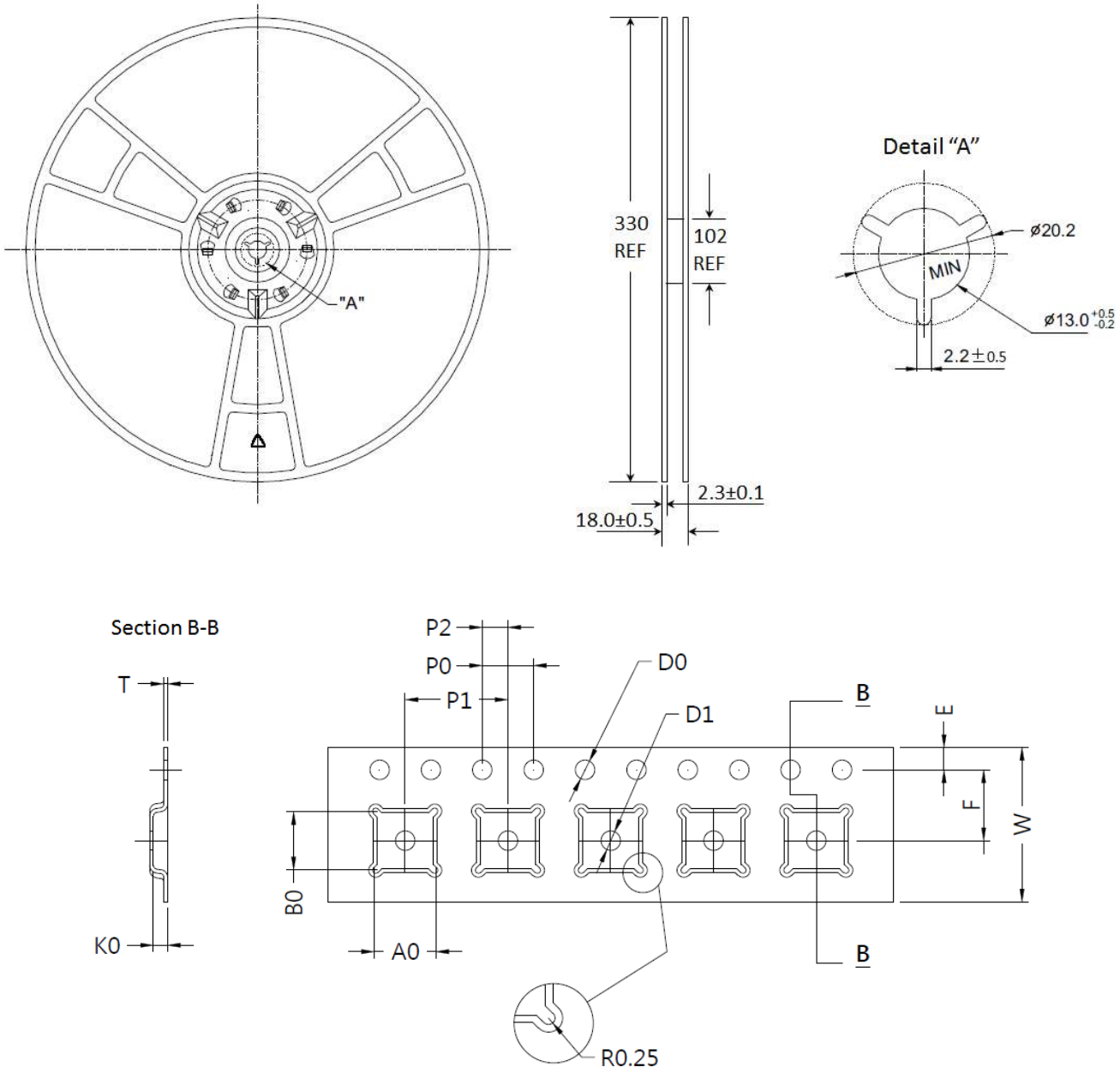


Figure 14 Tape and Reel Drawing

Table 8 Tape and Reel Dimensions

Dimension (mm)	**Value** (mm)	**Tolerance** (mm)	**Dimension** (mm)	**Value** (mm)	**Tolerance** (mm)
A0	3.35	±0.10	K0	1.10	±0.10
B0	3.35	±0.10	P0	4.00	±0.10
D0	1.50	+0.10/-0.00	P1	8.00	±0.10
D1	1.50	+0.10/-0.00	P2	2.00	±0.05
E	1.75	±0.10	T	0.30	±0.05
F	5.50	±0.05	W	12.00	±0.30

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