

Features

- Precision synthesizer generates any clock-rate from 1 Hz to 177.5 MHz with jitter below 1ps
- Programmable digital PLL synchronize to any clock rate from 1 Hz (1 pps) to 750 MHz
- Input reference configurable as single ended LVCMOS (up to 177.5 MHz) or differential LVPECL (up to 750 MHz)
- Flexible two-stage architecture translates between arbitrary data rates, line coding rates and FEC rates
- Programmable Digital PLL loop filter: 30 MHz, 14 Hz, 28 Hz, 56 Hz, 112 Hz, 224 Hz, 448 Hz or 896 Hz
- Two LVCMOS outputs —from 1 Hz (1 pps) to 177.5 MHz

Ordering Information

ZL30159GGG2 64 Pin LPGA* Trays
 *Pb Free Tin/Silver/Copper
-40°C to +85°C

- Operates from a single crystal resonator or clock oscillator
- Configurable via SPI/I2C interface

Applications

- General purpose clock rate translator
- GPS receiver clock synthesizer

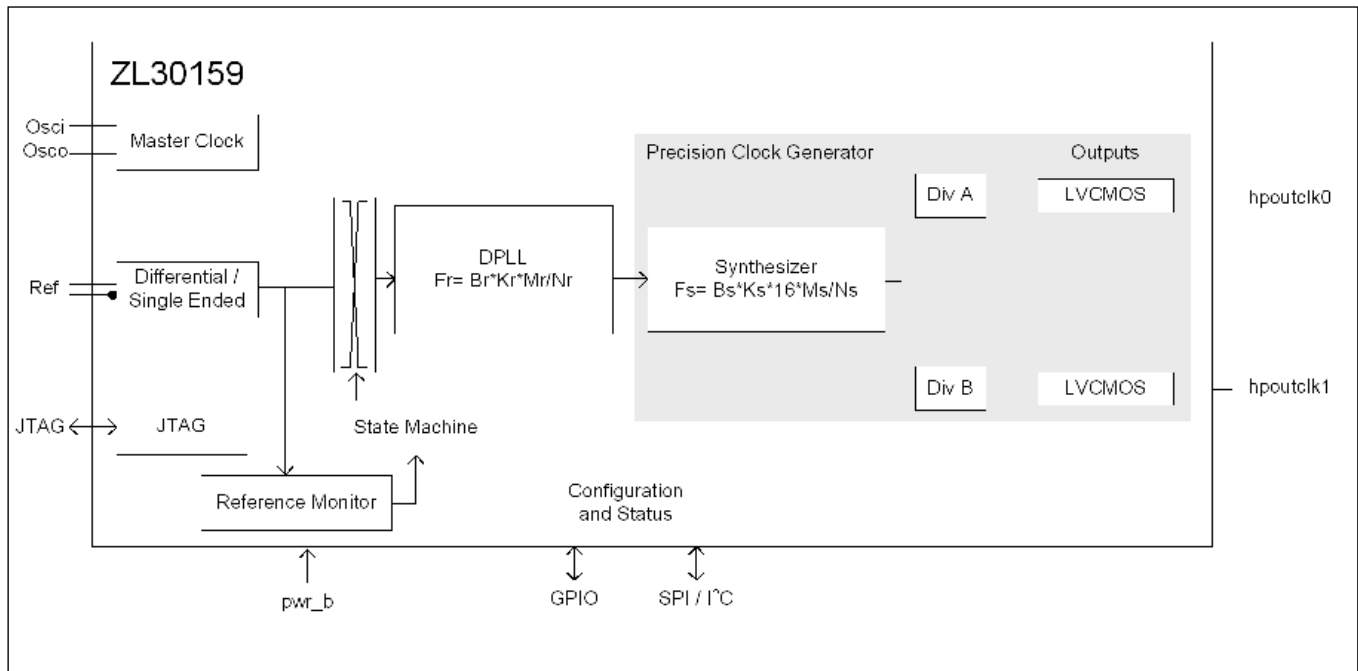
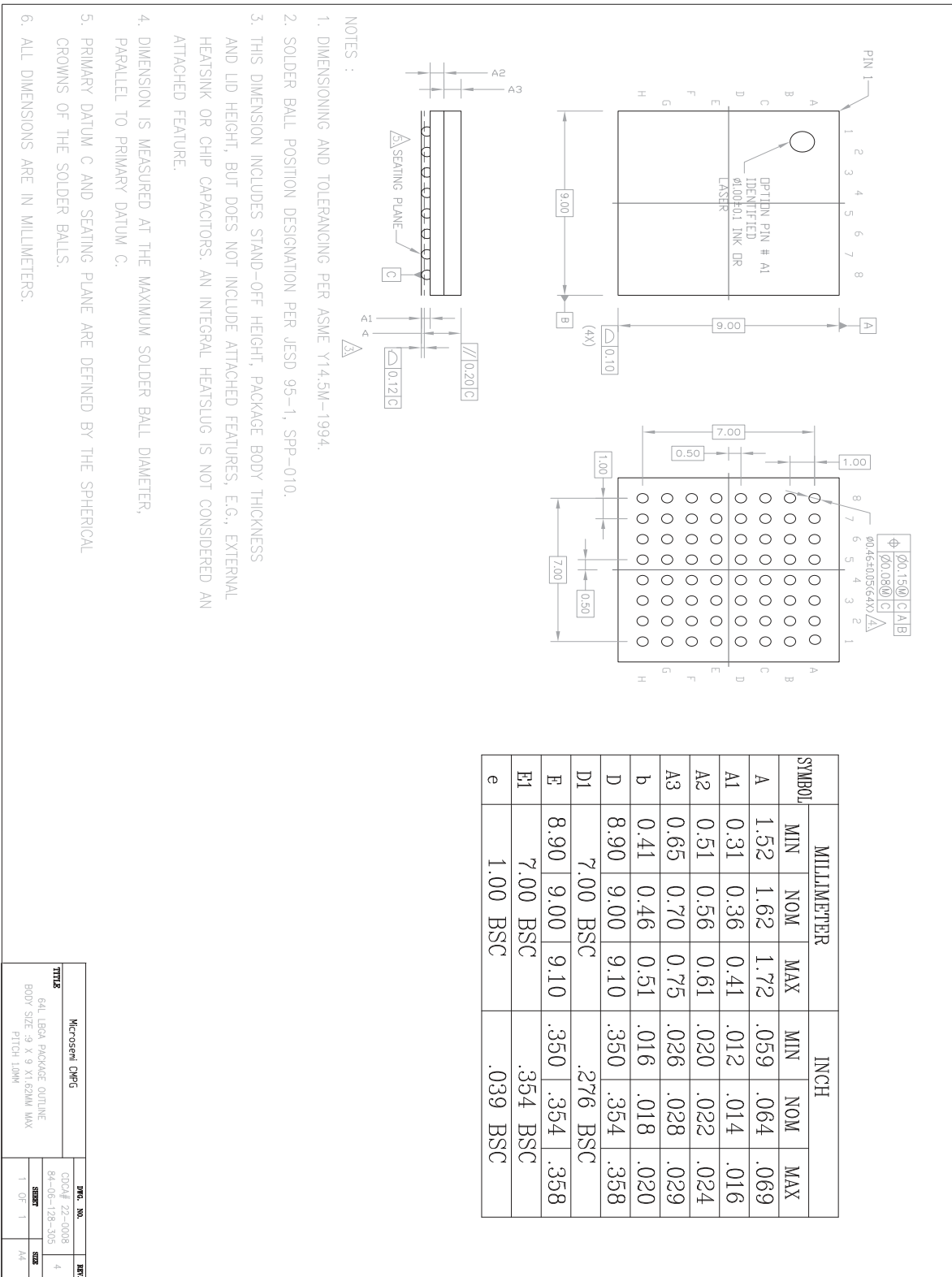


Figure 1 - Functional Block Diagram

Mechanical Drawing



- NOTES :
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
 2. SOLDER BALL POSITION DESIGNATION PER JESD 95-1, SPP-010.
 3. THIS DIMENSION INCLUDES STAND-OFF HEIGHT, PACKAGE BODY THICKNESS AND LID HEIGHT, BUT DOES NOT INCLUDE ATTACHED FEATURES, E.G., EXTERNAL HEATSINK OR CHIP CAPACITORS. AN INTEGRAL HEATSLUG IS NOT CONSIDERED AN ATTACHED FEATURE.
 4. DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
 5. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
 6. ALL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.52	1.62	1.72	.059	.064	.069
A1	0.31	0.36	0.41	.012	.014	.016
A2	0.51	0.56	0.61	.020	.022	.024
A3	0.65	0.70	0.75	.026	.028	.029
b	0.41	0.46	0.51	.016	.018	.020
D	8.90	9.00	9.10	.350	.354	.358
D1	7.00 BSC			.276 BSC		
E	8.90	9.00	9.10	.350	.354	.358
E1	7.00 BSC			.354 BSC		
e	1.00 BSC			.039 BSC		

Microsemi Chip		DWG. NO.		REV.	
TTTT8		CDA# 22-0008		4	
64L LEGA PACKAGE OUTLINE		84-06-128-305		SIZE	
BODY SIZE : 9 X 9 X1.62MM MAX		PITCH 1.0MM		REV.	

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