# **RF Power GaN Transistor**

This 56 W symmetrical Doherty RF power GaN transistor is designed for cellular base station applications requiring very wide instantaneous bandwidth capability covering the frequency range of 1805 to 2200 MHz.

This part is characterized and performance is guaranteed for applications operating in the 1805 to 2200 MHz band. There is no guarantee of performance when this part is used in applications designed outside of these frequencies.

# 2000 MHz

• Typical Doherty Single-Carrier W-CDMA Performance:  $V_{DD}$  = 48 Vdc,  $I_{DQA}$  = 250 mA,  $V_{GSB}$  = -5.0 Vdc,  $P_{out}$  = 56 W Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.

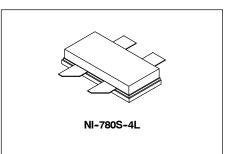
Frequency	G <sub>ps</sub> (dB)	η <sub>D</sub> (%)	Output PAR (dB)	ACPR (dBc)
1805 MHz	16.0	54.3	8.0	-26.4
1995 MHz	16.8	52.2	7.8	-31.9
2170 MHz	15.4	53.9	7.6	-33.8

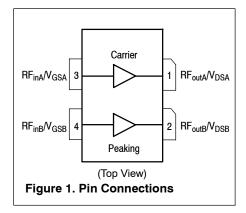
### Features

- · High terminal impedances for optimal broadband performance
- Advanced high performance in-package Doherty
- Improved linearized error vector magnitude with next generation signal
- Able to withstand extremely high output VSWR and broadband operating conditions

# A3G18D510-04S

1805–2200 MHz, 56 W Avg., 48 V AIRFAST RF POWER GaN TRANSISTOR







#### Table 1. Maximum Ratings

Rating	Symbol	Va	lue	Unit	
Drain-Source Voltage	V <sub>DSS</sub>	125		Vdc	
Gate-Source Voltage	V <sub>GS</sub>	8, 0		Vdc	
Operating Voltage		V <sub>DD</sub>	0 to	+55	Vdc
Maximum Forward Gate Current, $I_{G (A+B)}$ , @ $T_{C} = 25^{\circ}C$		I <sub>GMAX</sub>	2	25	mA
Storage Temperature Range		T <sub>stg</sub>	-65 te	o +150	°C
Case Operating Temperature Range		T <sub>C</sub>	-55 te	o +150	°C
Operating Active Die Surface Temperature Range		TJ	-55 te	o +225	°C
Maximum Channel Temperature (1)		T <sub>CH</sub>	2	75	°C
Table 2. Thermal Characteristics		1 1			
Characteristic		Symbol	Va	lue	Unit
Thermal Resistance by Infrared Measurement, Active Die Surface-to-Cas Case Temperature 72°C, $P_D = 68 \text{ W}$	е	R <sub>θJC</sub> (IR)	0.8	3 (2)	°C/W
Thermal Resistance by Finite Element Analysis, Channel-to-Case Case Temperature 72°C, $P_D = 68 \text{ W}$		R <sub>θCHC</sub> (FEA)	1.1 (3) °C		°C/W
Table 3. ESD Protection Characteristics					
Test Methodology			Cla	ass	
Human Body Model (per JS-001-2017)	1B				
Charge Device Model (per JS-002-2014)	IV				
Table 4. Electrical Characteristics ( $T_A = 25^{\circ}C$ unless otherwise noted)	1				
Characteristic	Symbol	Min	Тур	Max	Unit
Off Characteristics <sup>(4)</sup>					
Off-State Drain Leakage	I <sub>D(BR)</sub>				
		—	_	24.3 24.3	mAdc mAdc
				24.0	IIIAde
Dn Characteristics — Side A, Carrier Gate Threshold Voltage	Veen	-3.8	-3.0	-2.3	Vdc
$(V_{DS} = 10 \text{ Vdc}, I_D = 24.3 \text{ mAdc})$	V <sub>GS(th)</sub>	-3.6	-3.0	-2.5	vuc
Gate Quiescent Voltage $(V_{DD} = 48 \text{ Vdc}, I_D = 250 \text{ mAdc}, \text{Measured in Functional Test})$	V <sub>GSA(Q)</sub>	-3.7	-3.2	-2.7	Vdc
Gate-Source Leakage Current (V <sub>DS</sub> = 150 Vdc, V <sub>GS</sub> = -8 Vdc)	-12.2	_	_	mAdc	
Dn Characteristics — Side B, Peaking	•	. 1			•
Gate Threshold Voltage $(V_{DS} = 10 \text{ Vdc}, I_D = 24.3 \text{ mAdc})$	V <sub>GS(th)</sub>	-3.8	-3.3	-2.3	Vdc
Gate-Source Leakage Current (V <sub>DS</sub> = 150 Vdc, V <sub>GS</sub> = -8 Vdc)	I <sub>GSS</sub>	-12.2	—	—	mAdc

1. Reliability tests were conducted at 225°C. Operations with  $T_{CH}$  at 275°C will reduce median time to failure.

Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to <u>http://www.nxp.com/RF</u> and search for AN1955.
R<sub>θCHC</sub> (FEA) must be used for purposes related to reliability and limitations on maximum channel temperature. MTTF may be estimated by the expression MTTF (hours) = 10<sup>[A + B/(T + 273)]</sup>, where *T* is the channel temperature in degrees Celsius, *A* = -10.3 and *B* = 8263.

4. Each side of device measured separately.

(continued)

#### Table 4. Electrical Characteristics (T<sub>A</sub> = 25°C unless otherwise noted) (continued)

Characteristic	Symbol	Min	Тур	Max	Unit

**Functional Tests** <sup>(1,2)</sup> (In NXP Doherty Production Test Fixture, 50 ohm system)  $V_{DD} = 48$  Vdc,  $I_{DQA} = 250$  mA,  $V_{GSB} = -5.0$  Vdc,  $P_{out} = 56$  W Avg., f = 1805 MHz, Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @  $\pm 5$  MHz Offset. **[See note on correct biasing sequence.]** 

		0			
Power Gain	G <sub>ps</sub>	15.0	16.0	18.0	dB
Drain Efficiency	η <sub>D</sub>	44.3	54.3	—	%
Pout @ 3 dB Compression Point, CW	P3dB	53.6	55.1	—	dBm
Adjacent Channel Power Ratio	ACPR	_	-26.4	-21.9	dBc

Wideband Ruggedness (In NXP Doherty Production Test Fixture, 50 ohm system)  $I_{DQA}$  = 250 mA,  $V_{GSB}$  = -5.0 Vdc, f = 1995 MHz, Additive White Gaussian Noise (AWGN) with 10 dB PAR

ISBW of 400 MHz at 55 Vdc, 228 W Avg. Modulated Output Power	No Device Degradation
(8.5 dB Input Overdrive from 228 W Avg. Modulated Output Power)	

**Typical Performance** (In NXP Doherty Production Test Fixture, 50 ohm system)  $V_{DD}$  = 48 Vdc,  $I_{DQA}$  = 250 mA,  $V_{GSB}$  = -5.0 Vdc, 1805–2170 MHz Bandwidth

Pout @ 3 dB Compression Point <sup>(2)</sup>	P3dB	_	355	_	W
AM/PM (Maximum value measured at the P3dB compression point across the 1805–2170 MHz bandwidth)	Φ	_	-25	_	o
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	VBW <sub>res</sub>	—	260	_	MHz
Gain Flatness in 365 MHz Bandwidth @ P <sub>out</sub> = 56 W Avg.	G <sub>F</sub>	—	1.7	_	dB
Gain Variation over Temperature (-40°C to +85°C)	ΔG	—	0.013	_	dB/°C
Output Power Variation over Temperature (-40°C to +85°C)	∆P1dB		0.013		dB/°C

#### **Table 5. Ordering Information**

Device	Tape and Reel Information	Package
A3G18D510-04SR3	R3 Suffix = 250 Units, 32 mm Tape Width, 13-inch Reel	NI-780S-4L

1. Part internally input matched.

2. P3dB = P<sub>avg</sub> + 7.0 dB where P<sub>avg</sub> is the average output power measured using an unclipped W-CDMA single-carrier input signal where output PAR is compressed to 7.0 dB @ 0.01% probability on CCDF.

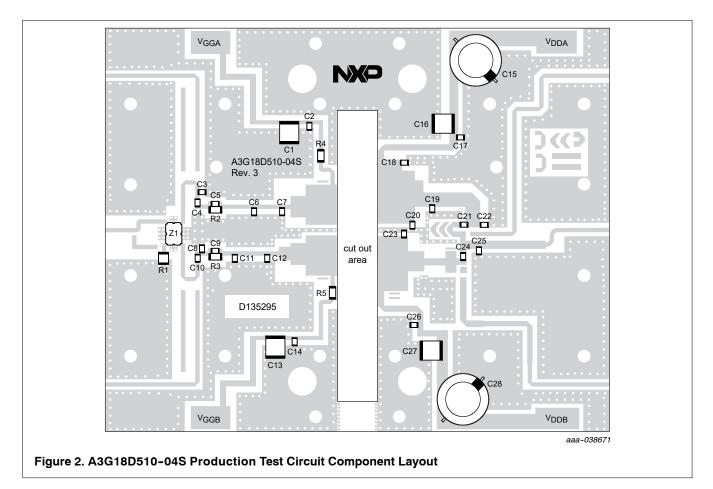
# NOTE: Correct Biasing Sequence for GaN Depletion Mode Transistors in a Doherty Configuration

#### **Bias ON the device**

- 1. Set gate voltage  $V_{GSA}$  and  $V_{GSB}$  to –5 V.
- 2. Set drain voltage V<sub>DSA</sub> and V<sub>DSB</sub> to nominal supply voltage (+48 V).
- 3. Increase V<sub>GSA</sub> (carrier side) until I<sub>DQA</sub> current is attained.
- 4. Increase V<sub>GSB</sub> (peaking side) to target bias voltage.
- 5. Apply RF input power to desired level.

#### **Bias OFF the device**

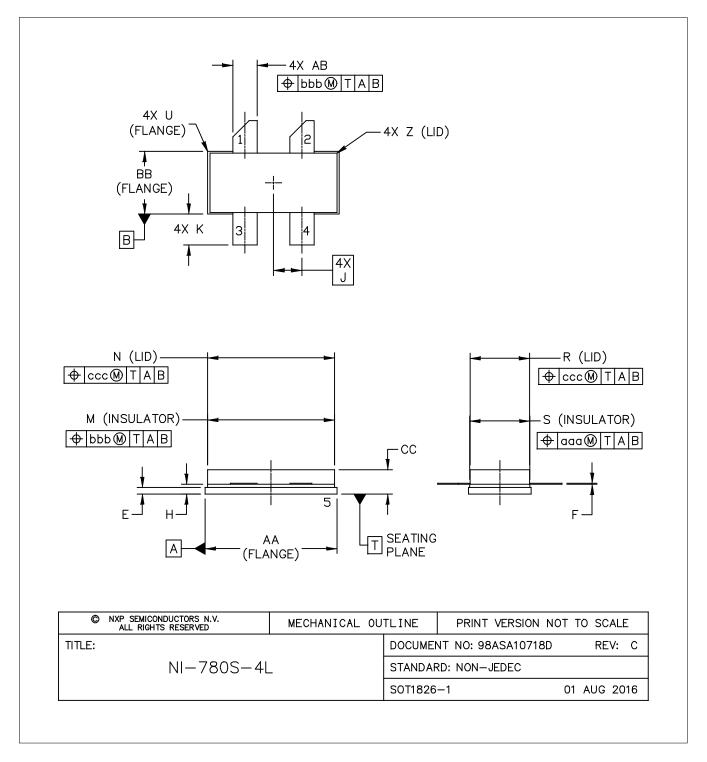
- 1. Disable RF input power.
- 2. Adjust gate voltage  $V_{GSA}$  and  $V_{GSB}$  to –5 V.
- Adjust drain voltage V<sub>DSA</sub> and V<sub>DSB</sub> to 0 V. Allow adequate time for drain voltage to reduce to 0 V from external drain capacitors.
- 4. Disable  $V_{GSA}$  and  $V_{GSB}$ .



# Table 6. A3G18D510-04S Production Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1, C13, C16, C27	10 μF Chip Capacitor	C5750X7S2A106M230KB	TDK
C2, C14, C17, C21, C24, C26	2, C14, C17, C21, C24, C26 15 pF Chip Capacitor		ATC
C3	0.4 pF Chip Capacitor	600F0R4BT250XT	ATC
C4, C5, C9, C10	11 pF Chip Capacitor	600F110JT250XT	ATC
C6	1.6 pF Chip Capacitor	600F1R6BT250XT	ATC
C7, C22	1 pF Chip Capacitor	600F1R0BT250XT	ATC
C8, C18	0.8 pF Chip Capacitor	600F0R8BT250XT	ATC
C11, C20	1.5 pF Chip Capacitor	600F1R5BT250XT	ATC
C12	2 pF Chip Capacitor	600F2R0BT250XT	ATC
C15, C28	220 μF, 100 V Electrolytic Capacitor	MCGPR100V227M16X26	Multicomp
C19, C23	1.2 pF Chip Capacitor	600F1R2BT250XT	ATC
C25	0.2 pF Chip Capacitor	600F0R2BT250XT	ATC
R1	50 Ω, 10 W Termination Chip Resistor	C10A50Z4	Anaren
R2	9.1 Ω, 1/4 W Chip Resistor	CRCW12069R10FKEA	Vishay
R3	7.5 Ω, 1/4 W Chip Resistor	CRCW12067R50FKEA	Vishay
R4	3.9 Ω, 1/4 W Chip Resistor	CRCW12063R90FKEA	Vishay
R5	4.3 Ω, 1/4 W Chip Resistor	CRCW12064R30FKEA	Vishay
Z1	1700–2000 MHz, 90°, 3 dB Hybrid Coupler	X3C19P1-03S	Anaren
PCB	RO4350B, 0.020″, ε <sub>r</sub> = 3.66	D135295	MTL

# **Package Information**



#### NOTES:

- 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1994.
- 2. CONTROLLING DIMENSION: INCH.
- 3. DELETED
- 4. DIMENSION H IS MEASURED .030 (0.762) AWAY FROM FLANGE TO CLEAR EPOXY FLOW OUT PARALLEL TO DATUM B.

	IN	INCH		MILLIMETER		INCH		MIL	LIME	TER
DIM	MIN	MAX	MIN	MAX	DIM	MIN	MAX	MIN		MAX
AA	.805	.815	20.45	20.70	U		.040			1.02
BB	.382	.388	9.70	9.86	Z		.030			0.76
cc	.125	.170	3.18	4.32	AB	. 145	. 155	3. 68	—	3. 94
E	.035	.045	0.89	1.14						
F	.003	.006	0.08	0.15	aaa		.005		0.12	7
н	.057	.067	1.45	1.70	bbb		.010		0.25	4
J	. 175	BSC	4.4	4 BSC	ccc		.015		0.38	1
к	.170	.210	4.32	5.33						
м	.774	.786	19.61	20.02						
N	.772	.788	19.61	20.02						
R	.365	.375	9.27	9.53						
S	.365	.375	9.27	9.52						
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# **PRODUCT DOCUMENTATION, SOFTWARE AND TOOLS**

Refer to the following resources to aid your design process.

# **Application Notes**

- AN1908: Solder Reflow Attach Method for High Power RF Devices in Air Cavity Packages
- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

## Software

.s2p File

# **Development Tools**

Printed Circuit Boards

### **REVISION HISTORY**

The following table summarizes revisions to this document.

Revision	Date	Description
0	Aug. 2020	Initial release of data sheet

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