SaRonix-eCera™

1.2V CMOS Low Jitter XO

FJ

2.5 x 2.0mm Ceramic SMD

Product Features

• 1 to 60 MHz Frequency Range

• <1 ps RMS jitter with fundamental or overtone design

• 1.2V CMOS compatible logic levels

• Designed for standard reflow and washing techniques

• Low power standby mode: 10 μA max

• Pb-free and RoHS/Green compliant

Product Description

The FJ Series crystal clock oscillators achieve superb jitter and stability over a broad range of operating conditions and frequencies.
The output clock signal, generated internally with a non-PLL oscillator design, is compatible with LVCMOS logic levels. The device, available on tape and reel, is contained in a 2.5 x 2.0mm surface-mount ceramic package.
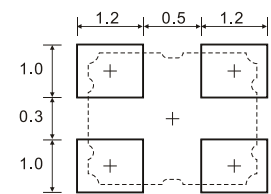
Applications

Ideal for compact, high-density applications:

• WLAN

• HBA

• Portable Multimedia Player (PMP)

• Notebook Computer

• SDIO / PCMIA CARD

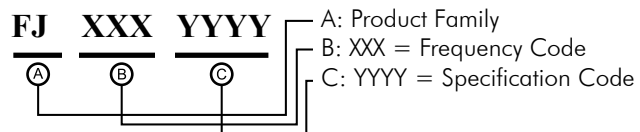• USB BT Interface

• Bluetooth

Package:

2.5±0.1

2.0±0.1

0.9±0.1

0.6   0.9   0.1

0.5

1.6

#1   #2

#4   #3
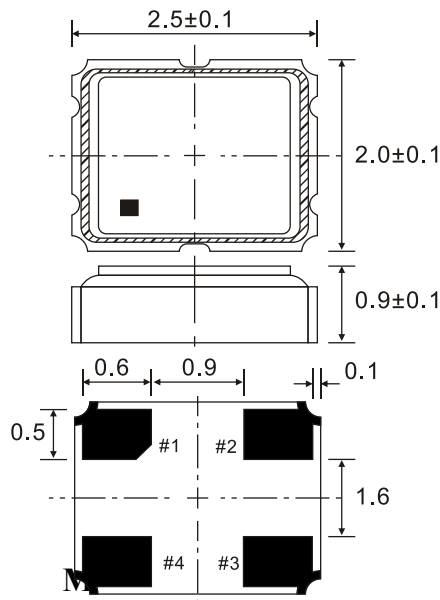
Recommended Land Pattern:

1.2   0.5   1.2

1.0

0.3

1.0

Pin Functions:

Pin	Function
1	ED
2	Ground
3	Clock Output
4	V$_{CC}$

Part Ordering Information:

FJ   XXX   YYYY

Ⓐ   Ⓑ   Ⓒ

A: Product Family
B: XXX = Frequency Code
C: YYYY = Specification Code

Following the above format, Saronix-eCera part numbers will be assigned upon confirmation of exact customer requirements.

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Electrical Performance

Parameter	Min.	Typ.	Max.	Units	Notes
Output Frequency	1		60	MHz	As specified
Supply Voltage	1.08	1.20	1.32	V	
Supply Current, Output Enabled			4	mA	
Supply Current, Standby Mode			10	μA	Output Hi-Z
Frequency Stability			±20 to ±50	ppm	See Note 1 below
Operating Temperature Range	-20		+70	°C	Commercial (standard)
	-40		+85		Industrial (standard)
Output Logic 0, V_{OL}			10% V_{DD}	V	
Output Logic 1, V_{OH}	90% V_{DD}			V	
Output Load			15	pF	
Duty Cycle	45		55	%	Measured 50% V_{DD}
Rise and Fall Time			5	ns	Measured 20/80% of waveform
Jitter, Phase			1	ps RMS (1-σ)	10kHz to 20 MHz frequency band
Jitter, Accumulated			5	ps RMS (1-σ)	20.000 adjacent periods
Jitter, Total			50	ps pk-pk	100.000 random periods

Notes:
1. Stability includes all combinations of operating temperature, load changes, rated input (supply) voltage changes, initial calibration tolerance (25°C), aging (1 year at 25°C average effective ambient temperature), shock and vibration.
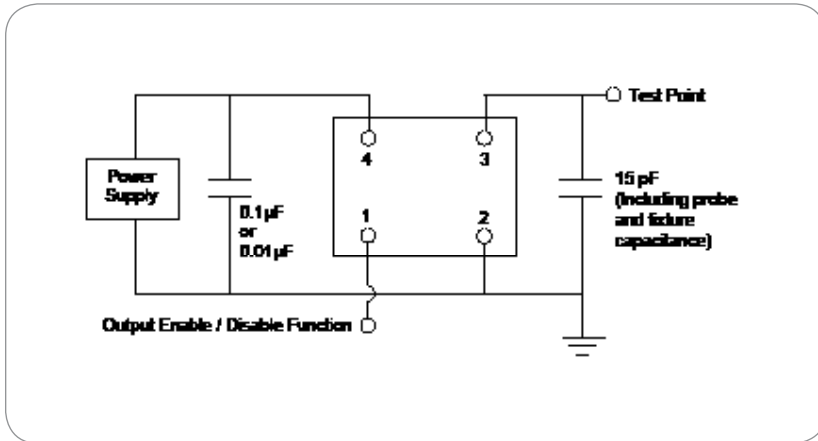2. For specifications othere than those listed, please contact sales.

Output Enable / Disable Function

Parameter	Min.	Typ.	Max.	Units	Notes
Input Voltage (pin 1), Output Enable	0.7			V	or open
Input Voltage (pin 1), Output Disable (low power standby)			0.3	V	Output is Hi-Z
Internal Pullup Resistance	50			kΩ	
Output Disable Delay			100	ns	
Output Enable Delay			10	ms	

Absolute Maximum Ratings

Parameter	Min.	Typ.	Max.	Units	Notes
Storage Temperature	-55		+125	°C	

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Test Circuit

Reflow Soldering Profile

As per IPC/JEDEC J-STD-020C
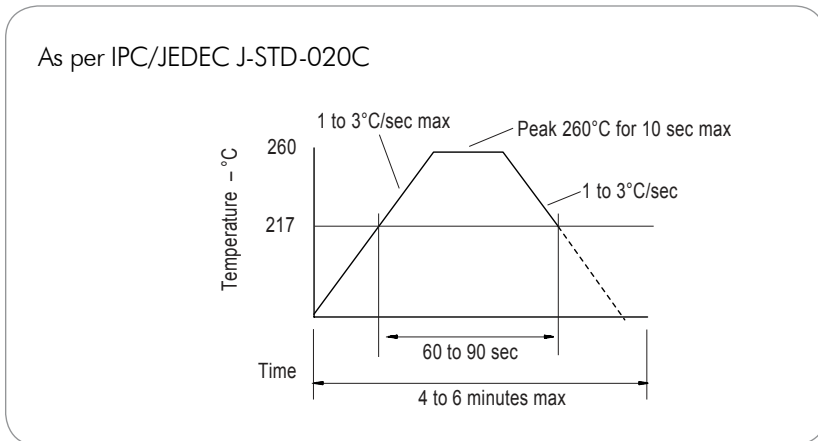
Reliability Test Ratings

This product is rated to meet the following test conditions:

Type	Parameter	Test Condition
Mechanical	Shock	MIL-STD-883, Method 2002, Condition B
Mechanical	Solderability	JESD22-B102-D Method 2 (Preconditioning E)
Mechanical	Terminal strength	MIL-STD-883, Method 2004, Condition D
Mechanical	Gross leak	MIL-STD-883, Method 1014, Condition C
Mechanical	Fine leak	MIL-STD-883, Method 1014, Condition A2 ($R_1 = 2 \times 10^{-8}$ atm cc/s)
Mechanical	Solvent resistance	MIL-STD-202, Method 215
Environmental	Thermal shock	MIL-STD-883, Method 1011, Condition A
Environmental	Moisture resistance	MIL-STD-883, Method 1004
Environmental	Vibration	MIL-STD-883, Method 2007, Condition A
Environmental	Resistance to soldering heat	J-STD-020C Table 5-2 Pb-free devices (2 cycles max)

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