



## GreenFET3 SLG59M1598V

Layout Guide

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## **Description**

The SLG59M1598V is a 17 m $\Omega$ , ~ 2.5 A single-channel load switch that is able to switch 0.85 V to 5 V power rails. The product is packaged in an ultra-small 1 x 1.6 mm package.

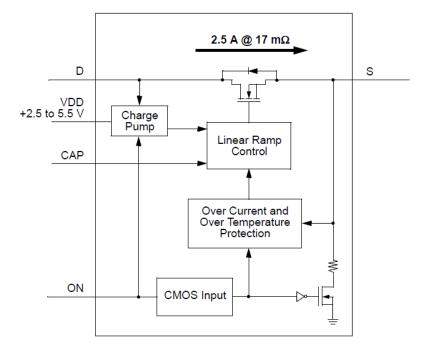


Figure 1: SLG59M1598V Block Diagram

This layout guide provides some important information about the PCB layout of SLG59M1598V applications.

SILEGO TDFN 1 x 1.6 - 8L PKG

Unit: um

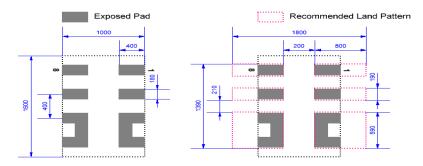


Figure 2. SLG59M1598V Package Dimensions and Recommended Land Pattern

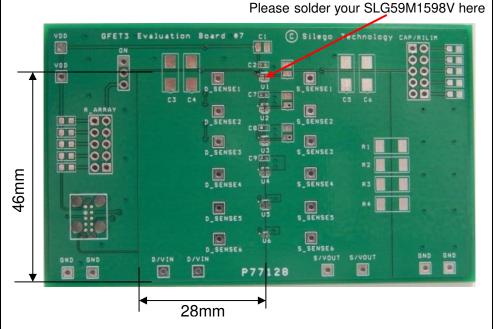


Figure 3. SLG59M1598V Evaluation Test Board

Note: Evaluation board has D\_Sense and S\_Sense pads. Please use them only for RDS(ON) evaluation.

## 2. Power and Ground Planes

- 2.1.The VDD pin needs 0.1uF external capacitor to smooth pulses from the power supply. Locate these capacitor close to PIN1.
- 2.2. The trace length from the control IC to the ON pin should be as short as possible and must avoid crossing this trace with power rails.
- 2.3. The D/VIN and S/VOUT pins carry significant current. Please note how the D/VIN and S/VOUT pads are placed directly on the power planes in Figure 3, which minimizes the RDS(ON) associated with long, narrow traces. The D/VIN and S/VOUT pins dissipate most of the heat generated during high-load current condition. The layout shown in Figure 3 is illustrating a proper solution for heat to transfer as efficiently as possible out of the device.
- 2.4. Place the power rail ramp capacitor as close as possible to the CAP pin (PIN7) to avoid/reduce the effect of parasitic mount capacitance.
- 2.5. The GND pin (PIN8) should be connected to GND.
- 2.6. 2 oz. copper is recommended for higher currents.