Data Sheet January 2002

20A, 30V, 0.025 Ohm, N-Channel Power MOSFETs

The RFD20N03 and RFD20N03SM N-Channel power MOSFETs are manufactured using the MegaFET process. This process which uses feature sizes approaching those of LSI integrated circuits, gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers, and relay drivers. These transistors can be operated directly from integrated circuits.

Formerly developmental type TA49235.

Ordering Information

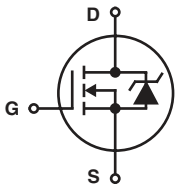
PART NUMBER	PACKAGE	BRAND
RFD20N03	TO-251AA	F20N03
RFD20N03SM	TO-252AA	F20N03

NOTE: When ordering, use the entire part number. Add the suffix 9A to obtain the TO-252AA variant in tape and reel, e.g., RFD20N03SM9A.

Features

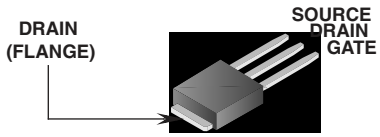
- 20A, 30V
- $r_{DS(ON)} = 0.025\Omega$
- Temperature Compensating PSPICE® Model
- Thermal Impedance SPICE Model
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- 175°C Operating Temperature
- Related Literature
  - TB334 “Guidelines for Soldering Surface Mount Components to PC Boards”

Symbol

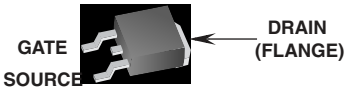


Packaging

JEDEC TO-251AA



JEDEC TO-252AA



Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

			UNITS
Drain to Source Voltage (Note 1)	V_{DSS}	30	V
Drain to Gate Voltage (R_{GS} = 20kΩ) (Note 1)	V_{DGR}	30	V
Gate to Source Voltage	V_{GS}	±20	V
Drain Current			
Continuous (Figure 2)	I_D	20	A
Pulsed Drain Current	I_{DM}	Figure 5	
Pulsed Avalanche Rating	E_{AS}	Figure 6	
Power Dissipation (Figure 4)	P_D	90	W
Derate Above 25^oC (Figure 1)		0.60	$W/^oC$
Operating and Storage Temperature	T_J, T_{STG}	-55 to 175	^oC
Maximum Temperature for Soldering			
Leads at 0.063in (1.6mm) from Case for 10s	T_L	300	^oC
Package Body for 10s, See Techbrief 334	T_{pkg}	260	^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. $T_J = 25^oC$ to 150^oC.

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV_{DSS}	I_D = 250μA, V_{GS} = 0V (Figure 11)		30	-	-	V
Gate to Source Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250μA (Figure 10)		2	-	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 30V, V_{GS} = 0V		-	-	1	μA
		V_{DS} = 30V, V_{GS} = 0V, $T_C = 150^oC$		-	-	50	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±20V		-	-	100	nA
Drain to Source On Resistance	$r_{DS(ON)}$	I_D = 20A, V_{GS} = 10V (Figure 9)		-	0.022	0.025	Ω
Turn-On Time	t_{ON}	V_{DD} = 15V, $I_D \cong$ 20A, R_L =0.75Ω, V_{GS} = 10V, R_{GS} = 9.1Ω		-	-	60	ns
Turn-On Delay Time	$t_{d(ON)}$			-	10	-	ns
Rise Time	t_r			-	30	-	ns
Turn-Off Delay Time	$t_{d(OFF)}$			-	12	-	ns
Fall Time	t_f			-	32	-	ns
Turn-Off Time	t_{OFF}			-	-	66	ns
Total Gate Charge	$Q_{g(TOT)}$	V_{GS} = 0V to 20V	V_{DD} = 15V, $I_D \cong$ 20A, R_L = 0.75Ω, $I_{g(REF)}$ = 1.0mA (Figure 13)	-	60	75	nC
Gate Charge at 10V	$Q_{g(10)}$	V_{GS} = 0V to 10V		-	28	40	nC
Threshold Gate Charge	$Q_{g(TH)}$	V_{GS} = 0V to 2V		-	2.4	2.9	nC
Input Capacitance	C_{ISS}	V_{DS} = 25V, V_{GS} = 0V, f = 1MHz (Figure 12)		-	1150	-	pF
Output Capacitance	C_{OSS}			-	550	-	pF
Reverse Transfer Capacitance	C_{RSS}			-	110	-	pF
Thermal Resistance Junction to Case	$R_{\theta JC}$	(Figure 3)		-	-	1.66	$^oC/W$
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	TO-251, TO-252		-	-	100	$^oC/W$

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage	V_{SD}	I_{SD} = 20A	-	-	1.25	V
Reverse Recovery Time	t_{rr}	I_{SD} = 20A, dI_{SD}/dt = 100A/μs	-	-	70	ns
Reverse Recovered Charge	Q_{RR}	I_{SD} = 20A, dI_{SD}/dt = 100A/μs	-	-	145	nC

Typical Performance Curves

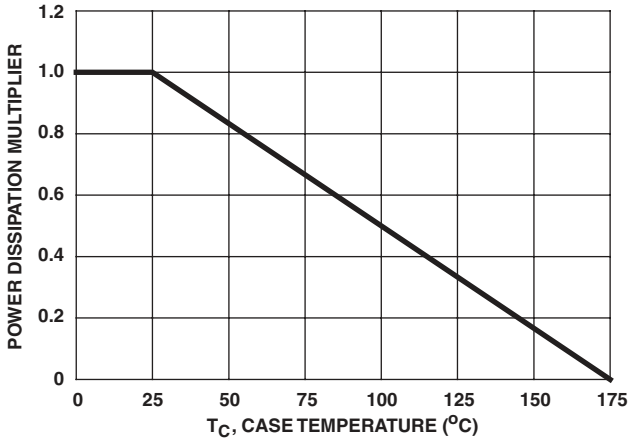


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

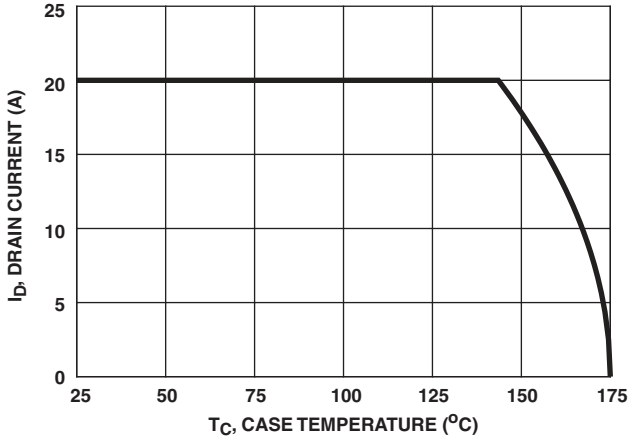


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

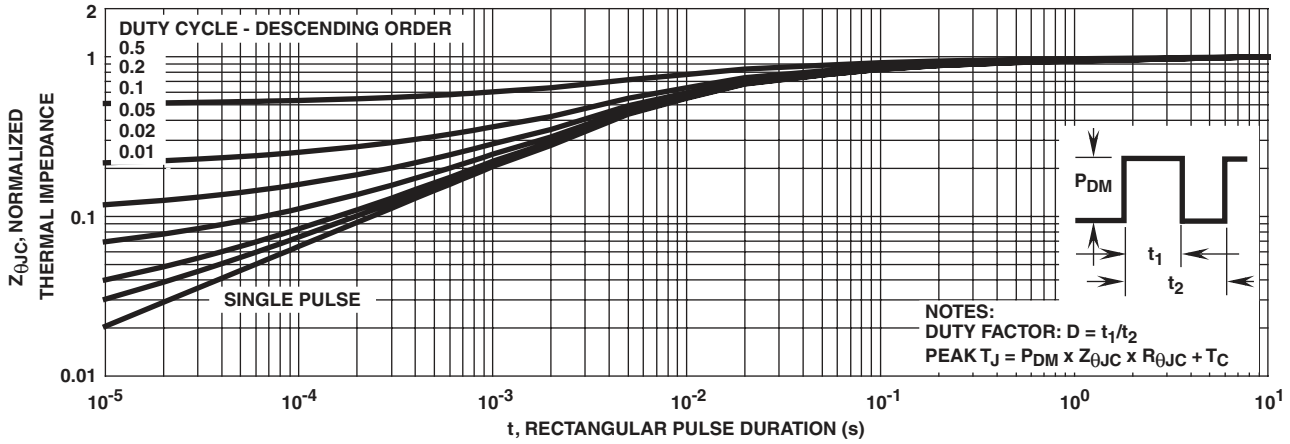


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

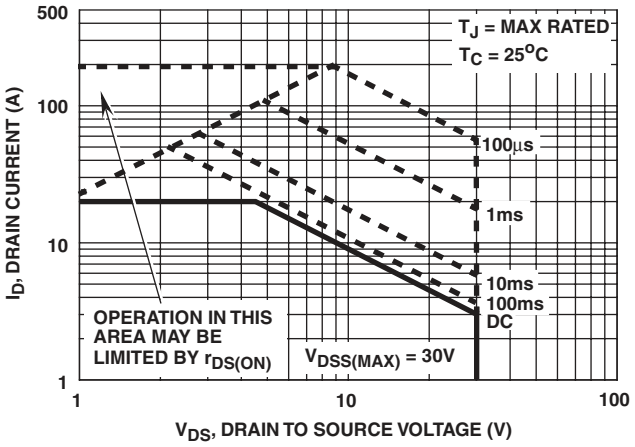


FIGURE 4. FORWARD BIAS SAFE OPERATING AREA

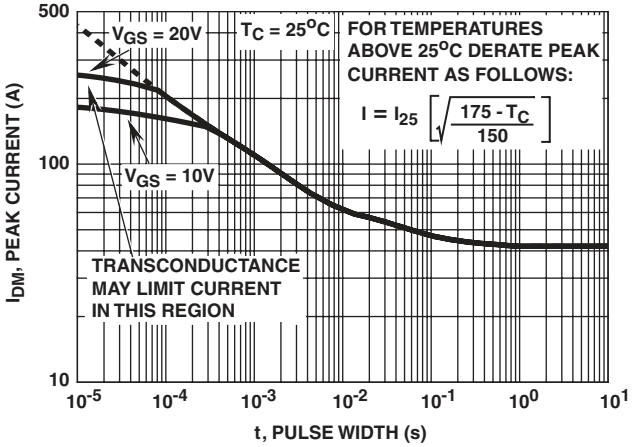
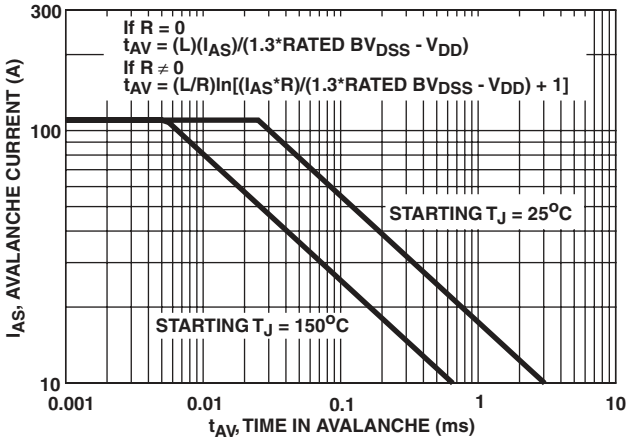


FIGURE 5. PEAK CURRENT CAPABILITY

Typical Performance Curves (Continued)



NOTE: Refer to Fairchild Application Notes AN9321 and AN9322.

FIGURE 6. UNCLAMPED INDUCTIVE SWITCHING CAPABILITY

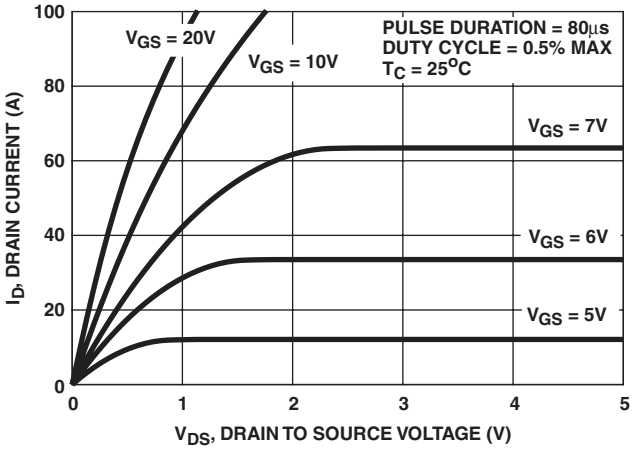


FIGURE 7. SATURATION CHARACTERISTICS

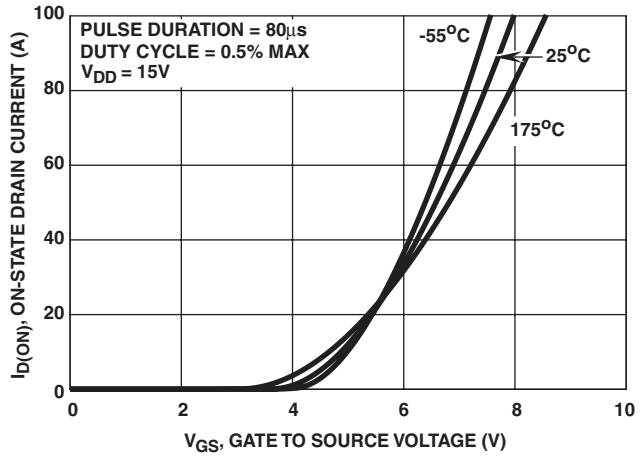


FIGURE 8. TRANSFER CHARACTERISTICS

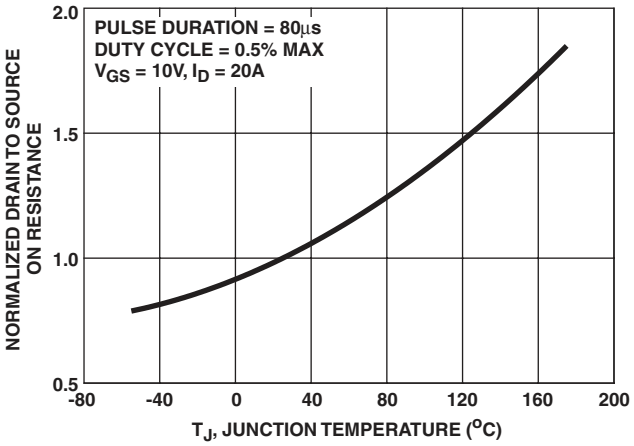


FIGURE 9. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

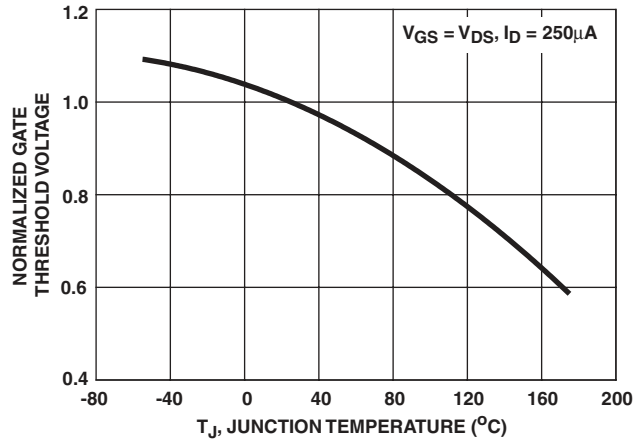


FIGURE 10. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

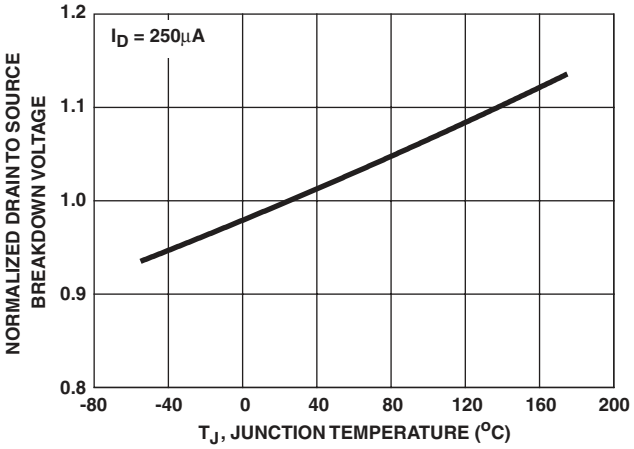


FIGURE 11. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

Typical Performance Curves (Continued)

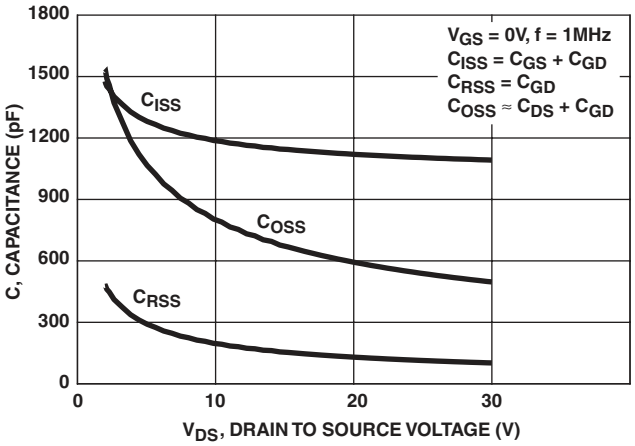


FIGURE 12. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE

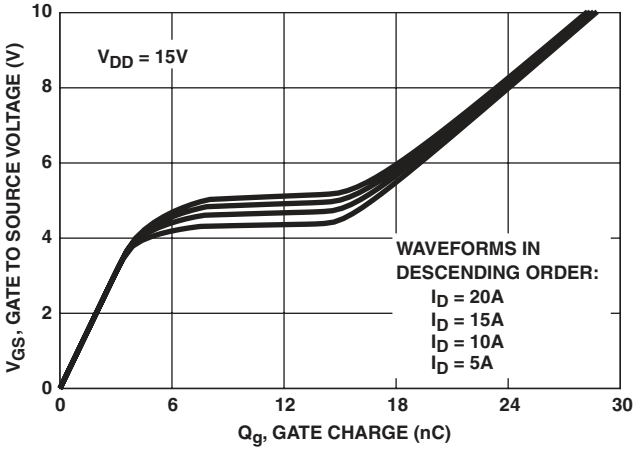


FIGURE 13. GATE CHARGE WAVEFORMS FOR CONSTANT GATE CURRENT

Test Circuits and Waveforms

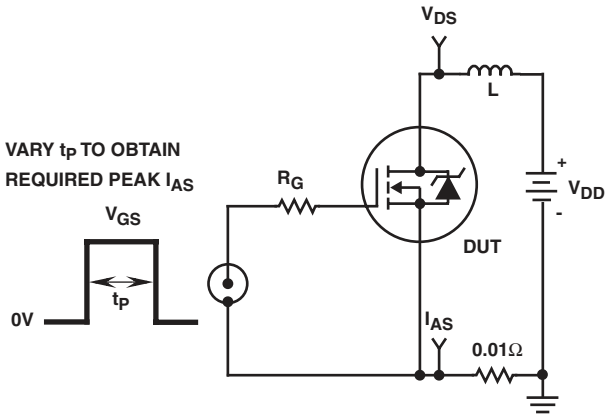


FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT

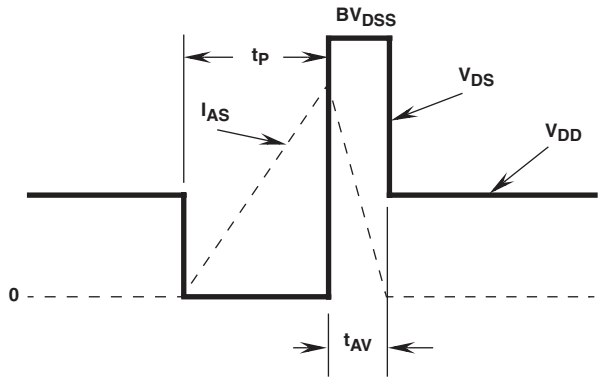


FIGURE 15. UNCLAMPED ENERGY WAVEFORMS

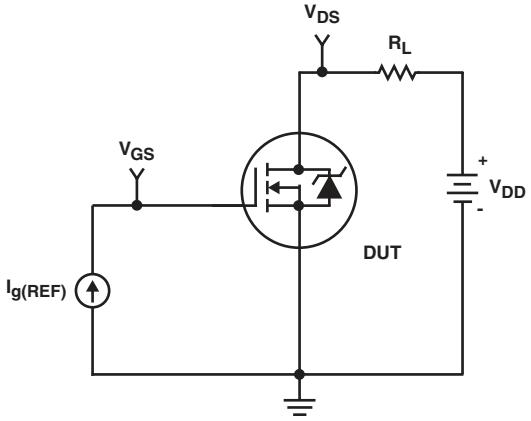


FIGURE 16. GATE CHARGE TEST CIRCUIT

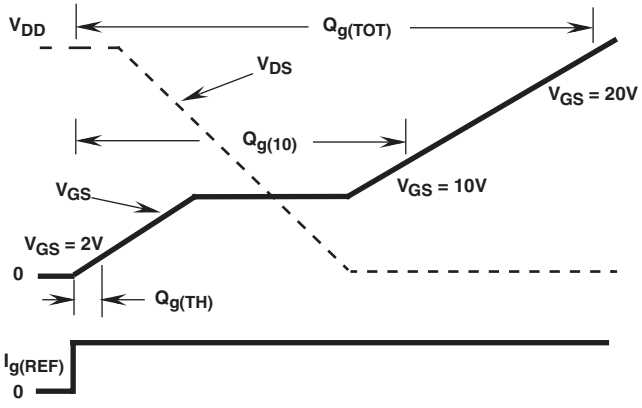


FIGURE 17. GATE CHARGE WAVEFORM

Test Circuits and Waveforms (Continued)

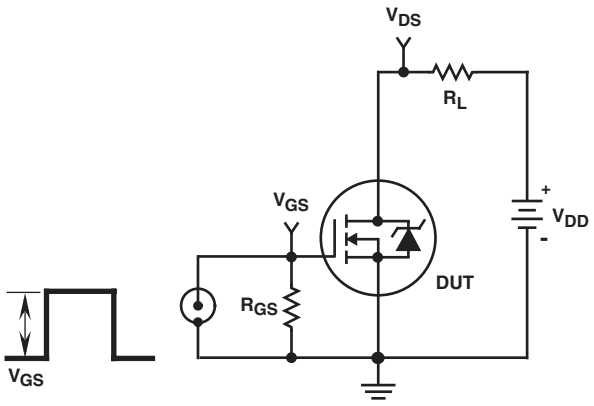


FIGURE 18. SWITCHING TIME TEST CIRCUIT

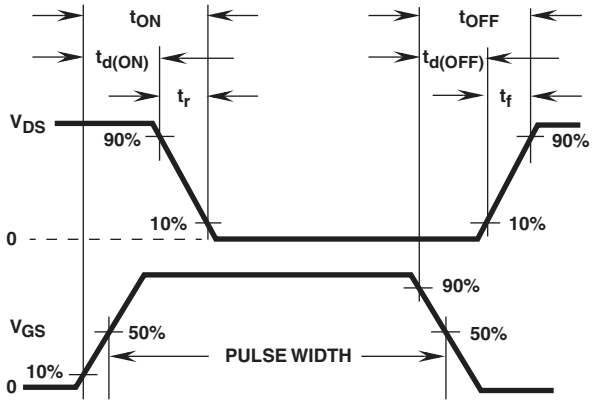


FIGURE 19. RESISTIVE SWITCHING WAVEFORMS

PSPICE Electrical Model

SUBCKT RFD20N03, RFD20N03SM 2 1 3 ; rev 28 Jul 97

CA 12 8 1.3e-9
CB 15 14 1.3e-9
CIN 6 8 9.9e-10

DBODY 7 5 DBODYMOD
DBREAK 5 11 DBREAKMOD
DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17 18 33.15
EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 6 10 6 8 1
EVTHRES 6 21 19 8 1
EVTEMP 20 6 18 22 1

IT 8 17 1

LDRAIN 2 5 1.00e-9
LGATE 1 9 3.57e-9
LSOURCE 3 7 4.25e-9

MMED 16 6 8 8 MMEDMOD
MSTRO 16 6 8 8 MSTROMOD
MWEAK 16 21 8 8 MWEAKMOD

RBREAK 17 18 RBREAKMOD 1
RDRAIN 50 16 RDRAINMOD 5e-4
RGATE 9 20 1.24
RLDRAIN 2 5 10
RLGATE 1 9 28.6
RLSOURCE 3 7 26.9
RSLC1 5 51 RSLCMOD 1e-6
RSLC2 5 50 1e3
RSOURCE 8 7 RSOURCEMOD 6.2e-3
RVTHRES 22 8 RVTHRESMOD 1
RVTEMP 18 19 RVTEMPMOD 1

S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD

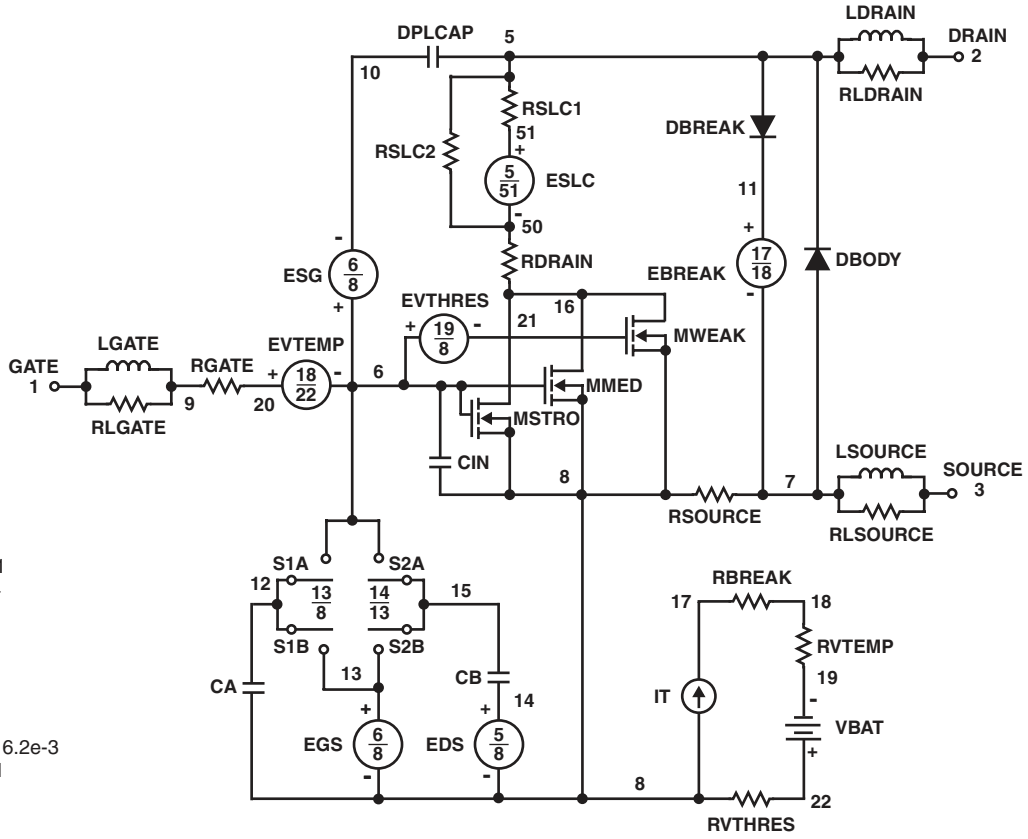
VBAT 22 19 DC 1

ESLC 51 50 VALUE={(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)/(1e-6*120),3))}

.MODEL DBODYMOD D (IS = 9e-13 RS = 6.4e-3 IKF=7.4 TIKF=0.005 N=1.02 TRS1 = 3.5e-3 TRS2 =-1e-5 CJO = 1.78e-9 TT = 4.0e-8 M = 0.4053)
.MODEL DBREAKMOD D (RS = 0.1 N=3.5 IKF=-1e-3 TRS1 = -1e-3 TRS2 =1e-6)
.MODEL DPLCAPMOD D (CJO = 1.3e-9 IS = 1e-30 N = 10 M = 0.62)
.MODEL MMEDMOD NMOS (VTO = 3.17 KP = 1.3 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 1.24)
.MODEL MSTROMOD NMOS (VTO = 3.68 KP = 13 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u)
.MODEL MWEAKMOD NMOS (VTO = 2.68 KP = 0.009 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 12.4 RS = 0.1)
.MODEL RBREAKMOD RES (TC1 = 8e-4 TC2 = 4.5e-7)
.MODEL RDRAINMOD RES (TC1 = 3.5e-2 TC2 = 4.5e-4)
.MODEL RSLCMOD RES (TC1 = 1e-3 TC2 = 1e-6)
.MODEL RSOURCEMOD RES (TC1 = 0 TC2 = 0)
.MODEL RVTHRESMOD RES (TC = -1.2e-3 TC2 = -2e-5)
.MODEL RVTEMPMOD RES (TC1 = -3.5e-3 TC2 = 1e-7)

.MODEL S1AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -8.60 VOFF= -2.50)
.MODEL S1BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -2.50 VOFF= -8.60)
.MODEL S2AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 0.00 VOFF= 0.30)
.MODEL S2AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 0.30 VOFF= 0.00)

.ENDS



NOTE: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank Wheatley.

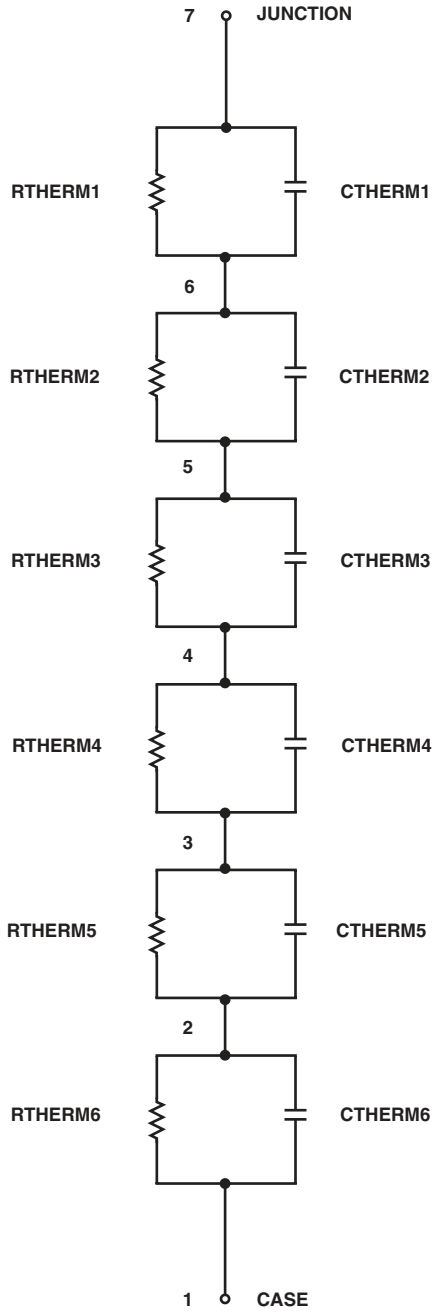
SPICE Thermal Model

REV 28 July 97

RFD20N03, RFD20N03SM

CTHERM1 7 6 9.9e-7
CTHERM2 6 5 1.5e-3
CTHERM3 5 4 2.2e-3
CTHERM4 4 3 5.7e-3
CTHERM5 3 2 7.5e-2
CTHERM6 2 1 5.4e-1

RTHERM1 7 6 8e-3
RTHERM2 6 5 2.3e-2
RTHERM3 5 4 9.0e-2
RTHERM4 4 3 6.9e-1
RTHERM5 3 2 6.1e-1
RTHERM6 2 1 8.0e-2



TRADEMARKS

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

ACEx™	FAST ®	OPTOLOGIC™	SMART START™	VCX™
Bottomless™	FASTr™	OPTOPLANAR™	STAR*POWER™	
CoolFET™	FRFET™	PACMAN™	Stealth™	
CROSSVOLT™	GlobalOptoisolator™	POP™	SuperSOT™-3	
DenseTrench™	GTO™	Power247™	SuperSOT™-6	
DOME™	HiSeC™	PowerTrench®	SuperSOT™-8	
EcoSPARK™	ISOPLANAR™	QFET™	SyncFET™	
E^2CMOS™	LittleFET™	QS™	TinyLogic™	
EnSigna™	MicroFET™	QT Optoelectronics™	TruTranslation™	
FACT™	MicroPak™	Quiet Series™	UHC™	
FACT Quiet Series™	MICROWIRE™	SILENT SWITCHER®	UltraFET®	

STAR*POWER is used under license

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.
As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.