



# TDA7401

## DIGITALLY CONTROLLED AUDIO PROCESSOR WITH LOUDSPEAKERS EQUALIZER

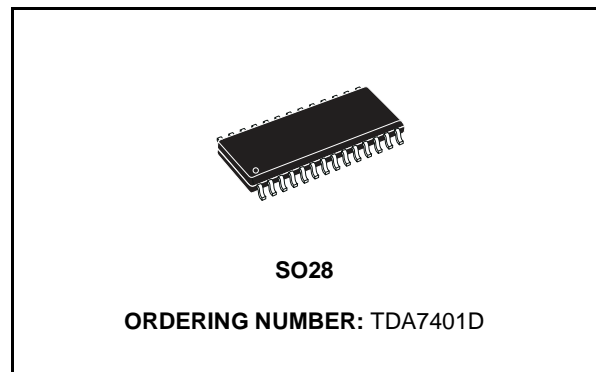
- FOUR HIGH PASS CHANNELS
- ONE STEREO LOW PASS CHANNEL WITH GAIN CONTROL
- DIRECT MUTE PIN
- FULLY PROGRAMMABLE VIA I<sup>2</sup>C BUS

### DESCRIPTION

The TDA7401 is an upgrade of the TDA7435 audioprocessor.

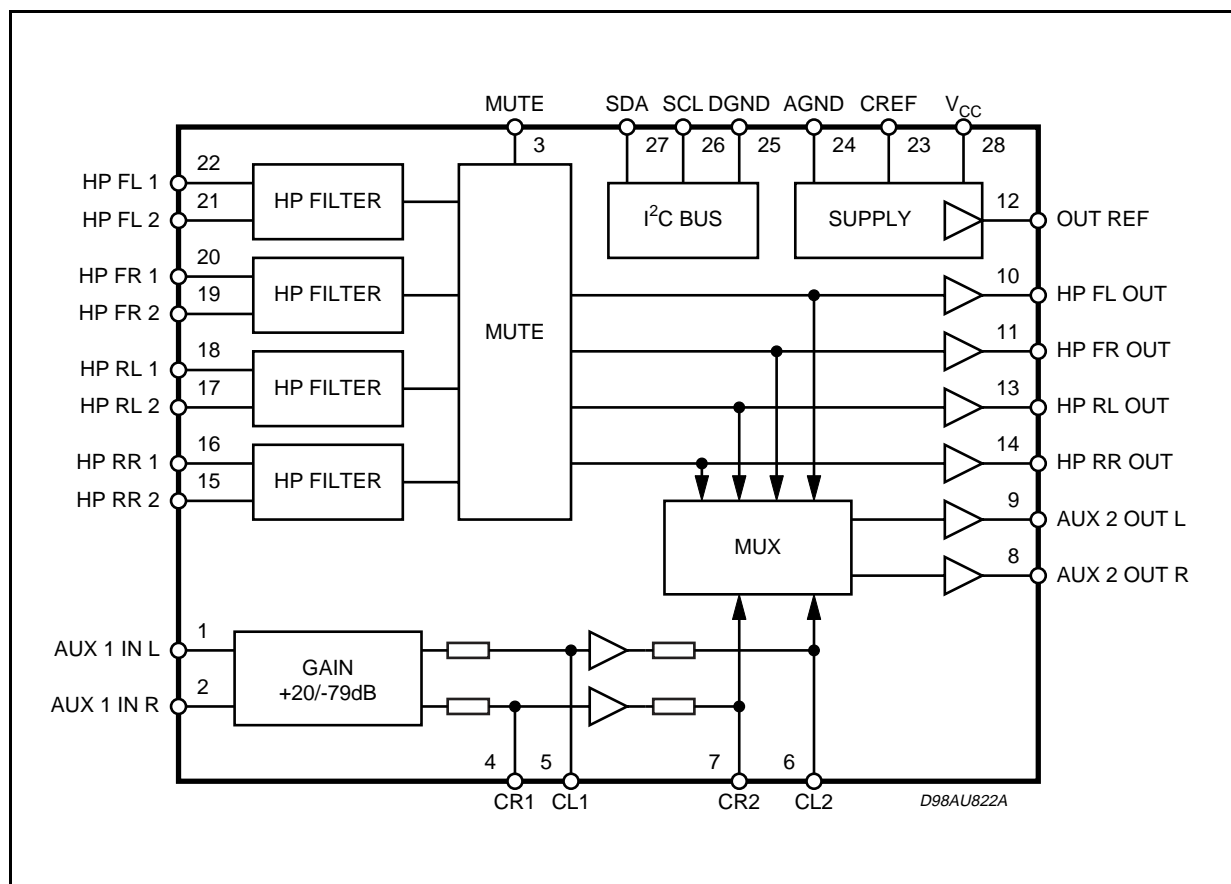
Due to a highly linear signal processing, using CMOS-switching techniques very low distortion and very low noise are obtained.

Second order high pass and low pass filters with programmable corner frequencies provide the loudspeaker equalization.



Very low DC stepping is obtained by using a BICMOS technology.

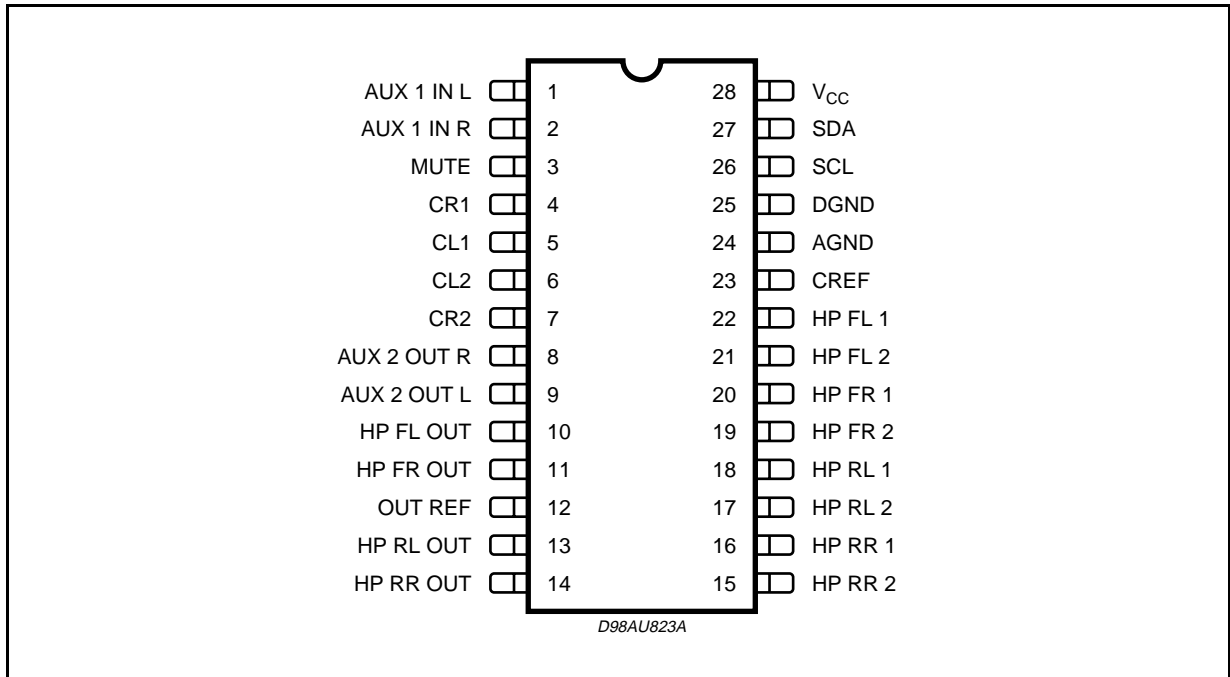
### BLOCK DIAGRAM



**ABSOLUTE MAXIMUM RATINGS**

| Symbol    | Parameter                     | Value      | Unit |
|-----------|-------------------------------|------------|------|
| $V_S$     | Operating Supply Voltage      | 10.5       | V    |
| $T_{amb}$ | Operating Ambient Temperature | -40 to 85  | °C   |
| $T_{stg}$ | Storage Temperature Range     | -55 to 150 | °C   |

**PIN CONNECTION**



**THERMAL DATA**

| Symbol          | Parameter                        | Value | Unit |
|-----------------|----------------------------------|-------|------|
| $R_{th\ j-amb}$ | Thermal Resistance Junction-pins | 65    | °C/W |

**QUICK REFERENCE DATA**

| Symbol    | Parameter   | Min. | Typ. | Max. | Unit |
|-----------|---|------|------|------|------|
| $V_S$     | Supply Voltage                                      | 6    | 9    | 10.2 | V    |
| $V_{CL}$  | Max. input signal handling                          | 2.1  | 2.6  |      | Vrms |
| THD       | Total Harmonic Distortion $V = 1V_{rms}$ $f = 1KHz$ |      | 0.01 | 0.08 | %    |
| S/N       | Signal to Noise Ratio                               |      | 106  |      | dB   |
| $S_C$     | Channel Separation $f = 1KHz$                       | -80  | 100  |      | dB   |
| $V_{REF}$ | Reference Voltage Output (pin 12)                   | 4.2  | 4.5  | 4.8  | V    |

**ELECTRICAL CHARACTERISTICS** ( $V_S = 9V$ ;  $R_L = 10K\Omega$ ;  $R_G = 50\Omega$ ;  $T_{amb} = 25^\circ C$ ; all gains = 0dB;  $f = 1KHz$ . Refer to the test circuit, unless otherwise specified.)

| Symbol                   | Parameter        | Test Condition | Min. | Typ. | Max. | Unit      |
|--------------------------|------------------|----------------|------|------|------|-----------|
| <b>INPUT STAGE: AUX1</b> |                  |                |      |      |      |           |
| $R_I$                    | Input Resistance |                | 37.5 | 50   | 62.5 | $K\Omega$ |
| $V_{CL}$                 | Clipping Level   | $d \leq 0.3\%$ | 2.1  | 2.6  |      | $V_{RMS}$ |
| $S_I$                    | Input Separation |                | 80   | 100  |      | dB        |

**GAIN CONTROL**

|            |                       |                            |       |     |       |    |
|------------|-----------------------|----------------------------|-------|-----|-------|----|
| $G_{MAX}$  | Maximum Input Gain    |                            |       | 20  |       | dB |
| $A_{MAX}$  | Maximum Attenuation   |                            |       | 79  |       | dB |
| $A_{STEP}$ | Step Resolution       |                            | 0.5   | 1   | 1.5   | dB |
| $E_A$      | Attenuation Set Error | $G = -20$ to $+20$ dB      | -1.25 | 0   | +1.25 | dB |
|            |                       | $G = -60$ to $-20$ dB      | -4    |     | 3     | dB |
| $E_T$      | Tracking Error        |                            |       |     | 2     | dB |
| $V_{DC}$   | DC Steps              | Adjacent Attenuation Steps |       | 0.1 | 3     | mV |
|            |                       | From 0dB to $G_{MIN}$      |       | 0.5 | 5     | mV |

**AUDIO OUTPUT (Pin 8 - 9, 10 - 14)**

|            |                        |             |     |     |     |           |
|------------|------------------------|-------------|-----|-----|-----|-----------|
| $V_{clip}$ | Clipping Level         | $d = 0.3\%$ | 2.1 | 2.6 |     | $V_{rms}$ |
| $R_L$      | Output Load Resistance | AC coupled  | 2   |     |     | $K\Omega$ |
| $R_O$      | Output Impedance       |             |     | 30  | 100 | $\Omega$  |
| $V_{DC}$   | DC Voltage Level       |             | 4.2 | 4.5 | 4.8 | V         |

**STAGE: HP FILTER**

|          |                       |                          |       |     |       |           |
|----------|-----------------------|--------------------------|-------|-----|-------|-----------|
| $R_1$    | Resistance at pin HP1 | HIGHPASS BYTE = XXXX1000 | 127.5 | 170 | 212.5 | $K\Omega$ |
| $R_2$    | Resistance at pin HP2 |                          | 1     |     |       | $M\Omega$ |
| $V_{CL}$ | Clipping Level        | $d \leq 0.3\%$           | 2.1   | 2.6 |       | $V_{rms}$ |

**MUTE**

|            |                         |          |      |     |      |           |
|------------|-------------------------|----------|------|-----|------|-----------|
| $A_{MUTE}$ | Mute Attenuation        |          | 80   | 100 |      | dB        |
| $V_{THM}$  | Mute Threshold          |          | 1.2  | 1.7 | 2.2  | V         |
| $R_{INT}$  | Pullup Resistor (pin 3) | (note 1) | 37.5 | 50  | 62.5 | $K\Omega$ |

**GENERAL**

|          |                              |   |    |      |      |         |
|----------|------------------------------|---|----|------|------|---------|
| $V_{CC}$ | Supply Voltage               |   | 6  | 9    | 10.2 | V       |
| $I_{CC}$ | Supply Current               |   | 7  | 8    | 9    | mA      |
| PSRR     | Power Supply Rejection Ratio | $f = 1KHz$  | 60 | 70   |      | dB      |
| $e_{NO}$ | Output Noise                 | Non Inverting Output Muted (B = 20 to 20kHz flat) |    | 3.5  | 15   | $\mu V$ |
|          |                              | All Gains 0dB (B = 20 to 20kHz flat)              |    | 5    | 15   | $\mu V$ |
| S/N      | Signal to Noise Ratio        | All Gains = 0dB; $V_O = 1V_{rms}$                 |    | 106  |      | dB      |
| $S_C$    | Channel Separation           |   | 80 | 100  |      | dB      |
| d        | Distortion                   | $V_{IN} = 1V$                                     |    | 0.01 | 0.08 | %       |

**BUS INPUTS**

|          |                                |                 |     |  |     |         |
|----------|--------------------------------|-----------------|-----|--|-----|---------|
| $V_{IL}$ | Input Low Voltage              |                 |     |  | 0.8 | V       |
| $V_{IH}$ | Input High Voltage             |                 | 2.5 |  |     | V       |
| $I_{IN}$ | Input Current                  | $V_{IN} = 0.4V$ | -5  |  | 5   | $\mu A$ |
| $V_O$    | Output Voltage SDA Acknowledge | $I_O = 1.6mA$   | 0.1 |  | 0.4 | V       |

Note 1: Internal pullup resistor to 3.3V; "LOW" = mute active

Figure 1. HP Filter

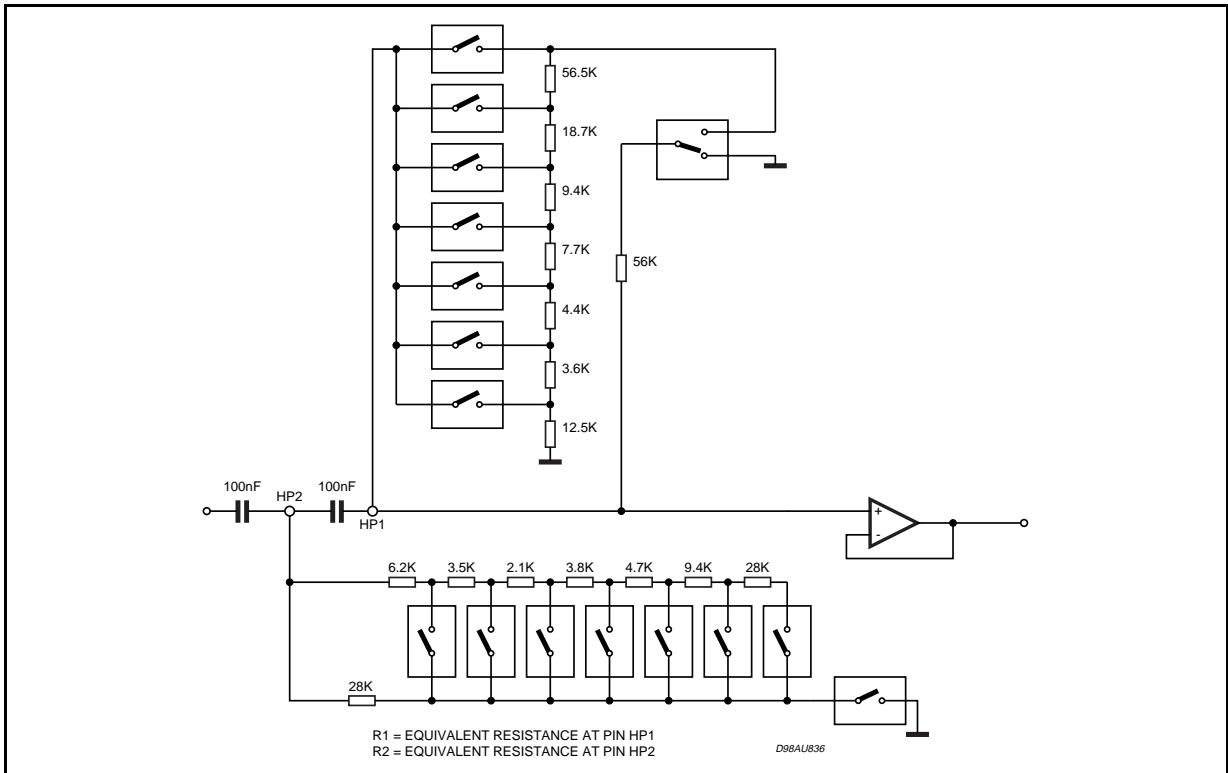
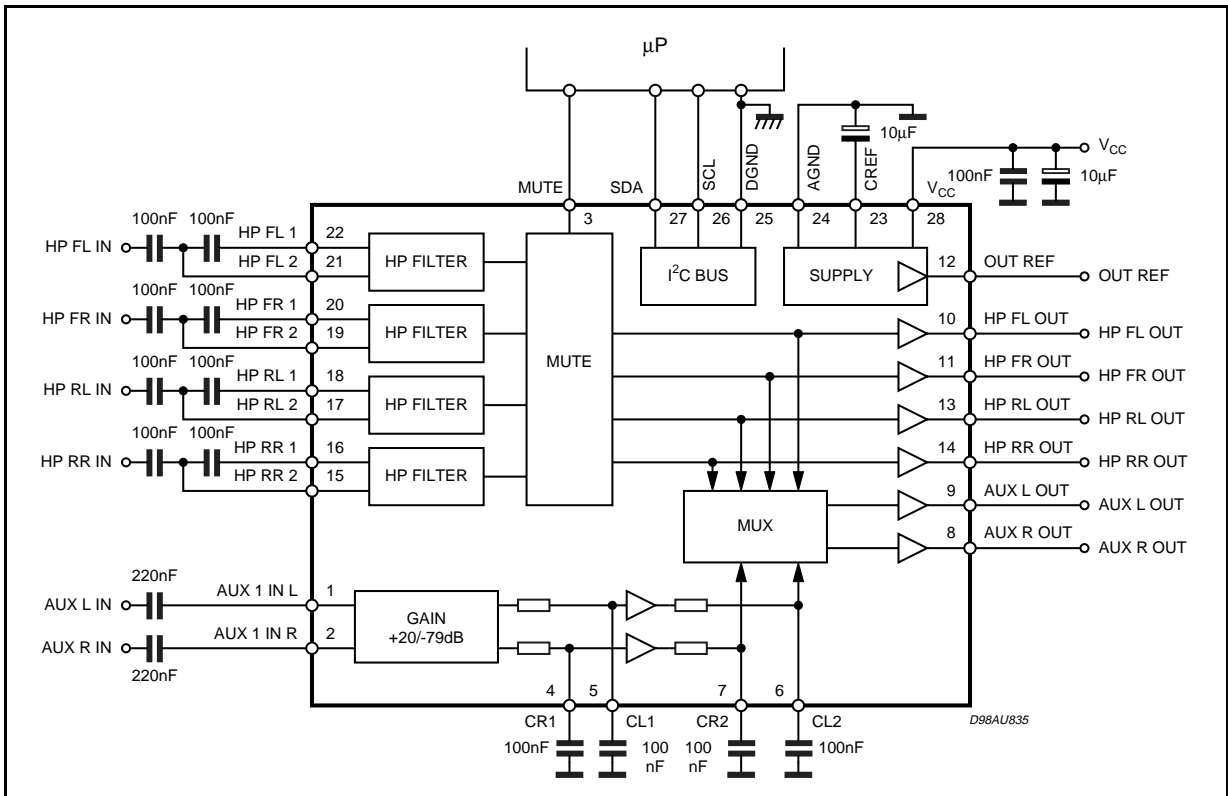


Figure 2. Application Circuit



**I<sup>2</sup>C BUS INTERFACE**

Data transmission from microprocessor to the TDA7401 and viceversa takes place thru the 2 wires I<sup>2</sup>C BUS interface, consisting of the two lines SDA and SCL (pull-up resistors to positive supply voltage must be externally connected).

**Data Validity**

As shown in fig. 2, the data on the SDA line must be stable during the high period of the clock. The HIGH and LOW state of the data line can only change when the clock signal on the SCL line is LOW.

**Start and Stop Conditions**

As shown in fig.3 a start condition is a HIGH to LOW transition of the SDA line while SCL is HIGH. The stop condition is a LOW to HIGH transition of the SDA line while SCL is HIGH. A STOP conditions must be sent before each START condition.

**Byte Format**

Every byte transferred to the SDA line must con-

tain 8 bits. Each byte must be followed by an acknowledge bit. The MSB is transferred first.

**Acknowledge**

The master ( $\mu$ P) puts a resistive HIGH level on the SDA line during the acknowledge clock pulse (see fig. 4). The peripheral (audioprocessor) that acknowledges has to pull-down (LOW) the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during this clock pulse.

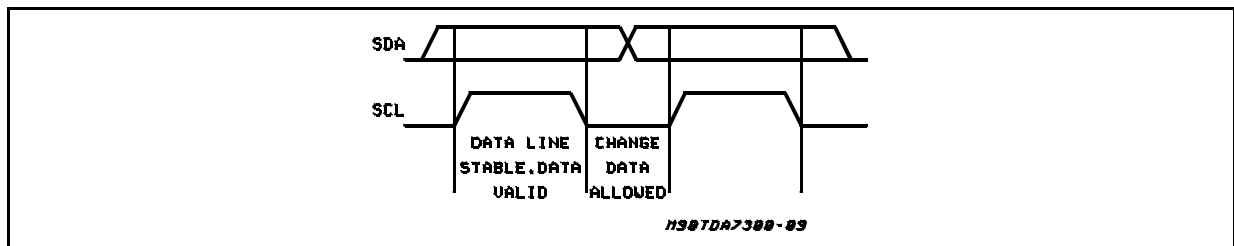
The audioprocessor which has been addressed has to generate an acknowledge after the reception of each byte, otherwise the SDA line remains at the HIGH level during the ninth clock pulse time. In this case the master transmitter can generate the STOP information in order to abort the transfer.

**Transmission without Acknowledge**

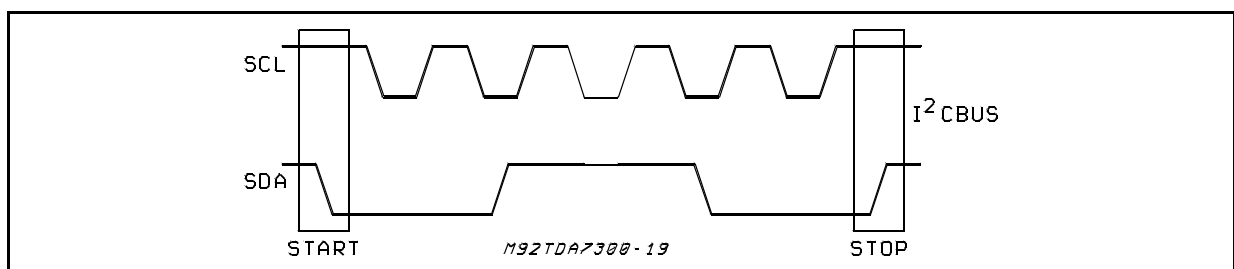
Avoiding to detect the acknowledge of the audioprocessor, the  $\mu$ P can use a simpler transmission: simply it waits one clock without checking the slave acknowledging, and sends the new data.

This approach of course is less protected from misworking and decreases the noise immunity.

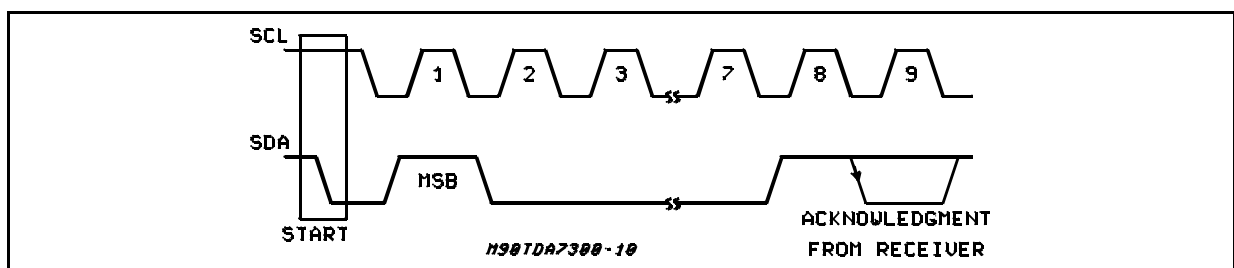
**Figure 3. Data Validity on the I<sup>2</sup>CBUS**



**Figure 4. Timing Diagram of I<sup>2</sup>CBUS**



**Figure 5. Acknowledge on the I<sup>2</sup>CBUS**



**SOFTWARE SPECIFICATION**

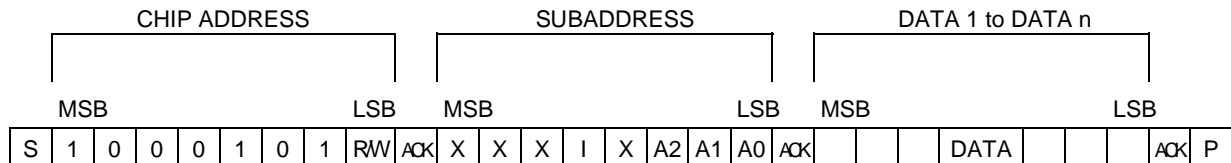
**Interface Protocol**

The interface protocol comprises:

- A start condition (s)
- A chip address byte,(the LSB bit determines

read/write transmission)

- A subaddress byte.
- A sequence of data (N-bytes + acknowledge)
- A stop condition (P)



ACK = Acknowledge  
 S = Start  
 P = Stop  
 I = Auto Increment  
 X = Not used

**AUTO INCREMENT**

If bit I in the subaddress byte is set to "1", the autoincrement of the subaddress is enabled

**SUBADDRESS (receive mode)**

| MSB |   |   |   |   | LSB |    |    | FUNCTION            |
|-----|---|---|---|---|-----|----|----|---------------------|
| X   | X | X | I | X | D2  | D1 | D0 |                     |
|     |   |   |   |   | 0   | 0  | 0  | Not used            |
|     |   |   |   |   | 0   | 0  | 1  | Mode                |
|     |   |   |   |   | 0   | 1  | 0  | Gain AUX 1 L        |
|     |   |   |   |   | 0   | 1  | 1  | Gain AUX 1 R        |
|     |   |   |   |   | 1   | 0  | 0  | High Pass Filter FL |
|     |   |   |   |   | 1   | 0  | 1  | High Pass Filter FR |
|     |   |   |   |   | 1   | 1  | 0  | High Pass Filter RL |
|     |   |   |   |   | 1   | 1  | 1  | High Pass Filter RR |

## MODE

| MSB |    |    |    |    |    |    | LSB | FUNCTION                                  |
|-----|----|----|----|----|----|----|-----|---|
| D7  | D6 | D5 | D4 | D3 | D2 | D1 | D0  |   |
|     |    |    |    |    |    | 0  | X   | High Pass Mute ON                         |
|     |    |    |    |    |    | 1  |     | High Pass Mute OFF                        |
|     |    |    |    |    | 0  |    |     | AUX1 Input Mute ON                        |
|     |    |    |    |    | 1  |    |     | AUX1 Input Mute OFF                       |
|     |    |    |    | 0  |    |    |     | AUX2 Inverted Output                      |
|     |    |    |    | 1  |    |    |     | AUX2 Non Inv. Output                      |
|     |    |    |    |    |    |    |     | <b>AUX 2 Output Selection</b>             |
|     |    | 0  | 0  |    |    |    |     | High Pass Filter Front                    |
|     |    | 0  | 1  |    |    |    |     | High Pass Filter Rear                     |
|     |    | 1  | 0  |    |    |    |     | Aux 1 Input                               |
|     |    | 1  | 1  |    |    |    |     | Mute                                      |
|     |    |    |    |    |    |    |     | AUX1 Low Pass Filter<br>(C1 = C2 = 100nF) |
| 0   | 0  |    |    |    |    |    |     | Flat                                      |
| 0   | 1  |    |    |    |    |    |     | 120Hz                                     |
| 1   | 0  |    |    |    |    |    |     | 80Hz                                      |
| 1   | 1  |    |    |    |    |    |     | 50Hz                                      |

## GAIN AUX1L, AUX1R

| MSB |    |    |    |    |    |    | LSB | GAIN AUX1L, R |
|-----|----|----|----|----|----|----|-----|---------------|
| D7  | D6 | D5 | D4 | D3 | D2 | D1 | D0  |               |
| 1   | 0  | 0  | 1  | 1  | 1  | 1  | 1   | +31dB         |
| :   | :  | :  | :  | :  | :  | :  | :   | :             |
| 1   | 0  | 0  | 1  | 0  | 0  | 0  | 1   | +17dB         |
| 1   | 0  | 0  | 1  | 0  | 0  | 0  | 0   | +16dB         |
| 1   | 0  | 0  | 0  | 1  | 1  | 1  | 1   | +15dB         |
| :   | :  | :  | :  | :  | :  | :  | :   | :             |
| 1   | 0  | 0  | 0  | 0  | 0  | 0  | 1   | +1dB          |
| 1   | 0  | 0  | 0  | 0  | 0  | 0  | 0   | 0dB           |
| 0   | 0  | 0  | 0  | 0  | 0  | 0  | 0   | 0dB           |
| 0   | 0  | 0  | 0  | 0  | 0  | 0  | 1   | -1dB          |
| :   | :  | :  | :  | :  | :  | :  | :   | :             |
| 0   | 0  | 0  | 0  | 1  | 1  | 1  | 1   | -15dB         |
| 0   | 0  | 0  | 1  | 0  | 0  | 0  | 0   | -16dB         |
| :   | :  | :  | :  | :  | :  | :  | :   | :             |
| 0   | 1  | 0  | 0  | 1  | 1  | 1  | 0   | -78dB         |
| 0   | 1  | 0  | 0  | 1  | 1  | 1  | 1   | -79dB         |
| X   | 1  | 1  | X  | X  | X  | X  | X   | Mute          |

**Note:** Is is not recommended to use a gain more than 20dB for system performance reason. In general, the max. gain should be limited by software to the maximum value, which is needed for the system.

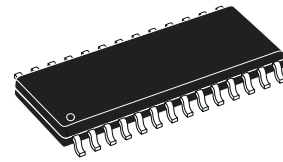
## HIGH PASS FILTERS

| MSB |    |    |    |    |    |    | LSB |   | FL, FR, RL, RR |
|-----|----|----|----|----|----|----|-----|---|----------------|
| D7  | D6 | D5 | D4 | D3 | D2 | D1 | D0  |   |                |
|     |    |    |    |    |    |    |     | <b>2nd order HP Filter Mode<br/>(C1 = C2 = 100nF)</b> |                |
| X   | X  | X  | X  | 0  | 0  | 0  | 0   | $f_c = 40\text{Hz}$                                   |                |
|     |    |    |    | 0  | 0  | 0  | 1   | $f_c = 60\text{Hz}$                                   |                |
|     |    |    |    | 0  | 0  | 1  | 0   | $f_c = 80\text{Hz}$                                   |                |
|     |    |    |    | 0  | 0  | 1  | 1   | $f_c = 100\text{Hz}$                                  |                |
|     |    |    |    | 0  | 1  | 0  | 0   | $f_c = 120\text{Hz}$                                  |                |
|     |    |    |    | 0  | 1  | 0  | 1   | $f_c = 150\text{Hz}$                                  |                |
|     |    |    |    | 0  | 1  | 1  | 0   | $f_c = 180\text{Hz}$                                  |                |
|     |    |    |    | 0  | 1  | 1  | 1   | $f_c = 220\text{Hz}$                                  |                |
|     |    |    |    |    |    |    |     | <b>First order HP Flat Mode</b>                       |                |
|     |    |    |    | 1  | 0  | 0  | 0   | $f_c = 9\text{Hz}$                                    |                |

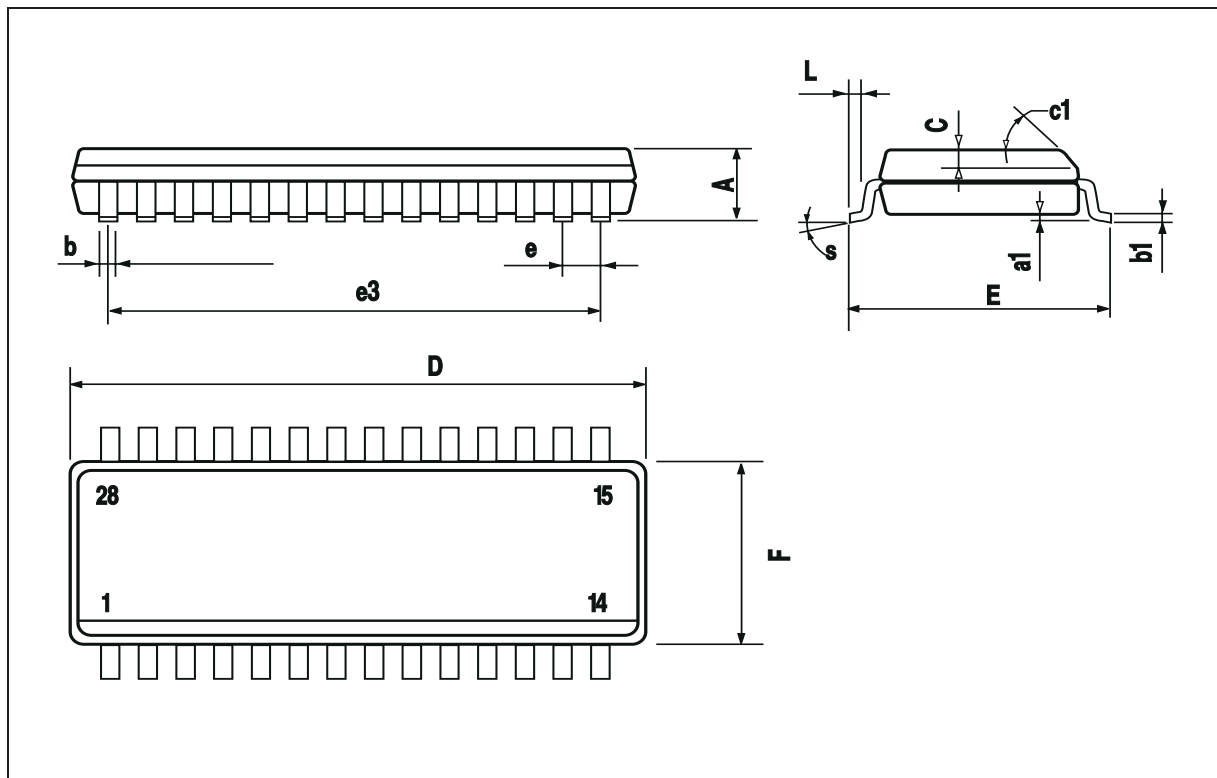


| DIM. | mm         |       |       | inch  |       |       |
|------|------------|-------|-------|-------|-------|-------|
|      | MIN.       | TYP.  | MAX.  | MIN.  | TYP.  | MAX.  |
| A    |            |       | 2.65  |       |       | 0.104 |
| a1   | 0.1        |       | 0.3   | 0.004 |       | 0.012 |
| b    | 0.35       |       | 0.49  | 0.014 |       | 0.019 |
| b1   | 0.23       |       | 0.32  | 0.009 |       | 0.013 |
| C    |            | 0.5   |       |       | 0.020 |       |
| c1   | 45° (typ.) |       |       |       |       |       |
| D    | 17.7       |       | 18.1  | 0.697 |       | 0.713 |
| E    | 10         |       | 10.65 | 0.394 |       | 0.419 |
| e    |            | 1.27  |       |       | 0.050 |       |
| e3   |            | 16.51 |       |       | 0.65  |       |
| F    | 7.4        |       | 7.6   | 0.291 |       | 0.299 |
| L    | 0.4        |       | 1.27  | 0.016 |       | 0.050 |
| S    | 8° (max.)  |       |       |       |       |       |

**OUTLINE AND MECHANICAL DATA**



**SO28**



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