

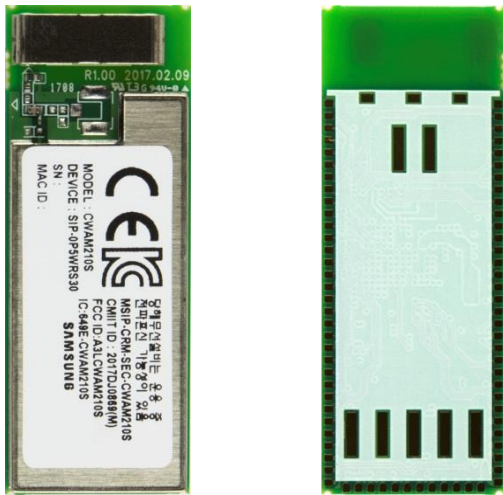


SAMSUNG  
**ARTIK**<sup>™</sup> Modules

**0**

**ARTIK 053 Datasheet**

# MODULE OVERVIEW



Top View (Left) and Bottom View (Right) of ARTIK 053 Module

The Samsung ARTIK™ 053 Module is a highly integrated module for secure Internet of Things (IoT) devices that require Wi-Fi® Connectivity. It is based on an ARM® Cortex® R4 core, with on-module RAM and flash memory, a complete 2.4GHz Wi-Fi subsystem with on-module antenna, an independent security subsystem, PUF-based module authentication, and a large complement of standard I/O interfaces.

ARTIK 053 Module provides excellent performance in a variety of environments, with a feature set tailored specifically for IoT end nodes.

|                         |                                                                                                                    |
|-------------------------|--------------------------------------------------------------------------------------------------------------------|
| <b>Processor</b>        |                                                                                                                    |
| <b>CPU</b>              | 32 bit ARM® Cortex® R4 with 32KB I-Cache and 32KB D-Cache 320MHz                                                   |
| <b>Memory</b>           |                                                                                                                    |
| <b>RAM</b>              | 1280KB (General usage)<br>128KB (Global IPC data)                                                                  |
| <b>FLASH</b>            | 8MB flash                                                                                                          |
| <b>Security</b>         |                                                                                                                    |
| <b>Secure System</b>    | AES/DES/TDES, SHA-1/SHA-2, PKA (Public Key Accelerator), PRNG/DTRNG (Random Number Generators), Secure key storage |
| <b>PUF</b>              | Physically Unclonable Function                                                                                     |
| <b>Radio</b>            |                                                                                                                    |
| <b>Wi-Fi</b>            | Certified IEEE802.11™ b/g/n Wi-Fi® 2.4GHz radio                                                                    |
| <b>Regulatory</b>       | FCC (U.S.), IC (Canada), CE (EU), KC (Korea), SRRC (China)                                                         |
| <b>Power Management</b> |                                                                                                                    |
| <b>Single Supply</b>    | Wide voltage input range 5-12V                                                                                     |
| <b>Interfaces</b>       |                                                                                                                    |
| <b>I/O</b>              | UART, I²C, SPI, PWM, ADC, GPIO                                                                                     |
| <b>Form Factor</b>      |                                                                                                                    |
| <b>Dimensions</b>       | 15x40x3mm (WxHxD)                                                                                                  |

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## VERSION HISTORY

| Revision | Date       | Description              | Maturity |
|----------|------------|--------------------------|----------|
| V1.0     | 04/26/2017 | Public release Datasheet | Release  |

## BLOCK DIAGRAM

Figure 1 shows the functional Block Diagram of the ARTIK 053 Module.

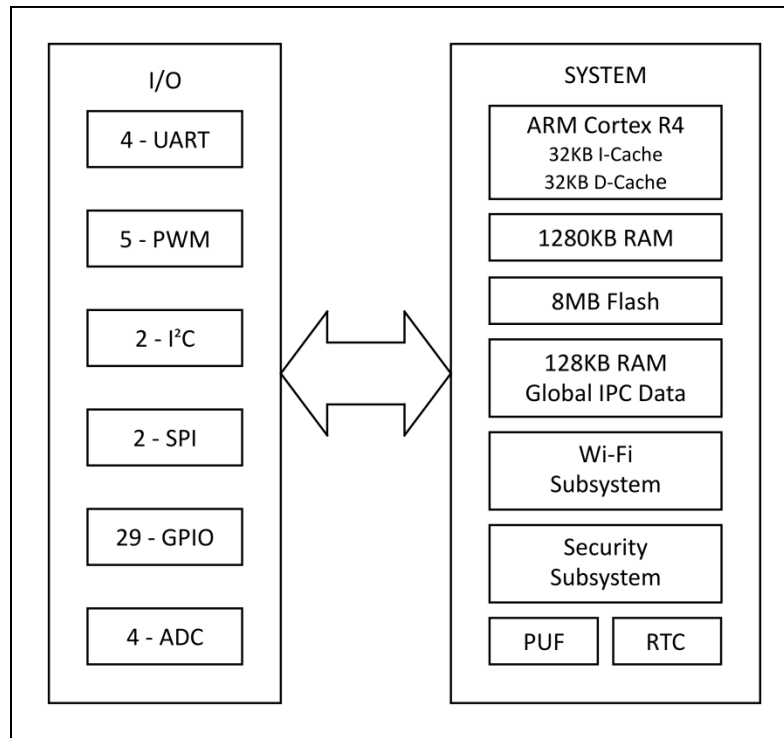


Figure 1. ARTIK 053 Module Block Diagram

## CPU

The ARTIK 053 Module CPU has an ARM® Cortex® R4. It has the following features:

- 32KB of Instruction Cache (I-Cache)
- 32KB of Data Cache (D-Cache)
- 320 MHz execution clock
- R4 core tuned for embedded and real-time applications

## MEMORY

The ARTIK 053 Module on-module memory has the following features:

- CPU and general purpose RAM
  - 1280KB CPU RAM
  - 128KB global Inter-Process Communication (IPC) RAM
- 8MB flash

## REAL TIME CLOCK

The ARTIK 053 Module has a Real Time Clock (RTC) for tracking date/time. The RTC has the following features:

- Binary-Coded Decimal (BCD) coded seconds, minutes, hour, day of the week, day, month, and year
- Leap year detection and compensation
- Millisecond tick time interrupt for Real-Time Operating System (RTOS) kernel time tick

## PUF UNIT

The ARTIK 053 Module has a Physically Unclonable Function (PUF) unit. The PUF unit has the following features:

- Generates unique key values, locked to an individual ARTIK 053 Module
- The algorithm construction is unique to each module
- Allows individual ARTIK 053 Modules to be “fingerprint-identified”

## SECURITY SUBSYSTEM

The ARTIK 053 Module has an independent security subsystem to ensure secure end-to-end operation in any IoT environment. The security subsystem includes the following features:

- Protected Execution Environment
  - Secure IPC Mailbox for inter-subsystem communication
  - Encapsulated key support
    - Backup encryption key - 256 bits
    - Security subsystem root private key - 521 bits
    - Storage key - 256 bits
- Symmetric key engines
  - Secure AES
  - Secure DES/Triple-DES
- Stream cipher engine
  - ARC4 engine
- Various Hash engines
  - SHA-1, SHA2-256, SHA2-384, SHA2-512, MD5 HMAC
- Asymmetric key engines
  - PKA (Public Key Accelerator) engine
- PRNG (Pseudo Random Number Generator)
- DTRNG (Digital True Random Number Generator)
- Secure key storage

## WI-FI SUBSYSTEM

The ARTIK 053 Module has an 802.11b/g/n Wi-Fi subsystem. The Wi-Fi subsystem has the following features:

- 802.11™ b/g/n support at 2.4GHz
- 20MHz single stream (802.11n)
- WPA/WPA2/WAPI
- Dedicated Wi-Fi Processor subsystem

## UART INTERFACE

The ARTIK 053 Module has four 2-pin UART interfaces, each with the following features:

- Can be operated in DMA or interrupt-based mode
- Support for 5, 6, 7 or 8 bit serial data transmit and receive
- Programmable baud rate
- One or two stop bit insertion

## GPIO INTERFACE

The ARTIK 053 Module has flexible General Purpose Input Output (GPIO) interfaces:

- 29 configurable GPIO ports
- Independently configurable for either input or output
- Configurable internal pull-up or pull-down resistors

## I<sup>2</sup>C INTERFACE

The ARTIK 053 Module has two high speed multi-master I<sup>2</sup>C interfaces available, with speeds up to 3.4Mbps.

## PWM INTERFACE

The ARTIK 053 Module has five PWM timers available, each with the following features:

- 32 bits of resolution for each PWM signal
- Two 8 bit pre-scalers (first level of division) and 5 clock-dividers/multiplexers for second level division
- Continuous run or one-shot pulse mode
- Dead zone generator to avoid simultaneous change of multiple PWM signals
- Interrupt generation

## SPI INTERFACE

The ARTIK 053 Module has two SPI interfaces, each with the following features:

- Full duplex communication
- 8, 16 or 32 bit shift registers and bus interface
- Motorola SPI protocol and National Semiconductor Microwire protocol
- Master and slave mode operation
- Two independent 32 bit wide transmit/receive FIFOs
- Transmit and receive speeds up to 50MHz

## ADC INTERFACE

The ARTIK 053 Module has four channels of analog-to-digital converter. The A/D interface has the following features:

- 12 bit resolution
- ADC conversion clock at 1.08 MSPS (Sampling per Second) using a main 6.5 MHz clock
- Support sample averaging over 1, 2, 4, 8, 16, 32, 64 samples
- Differential non-linearity error  $\pm 2$  LSB
- Integral non-linearity error  $\pm 6$  LSB
- Top offset error  $\pm 10$  LSB
- Bottom offset error  $\pm 10$  LSB
- Voltage range up to 1.8V

Figure 2 depicts the dynamic behavior between input voltage on the ADC and resulting LSB value in the ADC register.

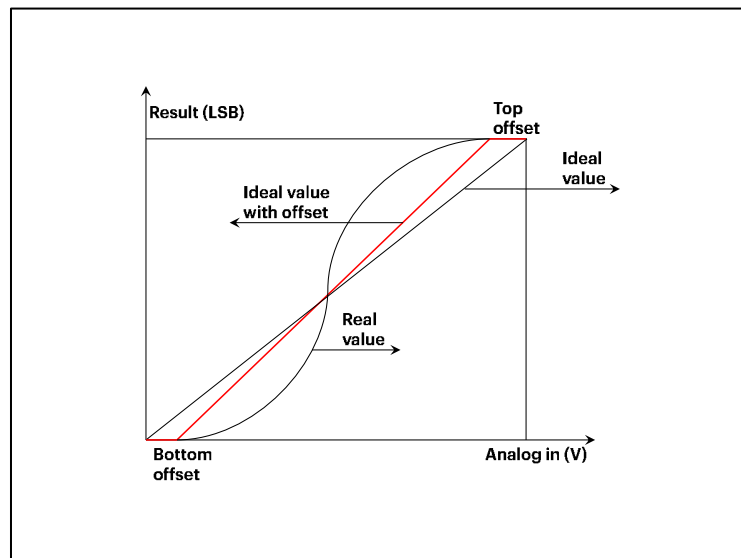


Figure 2. ADC LSB behavior



# MODULE EDGE PINOUT

The ARTIK 053 Module utilizes 79 signal, power, and ground pads. *Figure 3* shows how the Edge Pinout is oriented and how signal coordinates are assigned to the edge of the ARTIK 053 Module. *Table 1* shows the edge pads and the signal names.

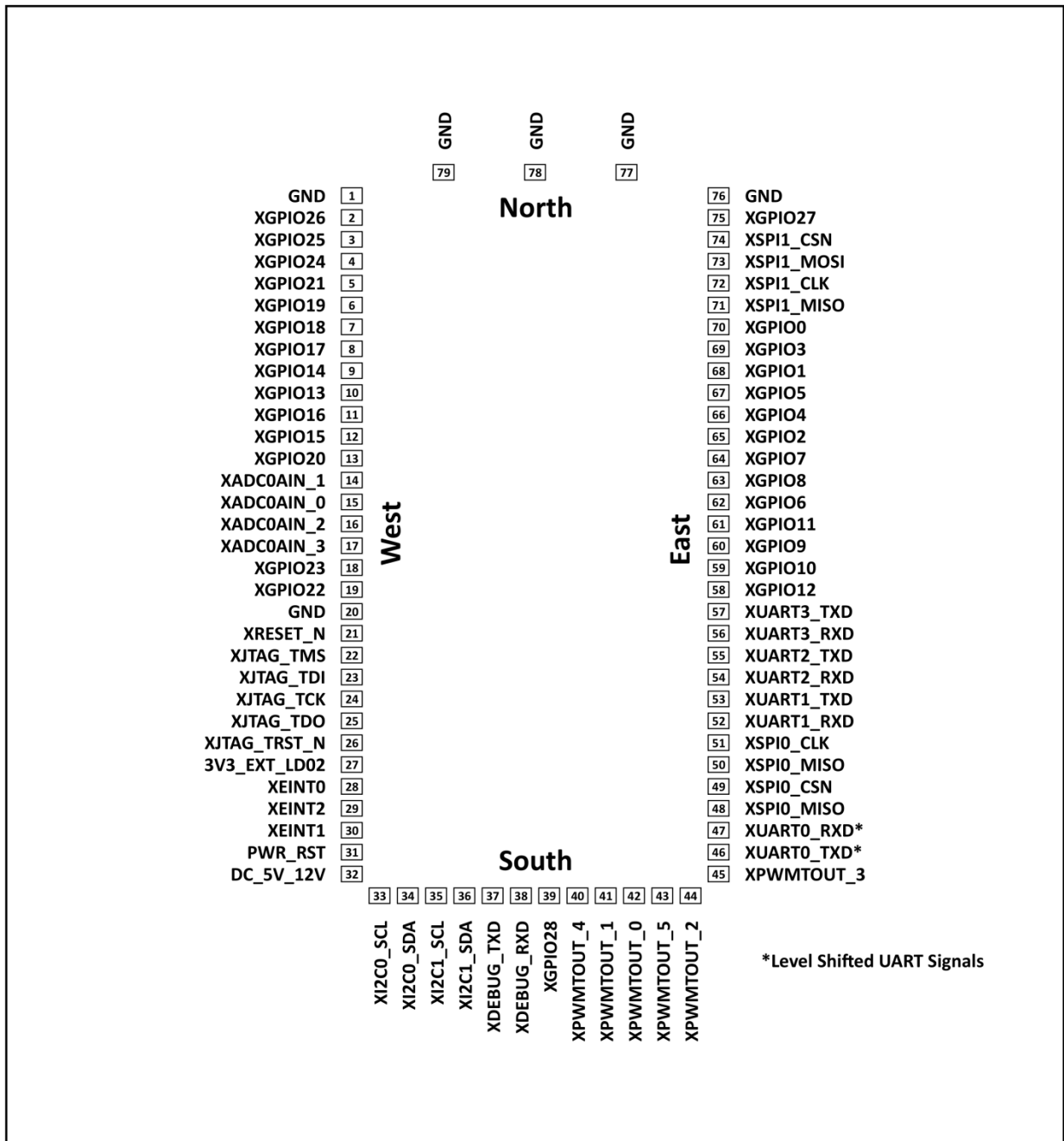


Figure 3. ARTIK 053 Module Edge Pinout

Table 1. ARTIK 053 Module Edge Pinout Signal Descriptions

| Pad Number | Pad Name     | I/O Type* | PU/PD | Power           | Default Function |
|------------|--------------|-----------|-------|-----------------|------------------|
| 1          | GND          | -         | -     | -               | GND              |
| 2          | XGPIO26      | I         | PD    | VDDQ33_EXT0     | GPIO             |
| 3          | XGPIO25      | I         | PD    | VDDQ33_EXT0     | GPIO             |
| 4          | XGPIO24      | I         | PD    | VDDQ33_EXT0     | GPIO             |
| 5          | XGPIO21      | I         | PD    | VDDQ33_EXT0     | GPIO             |
| 6          | XGPIO19      | I         | PD    | VDDQ33_EXT0     | GPIO             |
| 7          | XGPIO18      | I         | PD    | VDDQ33_EXT0     | GPIO             |
| 8          | XGPIO17      | I         | PD    | VDDQ33_EXT0     | GPIO             |
| 9          | XGPIO14      | I         | PD    | VDDQ33_EXT0     | GPIO             |
| 10         | XGPIO13      | I         | PD    | VDDQ33_EXT0     | GPIO             |
| 11         | XGPIO16      | I         | PD    | VDDQ33_EXT0     | GPIO             |
| 12         | XGPIO15      | I         | PD    | VDDQ33_EXT0     | GPIO             |
| 13         | XGPIO20      | I         | PD    | VDDQ33_EXT0     | GPIO             |
| 14         | XADC0AIN_1   | -         | -     | AVDD18_ADC0     | ADC              |
| 15         | XADC0AIN_0   | -         | -     | AVDD18_ADC0     | ADC              |
| 16         | XADC0AIN_2   | -         | -     | AVDD18_ADC0     | ADC              |
| 17         | XADC0AIN_3   | -         | -     | AVDD18_ADC0     | ADC              |
| 18         | XGPIO23      | I         | PD    | VDDQ1833_SDIO_0 | GPIO             |
| 19         | XGPIO22      | I         | PD    | VDDQ1833_SDIO_0 | GPIO             |
| 20         | GND          | -         | -     | -               | GND              |
| 21         | XRESET_N     | I         | -     | VDDQ33_EXT1     | RESET            |
| 22         | XJTAG_TMS    | I         | PU    | VDDQ33_EXT1     | DEBUG            |
| 23         | XJTAG_TDI    | I         | PU    | VDDQ33_EXT1     | DEBUG            |
| 24         | XJTAG_TCK    | I         | PD    | VDDQ33_EXT1     | DEBUG            |
| 25         | XJTAG_TDO    | I         | PD    | VDDQ33_EXT1     | DEBUG            |
| 26         | XJTAG_TRST_N | I         | PD    | VDDQ33_EXT1     | DEBUG            |
| 27         | 3V3_EXT_LDO2 | -         | -     | -               | POWER            |
| 28         | XEINT_0      | I         | PD    | VDDQ33_EXT1     | INT              |
| 29         | XEINT_2      | I         | PD    | VDDQ33_EXT1     | INT              |
| 30         | XEINT_1      | I         | PD    | VDDQ33_EXT1     | INT              |
| 31         | PWR_RST      | -         | -     | -               | RESET            |
| 32         | DC_5V_12V    | -         | -     | -               | POWER            |
| 33         | XI2C0_SCL    | I         | PD    | VDDQ33_EXT1     | I2C              |
| 34         | XI2C0_SDA    | I         | PD    | VDDQ33_EXT1     | I2C              |
| 35         | XI2C1_SCL    | I         | PD    | VDDQ33_EXT1     | I2C              |
| 36         | XI2C1_SDA    | I         | PD    | VDDQ33_EXT1     | I2C              |
| 37         | XDEBUG_TXD   | I         | PD    | VDDQ33_EXT1     | DEBUG            |
| 38         | XDEBUG_RXD   | I         | PD    | VDDQ33_EXT1     | DEBUG            |
| 39         | XGPIO28      | I         | PD    | VDDQ33_EXT0     | GPIO             |
| 40         | XPWMOUT_4    | I         | PD    | VDDQ33_EXT0     | PWM              |
| 41         | XPWMOUT_1    | I         | PD    | VDDQ33_EXT0     | PWM              |
| 42         | XPWMOUT_0    | I         | PD    | VDDQ33_EXT0     | PWM              |
| 43         | XPWMOUT_5    | I         | PD    | VDDQ33_EXT0     | PWM              |
| 44         | XPWMOUT_2    | I         | PD    | VDDQ33_EXT0     | PWM              |
| 45         | XPWMOUT_3    | I         | PD    | VDDQ33_EXT0     | PWM              |
| 46         | XUART0_TXD   | -         | -     | -               | LEVEL SHIFTED    |
| 47         | XUART0_RXD   | -         | -     | -               | LEVEL SHIFTED    |
| 48         | XSPI0_MISO   | I         | PD    | VDDQ33_EXT0     | SPI              |
| 49         | XSPI0_CSN    | I         | PD    | VDDQ33_EXT0     | SPI              |
| 50         | XSPI0_MOSI   | I         | PD    | VDDQ33_EXT0     | SPI              |
| 51         | XSPI0_CLK    | I         | PD    | VDDQ33_EXT0     | SPI              |

| Pad Number | Pad Name   | I/O Type* | PU/PD | Power       | Default Function |
|------------|------------|-----------|-------|-------------|------------------|
| 52         | XUART1_TXD | I         | PD    | VDDQ33_EXT0 | UART             |
| 53         | XUART1_RXD | I         | PD    | VDDQ33_EXT0 | UART             |
| 54         | XUART2_RXD | I         | PD    | VDDQ33_EXT0 | UART             |
| 55         | XUART2_TXD | I         | PD    | VDDQ33_EXT0 | UART             |
| 56         | XUART3_RXD | I         | PD    | VDDQ33_EXT0 | UART             |
| 57         | XUART3_TXD | I         | PD    | VDDQ33_EXT0 | UART             |
| 58         | XGPIO12    | I         | PD    | VDDQ33_EXT0 | GPIO             |
| 59         | XGPIO10    | I         | PD    | VDDQ33_EXT0 | GPIO             |
| 60         | XGPIO9     | I         | PD    | VDDQ33_EXT0 | GPIO             |
| 61         | XGPIO11    | I         | PD    | VDDQ33_EXT0 | GPIO             |
| 62         | XGPIO6     | I         | PD    | VDDQ33_EXT0 | GPIO             |
| 63         | XGPIO8     | I         | PD    | VDDQ33_EXT0 | GPIO             |
| 64         | XGPIO7     | I         | PD    | VDDQ33_EXT0 | GPIO             |
| 65         | XGPIO2     | I         | PD    | VDDQ33_EXT0 | GPIO             |
| 66         | XGPIO4     | I         | PD    | VDDQ33_EXT0 | GPIO             |
| 67         | XGPIO5     | I         | PD    | VDDQ33_EXT0 | GPIO             |
| 68         | XGPIO1     | I         | PD    | VDDQ33_EXT0 | GPIO             |
| 69         | XGPIO3     | I         | PD    | VDDQ33_EXT0 | GPIO             |
| 70         | XGPIO0     | I         | PD    | VDDQ33_EXT0 | GPIO             |
| 71         | XSPI1_MISO | I         | PD    | VDDQ33_EXT0 | SPI              |
| 72         | XSPI1_CLK  | I         | PD    | VDDQ33_EXT0 | SPI              |
| 73         | XSPI1_MOSI | I         | PD    | VDDQ33_EXT0 | SPI              |
| 74         | XSPI1_CSN  | I         | PD    | VDDQ33_EXT0 | SPI              |
| 75         | XGPIO27    | I         | PD    | VDDQ33_EXT0 | GPIO             |
| 76         | GND        | -         | -     | -           | GND              |

## Note:

- \* Default setting after reset
- I/O pad type definition - I:input, O:output, I/O:input/output
- Internal pull up/pull down definition - PU:pull-up, PD:pull-down, N:no pull

## MODULE EDGE PINOUT BY FUNCTION

### ADC INTERFACE

Table 2. ADC Interface

| Pad Number | Pad Name   | I/O Type | PU/PD | Power       | Default Function |
|------------|------------|----------|-------|-------------|------------------|
| 14         | XADC0AIN_1 | -        | -     | AVDD18_ADC0 | XADC0AIN_1       |
| 15         | XADC0AIN_0 | -        | -     | AVDD18_ADC0 | XADC0AIN_0       |
| 16         | XADC0AIN_2 | -        | -     | AVDD18_ADC0 | XADC0AIN_2       |
| 17         | XADC0AIN_3 | -        | -     | AVDD18_ADC0 | XADC0AIN_3       |

### DEBUG INTERFACE

Table 3. Debug Interface

| Pad Number | Pad Name     | I/O Type | PU/PD | Power       | Default Function |
|------------|--------------|----------|-------|-------------|------------------|
| 22         | XJTAG_TMS    | I        | PU    | VDDQ33_EXT1 | XJTAG_TMS        |
| 23         | XJTAG_TDI    | I        | PU    | VDDQ33_EXT1 | XJTAG_TDI        |
| 24         | XJTAG_TCK    | I        | PD    | VDDQ33_EXT1 | XJTAG_TCK        |
| 25         | XJTAG_TDO    | I        | PD    | VDDQ33_EXT1 | XJTAG_TDO        |
| 26         | XJTAG_TRST_N | I        | PD    | VDDQ33_EXT1 | XJTAG_TRST_N     |
| 37         | XDEBUG_TXD   | I        | PD    | VDDQ33_EXT1 | XDEBUG_TXD       |
| 38         | XDEBUG_RXD   | I        | PD    | VDDQ33_EXT1 | XDEBUG_RXD       |

### I<sup>2</sup>C INTERFACE

Table 4. I<sup>2</sup>C Interface

| Pad Number | Pad Name  | I/O Type | PU/PD | Power       | Default Function |
|------------|-----------|----------|-------|-------------|------------------|
| 33         | XI2C0_SCL | I        | PD    | VDDQ33_EXT1 | XI2C0_SCL        |
| 34         | XI2C0_SDA | I        | PD    | VDDQ33_EXT1 | XI2C0_SDA        |
| 35         | XI2C1_SCL | I        | PD    | VDDQ33_EXT1 | XI2C1_SCL        |
| 36         | XI2C1_SDA | I        | PD    | VDDQ33_EXT1 | XI2C1_SDA        |

### INT INTERFACE

Table 5. Interrupt Interface

| Pad Number | Pad Name | I/O Type | PU/PD | Power       | Default Function |
|------------|----------|----------|-------|-------------|------------------|
| 28         | XEINT_0  | I        | PD    | VDDQ33_EXT1 | XEINT_0          |
| 29         | XEINT_2  | I        | PD    | VDDQ33_EXT1 | XEINT_2          |
| 30         | XEINT_1  | I        | PD    | VDDQ33_EXT1 | XEINT_1          |

### POWER INTERFACE

| Pad Number | Pad Name     | I/O Type | PU/PD | Power | Default Function |
|------------|--------------|----------|-------|-------|------------------|
| 1          | GND          | -        | -     | -     | -                |
| 20         | GND          | -        | -     | -     | -                |
| 27         | 3V3_EXT_LDO2 | -        | -     | -     | -                |
| 32         | DC_5V_12V    | -        | -     | -     | -                |
| 76         | GND          | -        | -     | -     | -                |

## GPIO INTERFACE

Table 6. GPIO Interface

| Pad Number | Pad Name | I/O Type | PU/PD | Power           | Default Function |
|------------|----------|----------|-------|-----------------|------------------|
| 2          | XGPIO26  | I        | PD    | VDDQ33_EXT0     | XGPIO26          |
| 3          | XGPIO25  | I        | PD    | VDDQ33_EXT0     | XGPIO25          |
| 4          | XGPIO24  | I        | PD    | VDDQ33_EXT0     | XGPIO24          |
| 5          | XGPIO21  | I        | PD    | VDDQ33_EXT0     | XGPIO21          |
| 6          | XGPIO19  | I        | PD    | VDDQ33_EXT0     | XGPIO19          |
| 7          | XGPIO18  | I        | PD    | VDDQ33_EXT0     | XGPIO18          |
| 8          | XGPIO17  | I        | PD    | VDDQ33_EXT0     | XGPIO17          |
| 9          | XGPIO14  | I        | PD    | VDDQ33_EXT0     | XGPIO14          |
| 10         | XGPIO13  | I        | PD    | VDDQ33_EXT0     | XGPIO13          |
| 11         | XGPIO16  | I        | PD    | VDDQ33_EXT0     | XGPIO16          |
| 12         | XGPIO15  | I        | PD    | VDDQ33_EXT0     | XGPIO15          |
| 13         | XGPIO20  | I        | PD    | VDDQ33_EXT0     | XGPIO20          |
| 18         | XGPIO23  | I        | PD    | VDDQ1833_SDIO_0 | XGPIO23          |
| 19         | XGPIO22  | I        | PD    | VDDQ1833_SDIO_0 | XGPIO22          |
| 39         | XGPIO28  | I        | PD    | VDDQ33_EXT0     | XGPIO28          |
| 58         | XGPIO12  | I        | PD    | VDDQ33_EXT0     | XGPIO12          |
| 59         | XGPIO10  | I        | PD    | VDDQ33_EXT0     | XGPIO10          |
| 60         | XGPIO9   | I        | PD    | VDDQ33_EXT0     | XGPIO9           |
| 61         | XGPIO11  | I        | PD    | VDDQ33_EXT0     | XGPIO11          |
| 62         | XGPIO6   | I        | PD    | VDDQ33_EXT0     | XGPIO6           |
| 63         | XGPIO8   | I        | PD    | VDDQ33_EXT0     | XGPIO8           |
| 64         | XGPIO7   | I        | PD    | VDDQ33_EXT0     | XGPIO7           |
| 65         | XGPIO2   | I        | PD    | VDDQ33_EXT0     | XGPIO2           |
| 66         | XGPIO4   | I        | PD    | VDDQ33_EXT0     | XGPIO4           |
| 67         | XGPIO5   | I        | PD    | VDDQ33_EXT0     | XGPIO5           |
| 68         | XGPIO1   | I        | PD    | VDDQ33_EXT0     | XGPIO1           |
| 69         | XGPIO3   | I        | PD    | VDDQ33_EXT0     | XGPIO3           |
| 70         | XGPIO0   | I        | PD    | VDDQ33_EXT0     | XGPIO0           |
| 75         | XGPIO27  | I        | PD    | VDDQ33_EXT0     | XGPIO27          |

## PWM INTERFACE

Table 7. PWM Interface

| Pad Number | Pad Name   | I/O Type | PU/PD | Power       | Default Function |
|------------|------------|----------|-------|-------------|------------------|
| 40         | XPWMTOUT_4 | I        | PD    | VDDQ33_EXT0 | XPWMTOUT_4       |
| 41         | XPWMTOUT_1 | I        | PD    | VDDQ33_EXT0 | XPWMTOUT_1       |
| 42         | XPWMTOUT_0 | I        | PD    | VDDQ33_EXT0 | XPWMTOUT_0       |
| 43         | XPWMTOUT_5 | I        | PD    | VDDQ33_EXT0 | XPWMTOUT_5       |
| 44         | XPWMTOUT_2 | I        | PD    | VDDQ33_EXT0 | XPWMTOUT_2       |
| 45         | XPWMTOUT_3 | I        | PD    | VDDQ33_EXT0 | XPWMTOUT_3       |

## RESET INTERFACE

Table 8. Reset Interface

| Pad Number | Pad Name | I/O Type | PU/PD | Power       | Default Function |
|------------|----------|----------|-------|-------------|------------------|
| 21         | XRESET_N | I        | -     | VDDQ33_EXT1 | XRESET_N         |
| 31         | PWR_RST  | -        | -     | -           | -                |

## SPI INTERFACE

Table 9. SPI Interface

| Pad Number | Pad Name   | I/O Type | PU/PD | Power       | Default Function |
|------------|------------|----------|-------|-------------|------------------|
| 48         | XSPIO_MISO | I        | PD    | VDDQ33_EXT0 | XSPIO_MISO       |
| 49         | XSPIO_CSN  | I        | PD    | VDDQ33_EXT0 | XSPIO_CSN        |
| 50         | XSPIO_MOSI | I        | PD    | VDDQ33_EXT0 | XSPIO_MOSI       |
| 51         | XSPIO_CLK  | I        | PD    | VDDQ33_EXT0 | XSPIO_CLK        |
| 71         | XSPI1_MISO | I        | PD    | VDDQ33_EXT0 | XSPI1_MISO       |
| 72         | XSPI1_CLK  | I        | PD    | VDDQ33_EXT0 | XSPI1_CLK        |
| 73         | XSPI1_MOSI | I        | PD    | VDDQ33_EXT0 | XSPI1_MOSI       |
| 74         | XSPI1_CSN  | I        | PD    | VDDQ33_EXT0 | XSPI1_CSN        |

## UART INTERFACE

Table 10. UART Interface

| Pad Number | Pad Name   | I/O Type | PU/PD | Power       | Default Function | Comment               |
|------------|------------|----------|-------|-------------|------------------|-----------------------|
| 46         | XUART0_TXD | -        | -     | -           | XUART0_TXD       | Through Level Shifter |
| 47         | XUART0_RXD | -        | -     | -           | XUART0_RXD       | Through Level Shifter |
| 52         | XUART1_TXD | I        | PD    | VDDQ33_EXT0 | XUART1_TXD       | -                     |
| 53         | XUART1_RXD | I        | PD    | VDDQ33_EXT0 | XUART1_RXD       | -                     |
| 54         | XUART2_RXD | I        | PD    | VDDQ33_EXT0 | XUART2_RXD       | -                     |
| 55         | XUART2_TXD | I        | PD    | VDDQ33_EXT0 | XUART2_TXD       | -                     |
| 56         | XUART3_RXD | I        | PD    | VDDQ33_EXT0 | XUART3_RXD       | -                     |
| 57         | XUART3_TXD | I        | PD    | VDDQ33_EXT0 | XUART3_TXD       | -                     |

# ELECTRICAL SPECIFICATIONS

## ABSOLUTE MAXIMUM RATING

Table 11. Absolute Maximum Ratings

| PAD Number                                      | Symbol           | Condition                                                         | Min  | Typ | Max  | Units |
|-------------------------------------------------|------------------|-------------------------------------------------------------------|------|-----|------|-------|
| PAD: [32]                                       | $V_{IN}$         | Input voltage $V_{IN}$ on the high efficiency step down converter | -    | -   | 20   | V     |
| PAD: [2-19], [21-26], [28-31], [33-45], [48-75] | $V_{undershoot}$ | Undershoot voltage for I/O                                        | -0.3 | -   | -    | V     |
| PAD: [31]                                       | PWR_RST          | -                                                                 | -0.3 | -   | 6    | V     |
| PAD: [46, 47]                                   | $V_{MAX}$        | Based on 3V3 I/O signalling                                       | -    | -   | 63.3 | V     |
|                                                 |                  | Continuous                                                        | -    | -   | 305  | mA    |
|                                                 | $I_{MAX}$        | Pulsed                                                            | -    | -   | 800  | mA    |

## DC ELECTRICAL CHARACTERISTICS

Table 12. I/O DC Electrical Characteristics (PAD: [2-13, 18, 19], [21-26], [28-31], [33-45], [48-75], I/O)

| Parameter                   |            | Condition                                       | Min                              | Typ    | Max  | Units   |         |
|-----------------------------|------------|-------------------------------------------------|----------------------------------|--------|------|---------|---------|
| Tolerant External Voltage   | $V_{TOL}$  | 3.3 Power Off and On                            | -                                | -      | 3.60 | V       |         |
| High-Level Input Voltage    |            |                                                 |                                  |        |      |         |         |
| CMOS Interface              | $V_{IH}$   |                                                 | 2.31                             | -      | 3.60 | V       |         |
| Low-Level Input Voltage     |            |                                                 |                                  |        |      |         |         |
| CMOS Interface              | $V_{IL}$   | $V_{DD}=3.30V$                                  | -0.30                            | -      | 0.70 | V       |         |
| Hysteresis Voltage          | $\Delta V$ |                                                 | 0.15                             | -      | -    | V       |         |
| High-Level Input Current    |            |                                                 |                                  |        |      |         |         |
| Input Buffer                | $I_{IH}$   | $V_{IN}=3.30V$                                  | $V_{DD}=3.30V$ Power On          | -3.00  | -    | 3.00    | $\mu A$ |
|                             |            |                                                 | $V_{DD}=3.30V$ Power Off & SNS=0 | -5.00  | -    | 5.00    | $\mu A$ |
| Input Buffer with Pull-Down |            | $V_{IN}=3.30V$                                  |                                  | 13     | 40   | 90      | $\mu A$ |
| Low-Level Input Current     |            |                                                 |                                  |        |      |         |         |
| Input Buffer                | $I_{IL}$   | $V_{IN}=0V$                                     | $V_{DD}=3.30V$ Power On and Off  | -3.00  | -    | 3.00    | $\mu A$ |
| Input Buffer with Pull-Down |            | $V_{IN}=0V$                                     | $V_{DD}=3.30V$                   | -13.00 | -    | -90.00  | $\mu A$ |
| Output High Voltage         | $V_{OH}$   | $I_{OH} = 2.0mA, 4.0mA, 8.0mA$ and $12.0mA$     | 2.64                             | -      | 3.30 | V       |         |
| Output Low Voltage          | $V_{OL}$   | $I_{OL} = -2.0mA, -4.0mA, -8.0mA$ and $-12.0mA$ | 0                                | -      | 0.66 | V       |         |
| Output Hi-Z Current         | $V_{OZ}$   |                                                 | -5                               | -      | 5    | $\mu A$ |         |
| Input Capacitance           | $C_{IN}$   | Any input and bi-directional buffers            | -                                | -      | 5    | pF      |         |

Table 13. I/O DC Electrical Characteristics (PAD: [14-17], ADC)

| Parameter                                    | Acronym   | Condition                            | Min  | Typ | Max  | Units   |
|----------------------------------------------|-----------|--------------------------------------|------|-----|------|---------|
| High Level Input Voltage                     | $V_{IH}$  | Guaranteed Logic High Level          | 1.26 | -   | 1.80 | V       |
| Low Level Input Voltage                      | $V_{IL}$  | Guaranteed Logic Low Level           | 0    | -   | 0.54 | V       |
| Output High Voltage                          | $V_{OH}$  | $I_{OH}=2mA, 4mA, 8mA$ and $12mA$    | 1.44 | -   | 1.80 | V       |
| Output Low Voltage                           | $V_{OL}$  | $I_{OL}=2mA, 4mA, 8mA$ and $12mA$    | 0    | -   | 0.36 | V       |
| Input Pull-Up Resistor Current               | $I_{RPU}$ | $V_{PAD}=0$                          | 15   | -   | 77   | $\mu A$ |
| Input Pull-Down Resistor Current             | $I_{RPD}$ | $V_{PAD}=1.80$                       | 17   | -   | 77   | $\mu A$ |
| Input Hysteresis                             | $V_H$     | -                                    | 0.18 | -   | -    | V       |
| Input Leakage Current for Non Tolerant Cells | $I_{PAD}$ | $D_{VDD}=1.80, V_{PAD}=0$ or $1.80V$ | -6   | -   | +6   | $\mu A$ |
| Off State Leakage Current                    | $I_{OZ}$  | $D_{VDD}=1.80, V_{PAD}=0$ or $1.80V$ | -6   | -   | +6   | $\mu A$ |

Table 14. Recommended Operating Conditions

| Parameter                     | Symbol         | Min  | Typ | Max   | Units |
|-------------------------------|----------------|------|-----|-------|-------|
| Main Power Supply: PAD: [32]  | DC_5V_12V      | 4.50 | -   | 18.00 | V     |
| Maximum Operating Temperature | T <sub>c</sub> | -20  | -   | 85    | °C    |

Table 15. GPIO Signal Drive Strength

| State | Currents: Max conditions V <sub>DD</sub> =3.30V | Units |
|-------|-------------------------------------------------|-------|
| 0     | 2                                               | mA    |
| 1     | 4                                               | mA    |
| 2     | 8 (Default)                                     | mA    |
| 3     | 12                                              | mA    |

## ESD RATINGS

Table 16. ESD Ratings

| Parameter                                   | Min  | Typ | Max | Units |
|---------------------------------------------|------|-----|-----|-------|
| ESD stress voltage Human Body Model (JEDEC) | -1.0 | -   | 1.0 | kV    |
| ESD stress voltage Charged Device Model     | -    | 250 | -   | V     |

## AC ELECTRICAL CHARACTERISTICS

Table 17. Level Shifter AC Electrical Characteristics

| PAD Number    | Symbol                         | Condition                    | Min                                                 | Typ | Max | Units |    |
|---------------|--------------------------------|------------------------------|-----------------------------------------------------|-----|-----|-------|----|
| PAD: [46, 47] | <b>Dynamic Characteristics</b> |                              |                                                     |     |     |       |    |
|               | C <sub>ISS</sub>               | Input Capacitance            | V <sub>DS</sub> =25V, f=1.0MHz, V <sub>GS</sub> =0V | -   | -   | 50    | pF |
|               | C <sub>OSS</sub>               | Output Capacitance           |                                                     | -   | -   | 25    | pF |
|               | C <sub>RSS</sub>               | Reverse Transfer Capacitance |                                                     | -   | -   | 5     | pF |

## RF ELECTRICAL CHARACTERISTICS

Table 18. Tx Performance Characteristics

| Parameter          | Min  | Typ | Max  | Units |
|--------------------|------|-----|------|-------|
| RF frequency range | 2412 | -   | 2472 | GHz   |
| 11b (1-11Mbps)     | -    | 16  | -    | dBm   |
| 11g (6-54Mbps)     | -    | 14  | -    | dBm   |
| 11n, HT20 (MCS0-7) | -    | 12  | -    | dBm   |

Table 19. Rx Performance Characteristics

| Parameter          | Min  | Typ   | Max  | Units |
|--------------------|------|-------|------|-------|
| RF frequency range | 2412 | -     | 2472 | GHz   |
| 11b (1Mbps)        | -    | -97.2 | -    | dBm   |
| 11b (11Mbps)       | -    | -89.1 | -    | dBm   |
| 11g (6Mbps)        | -    | -94.1 | -    | dBm   |
| 11g (54Mbps)       | -    | -76.2 | -    | dBm   |
| 11n, HT20 (MCS0)   | -    | -93.9 | -    | dBm   |
| 11n, HT20 (MCS07)  | -    | -73.8 | -    | dBm   |



# MECHANICAL SPECIFICATIONS

Figure 4 shows the mechanical dimensions of the ARTIK 053 Module. All dimensions are in mm.

**Note:** The top layer "NO PCB ROUTING" gray areas are to prevent any shorts between exposed vias or traces and unused ARTIK 053 Module pads.

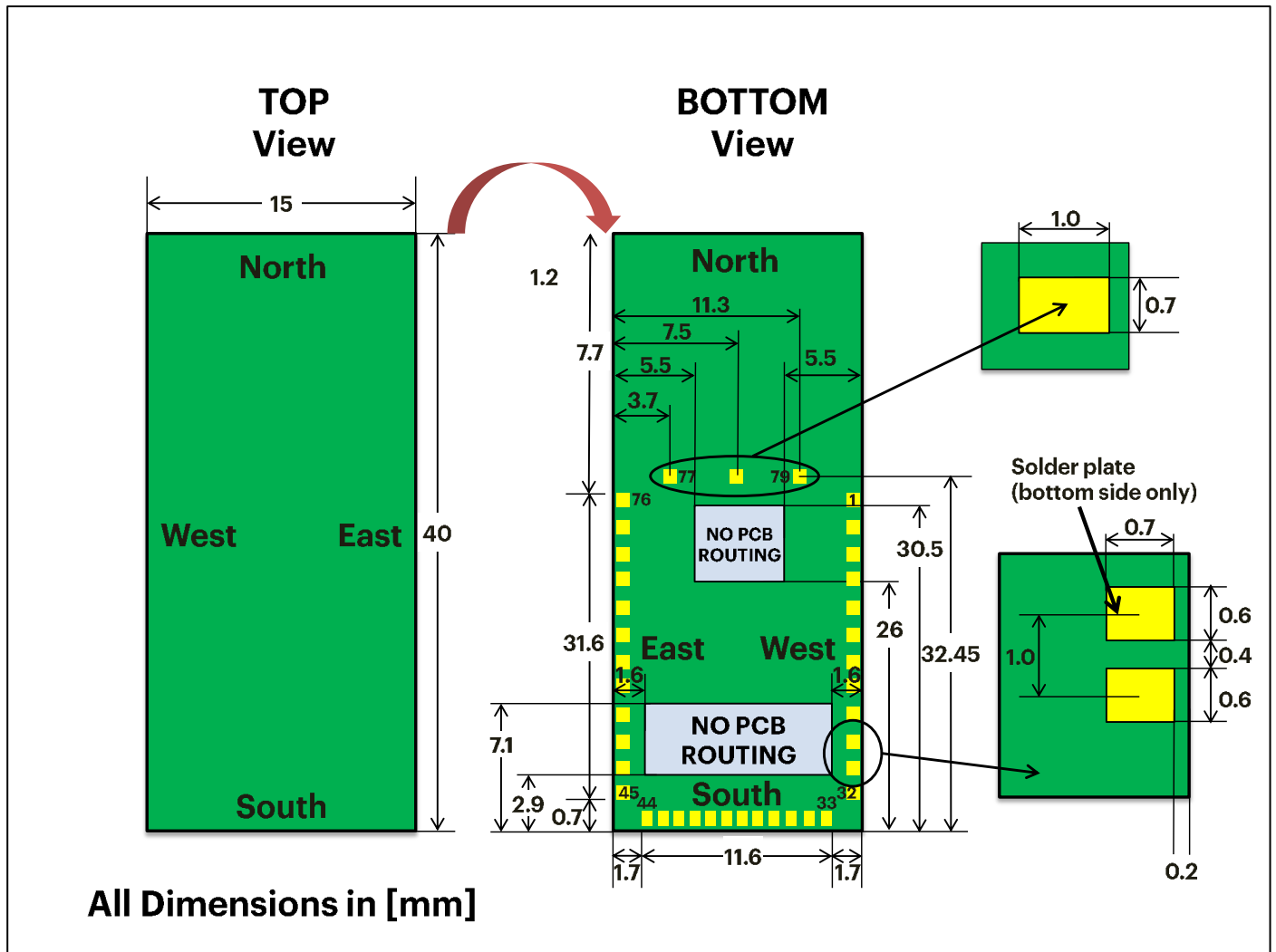


Figure 4. ARTIK 053 Module Mechanical Dimensions

## MODULE ANTENNA PLACEMENT REQUIREMENTS

The ARTIK 053 Module has an integrated on-module antenna. [Figure 5](#) describes the precise restrictions on location that must be accounted for when placing the ARTIK 053 Module on your native PCB design. In addition please adhere to the following guidelines:

- Avoid severe WiFi radiation loss by allocating at least a 5x6.7mm “No PCB Routing” area (all layers) on either side of the ARTIK 053 Module, next to the on-module antenna.
- Locate the antenna area at the edge of your PCB board, and as far away from other electronics as possible.
- See [Figure 4](#) for additional routing restrictions.

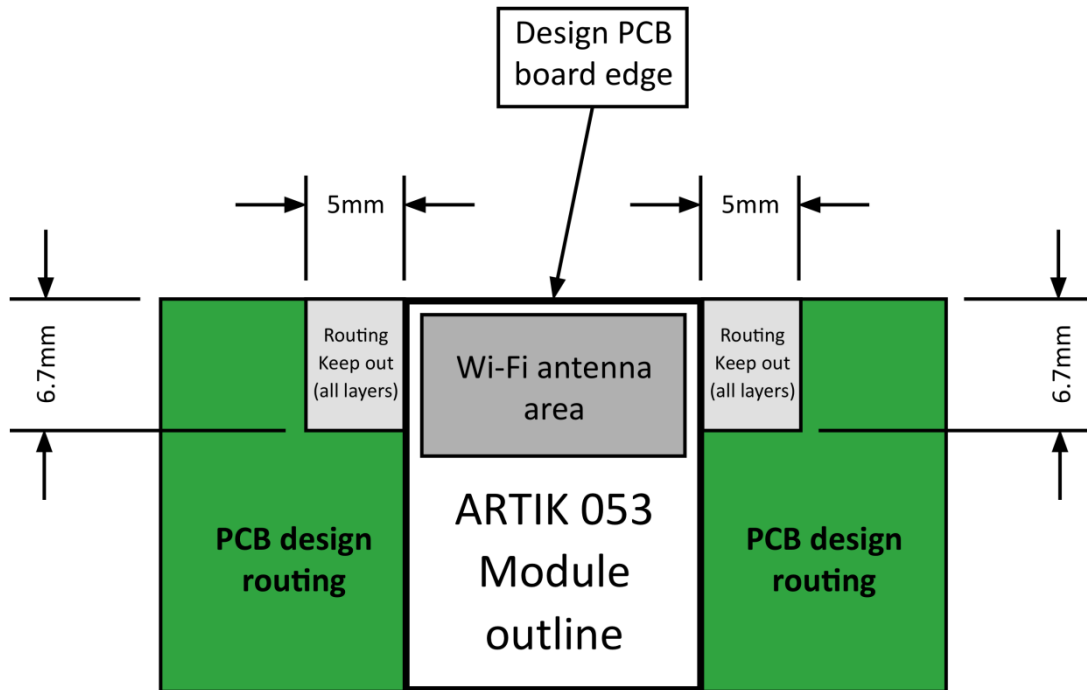


Figure 5. Module Placement Restrictions

# CERTIFICATION

## FCC REGULATORY DISCLOSURES

This device complies with Part 15 of the FCC`s Rules. Operation is subject to the following two Conditions: (1) This device may not cause harmful interference, and (2) This device must accept any interference received, including interference that may cause undesirable operation.

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/ TV technician for help.

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with a minimum distance of 20cm between the transmitter's radiating structure(s) and the body of the user or nearby persons.

This module is intended for OEM integration. The OEM integrator is responsible for FCC compliance and compliance with all applicable regulations including those for modular transmitters 47 C.F.R. 15.212. The OEM product must comply with all applicable labeling requirements including those contained in 15 C.F.R. 15.19. The OEM is solely responsible for certification and testing and labeling of its own products. In addition to any independently required labels, the OEM shall also affix to the outside of a device into which the module is installed a label referring to the enclosed module. This exterior label should be prepared in a legible font and permanently affixed and using the wording "Contains Transmitter Module FCCID: A3LCWAM210S."

The OEM is required to ensure that the end product integrates this module so as to maintain a minimum distance of 20 cm between the equipment's radiating structure(s) and the body of the user or nearby persons. The OEM shall also advise its end user of this requirement as required by applicable rules.

The OEM shall require that the end user of its product be informed that the FCC radio frequency exposure guidelines for an uncontrolled environment can be satisfied. The OEM shall further inform its end user that any change or modifications to this module not expressly approved by the manufacturer will void the warranty and the users' authority to operate the equipment.

## INDUSTRY CANADA REGULATORY DISCLOSURES

### Industry Canada Statement

This device complies with Industry Canada license-exempt RSS standard(s). Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

*Cet appareil est conforme avec Industrie Canada exempts de licence standard RSS (s). L'opération est soumise aux deux conditions suivantes:(1) cet appareil ne peut causer d'interférences, et (2) cet appareil doit accepter toute interférence, y compris les interférences qui peuvent causer un mauvais fonctionnement de l'appareil.*

### Industry Canada Radiation Exposures Statement and Limitations on Use

This equipment complies with IC RSS-102 radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20 cm between the radiator and your body. This equipment should be installed and must not be co-located or operating in conjunction with any other antenna or transmitter.

In the United States and Canada, only Channel 1~11 can be operated and these channel assignments deal only with the 2.4 GHz range.

The end product must be labeled to display the Industry Canada certification number of the module

**Contains transmitter module IC: 649E-CWAM210S**

Le dispositif d'accueil doivent être étiquetés pour afficher le numéro de certification d'Industrie Canada du module.

**Contient module émetteur IC : 649E-CWAM210S**

## EU REGULATORY DISCLOSURES

### CE Statement

*The following statement must be supplied with each product but can be printed in the user manual, the packaging, or provided as a separated leaflet.*

Hereby, Samsung declares that this IoT Module is in compliance with the essential requirements and other relevant provisions of Article 3 of the R&TTE Directive 1999/5/EC, 2004/108/EC and RoHS directive 2011/65/EU.

“The declaration of conformity may be consulted at [www.artik.io/certification](http://www.artik.io/certification)”

The OEM is required to ensure that the end product integrates this module so as to maintain a minimum distance of 20 cm between the equipment's radiating structure(s) and the body of the user or nearby persons. The OEM shall also advise its end user of this requirement as required by applicable rules.

## ORDERING INFORMATION

| Type             | Order Number  | Description          |
|------------------|---------------|----------------------|
| ARTIK 053 Module | SIP-0P5WRS301 | One ARTIK 053 Module |

For volume ordering of evaluation kits, please contact a sales representative in your area or visit <https://www.artik.io/contact-us/>.

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