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FAIRCHILD SEMICONDUCTOR®

November 2012

FL6300A
Quasi-Resonant Current Mode PWM Controller for Lighting

Features

- High-Voltage Startup
- Quasi-Resonant Operation
- Cycle-by-Cycle Current Limiting
- Peak-Current-Mode Control
- Leading-Edge Blanking (LEB)
- Internal Minimum t_{OFF}
- Internal 5 ms Soft-Start
- Over-Power Compensation
- GATE Output Maximum Voltage
- Auto-Recovery Over-Current Protection (FB Pin)
- Auto-Recovery Open-Loop Protection (FB Pin)
- Latch Protection V_{DD} Pin and Output Voltage (DET Pin) OVP
- Frequency Operation Below 100 kHz

Applications

- General LED Lighting
- Industrial, Commercial, and Residential Fixtures
- Outdoor Lighting: Street, Roadway, Parking, Construction, and Ornamental LED Lighting Fixtures

Description

The FL6300A lighting power controller includes a highly integrated PWM controller and provides several features to enhance the performance of flyback converters in medium- to high-power lumens applications.

The FL6300A is applied on quasi-resonant flyback converters, where maximum operating frequency is limited to below 100 kHz. A built-in HV startup circuit can provide more startup current to reduce the startup time of the controller. Once the V_{DD} voltage exceeds the turn-on threshold voltage, the HV startup function is disabled to reduce power consumption. An internal valley voltage detector ensures that the power system operates at quasi-resonant operation over a wide-range of line voltage and load conditions, as well as reducing switching loss to minimize switching voltage on the drain of the power MOSFET.

To minimize standby power consumption and improve light-load efficiency, a proprietary Green-Mode function provides off-time modulation to decrease switching frequency and perform extended valley voltage switching to keep to a minimum switching pulse. The operating frequency is limited by minimum t_{OFF} time, which is 38 µs to 8 µs.

FL6300A also provides many protection functions. Pulse-by-pulse current limiting ensures the fixed-peak current-limit level, even when a short circuit occurs. Once an open-circuit failure occurs in the feedback loop, the internal protection circuit disables PWM output immediately. When V_{DD} drops below the turn-off threshold voltage, the controller disables PWM output. The gate output is clamped at 18 V to protect the power MOSFET from high gate-source voltage conditions. The minimum t_{OFF} time limit prevents the system frequency from being too high. When over-voltage protection (OVP) is triggered by DET or when internal over-temperature protection (OTP) is triggered, the power system enters Latch Mode until AC power is removed.

Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method
FL6300AMY	-40°C to +125°C	8-Lead, Small Outline Package (SOP)	Tape & Reel

Application Diagram

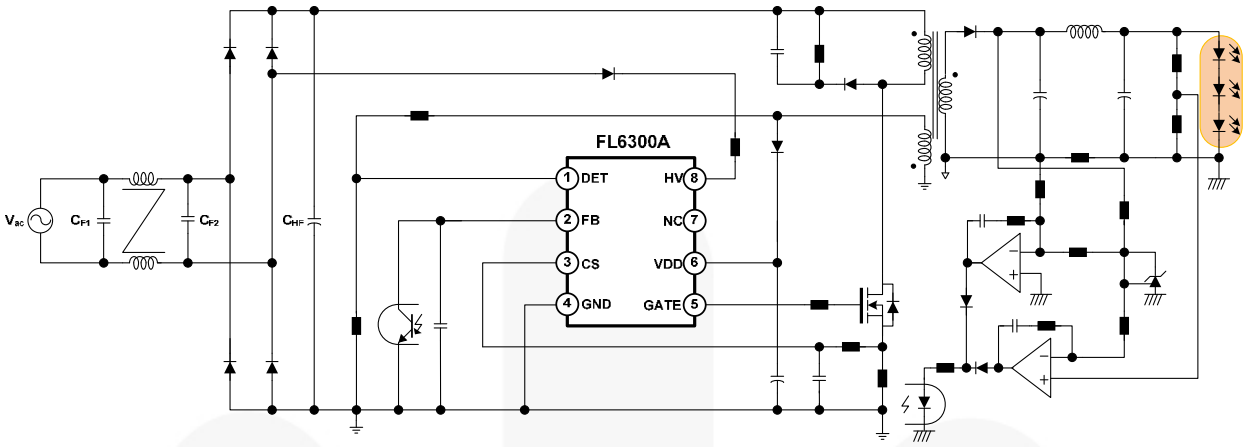


Figure 1. Typical Application Circuit for Flyback Converter

Internal Block Diagram

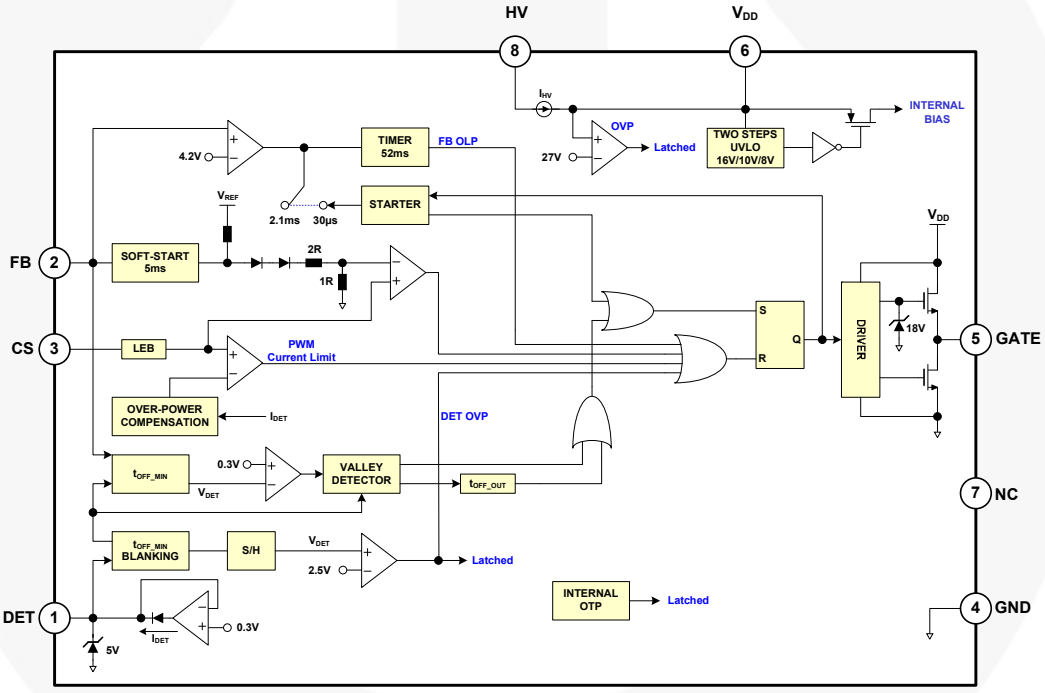
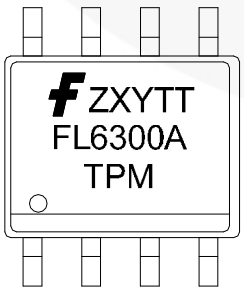


Figure 2. Functional Block Diagram

Marking Information



: Fairchild Logo
Z: Plant Code
X: Year Code
Y: Week Code
TT: Die Run Code
T: Package Type (M = SOP)
P: Y = Green Package
M: Manufacture Flow Code

Figure 3. Marking Diagram

Pin Configuration

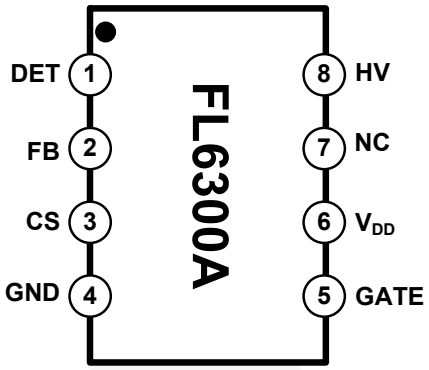


Figure 4. Pin Assignments

Pin Definitions

Pin #	Name	Description
1	DET	This pin is connected to an auxiliary winding of the transformer via resistors of the divider for the following purposes: – Generates a zero-current detection (ZCD) signal once the secondary-side switching current falls to zero. – Produces an offset voltage to compensate the threshold voltage of the peak current limit to provide a constant power limit. The offset is generated in accordance with the input voltage when PWM signal is enabled. – Detects the valley voltage of the switching waveform to achieve the valley voltage switching and minimize the switching losses. A voltage comparator and a 2.5 V reference voltage develop an output OVP protection. The ratio of the divider determines what output voltage to stop gate, as an optical coupler and secondary shunt regulator are used.
2	FB	The feedback pin should to be connected to the output of the error amplifier for achieving the voltage control loop. The FB pin should be connected to the output of the optical coupler if the error amplifier is equipped at the secondary-side of the power converter. For primary-side control applications, FB is applied to connect a RC network to the ground for feedback-loop compensation. The input impedance of this pin is a 5 kΩ equivalent resistance. A one-third (1/3) attenuator connected between the FB and the PWM circuit is used for the loop-gain attenuation. FL6300A performs an open-loop protection (OLP) once the FB voltage is higher than a threshold voltage (around 4.2 V) for more than 55ms.
3	CS	Input to the comparator of the over-current protection. A resistor senses the switching current and the resulting voltage is applied to this pin for the cycle-by-cycle current limit.
4	GND	The power ground and signal ground. A 0.1 µF decoupling capacitor placed between V_{DD} and GND is recommended.
5	GATE	Totem-pole output generates the PWM signal to drive the external power MOSFET. The clamped gate output voltage is 18 V.
6	V_{DD}	Power supply. The threshold voltages for startup and turn-off are 16 V and 10 V, respectively. The startup current is less than 20 µA and the operating current is lower than 4.5 mA.
7	NC	No connect
8	HV	High-voltage startup

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit
V_{VDD}	DC Supply Voltage		30	V
V_{HV}	HV		500	V
V_H	GATE	-0.3	25.0	V
V_L	V_{FB}, V_{CS}, V_{DET}	-0.3	7.0	V
P_D	Power Dissipation		400	mW
T_J	Operating Junction Temperature		+150	°C
T_{STG}	Storage Temperature Range	-55	+150	°C
T_L	Lead Temperature (Soldering 10 Seconds)		+270	°C
ESD	Human Body Model, JEDEC:JESD22-A114		3.0	KV
	Charged Device Model, JEDEC:JESD22-C101		1.5	

Notes:
1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device.
2. All voltage values, except differential voltages, are given with respect to GND pin.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
T_A	Operating Ambient Temperature	-40	+125	°C

Electrical Characteristics

Unless otherwise specified, V_{DD}=10~25 V, T_A=-40°C~125°C (T_A=T_J).

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD} Section						
V_{OP}	Continuously Operating Voltage				25	V
V_{DD-ON}	Turn-On Threshold Voltage		15	16	17	V
$V_{DD-PWM-OFF}$	PWM Off Threshold Voltage		9	10	11	V
V_{DD-OFF}	Turn-Off Threshold Voltage		7	8	9	V
I_{DD-ST}	Startup Current	V_{DD}=V_{DD-ON} -0.16 V GATE Open		10	20	µA
I_{DD-OP}	Operating Current	V_{DD}=15 V, f_S=60 kHz, C_L=2 nF		4.5	5.5	mA
$I_{DD-GREEN}$	Green-Mode Operating Supply Current (Average)	V_{DD}=15 V, f_S=2 kHz, C_L=2 nF			3.5	mA
$I_{DD-PWM-OFF}$	Operating Current at PWM-Off Phase	V_{DD}=$V_{DD-PWM-OFF}$-0.5 V	70	80	90	µA
V_{DD-OVP}	V_{DD} Over-Voltage Protection (Latch-Off)		26	27	28	V
$t_{VDD-OVP}$	V_{DD} OVP Debounce Time		100	150	200	µs
$I_{DD-LATCH}$	V_{DD} OVP Latch-Up Holding Current	V_{DD}=5 V		42		µA
HV Startup Current Source Section						
V_{HV-MIN}	Minimum Startup Voltage on Pin HV				50	V
I_{HV}	Supply Current Drawn from Pin HV	V_{AC}=90 V (V_{DC}=120 V) V_{DD}=0 V	1.5		4.0	mA
I_{HV-LC}	Leakage Current After Startup	HV=500 V, V_{DD}=V_{DD-OFF} +1 V		1	20	µA
Feedback Input Section						
A_V	Input-Voltage to Current Sense Attenuation	A_V=$\Delta V_{CS}/\Delta V_{FB}$, 0<$V_{CS}$<0.9	1/2.75	1/3.00	1/3.25	V/V
Z_{FB}	Input Impedance		3	5	7	KΩ
I_{OZ}	Bias Current	FB=V_{OZ}		1.2	2.0	mA
V_{OZ}	Zero Duty Cycle Input Voltage		0.8	1.0	1.2	V
V_{FB-OLP}	Open-Loop Protection Threshold Voltage		3.9	4.2	4.5	V
t_{D-OLP}	Debounce Time for Open-Loop/Overload Protection		46	52	62	ms
t_{SS}	Internal Soft-Start Time			5		ms

Continued on the following page...

Electrical Characteristics (Continued)

Unless otherwise specified, V_{DD}=10~25 V, T_A=-40°C ~125°C (T_A=T_J).

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DET Pin OVP and Valley Detection Section						
$V_{DET-OVP}$	Comparator Reference Voltage		2.45	2.50	2.55	V
Av	Open-Loop Gain(3)			60		dB
Bw	Gain Bandwidth(3)			1		MHz
V_{V-HIGH}	Output High Voltage		4.5			V
V_{V-LOW}	Output Low Voltage				0.5	V
$t_{DET-OVP}$	Output OVP (Latched) Debounce Time		100	150	200	µs
$I_{DET-SOURCE}$	Maximum Source Current	V_{DET}=0 V			1	mA
$V_{DET-HIGH}$	Upper Clamp Voltage	I_{DET}=-1 mA			5	V
$V_{DET-LOW}$	Lower Clamp Voltage	I_{DET}=1 mA	0.1	0.3		V
$t_{VALLEY-DELAY}$	Delay Time from Valley Signal Detected to Output Turn-On(3)			200		ns
$t_{OFF-BNK}$	Leading-Edge-Blanking Time for DET when PWM MOS Turns Off(3)			4		µs
$t_{TIME-OUT}$	Time-Out After $t_{OFF-MIN}$			9		µs
Oscillator Section						
t_{ON-MAX}	Maximum On-Time		38	45	54	µs
$t_{OFF-MIN}$	Minimum Off-Time	$V_{FB} \geqq V_{N,}$		8		µs
		V_{FB}=V_G		38		
V_N	Beginning of Green-On Mode at FB Voltage Level		1.95	2.10	2.25	V
V_G	Beginning of Green-Off Mode at FB Voltage Level		1.0	1.2	1.4	V
ΔV_{FBG}	Green-Off Mode V_{FB} Hysteresis Voltage		0.05	0.10	0.20	V
$t_{STARTER}$	Start Timer (Time-Out Timer)	V_{FB}<V_G	1.8	2.1	2.4	ms
		V_{FB}>V_{FB-OLP}	25	30	45	µs
Output Section						
V_{OL}	Output Voltage Low	V_{DD}=15 V, I_O=150 mA			1.5	V
V_{OH}	Output Voltage High	V_{DD}=12 V, I_O=150 mA	7.5			V
t_R	Rising Time			145	200	ns
t_F	Falling Time			55	120	ns
V_{CLAMP}	Gate Output Clamping Voltage		16.7	18.0	19.3	V

Continued on the following page…

Electrical Characteristics (Continued)

Unless otherwise specified, V_{DD}=10~25 V, T_A=-40°C ~125°C (T_A=T_J).

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Current Sense Section						
t_{PD}	Delay to Output		20	150	200	ns
V_{LIMIT}	Limit Voltage on CS Pin for Over-Power Compensation	I_{DET} < 74.41 µA	0.82	0.85	0.88	V
		I_{DET}=550 µA	0.380	0.415	0.450	
V_{SLOPE}	Slope Compensation(3)	t_{ON}=45 µs		0.3		V
		t_{ON}=0 µs		0.1		
t_{BNK}	Leading-Edge-Blanking Time (MOS Turns ON)		525	625	725	ns
V_{CS-H}	V_{CS} Clamped High Voltage once CS Pin Floating	CS Pin Floating	4.5		5.0	V
t_{CS-H}	Delay Time Once CS Pin Floating	CS Pin Floating		150		µs
Internal Over-Temperature Protection Section						
T_{OTP}	Internal Threshold Temperature for OTP(3)			+140		°C
$T_{OTP-HYST}$	Hysteresis Temperature for Internal OTP(3)			+15		°C

Note:

3. This parameter, although guaranteed by design, is not tested in production.

Typical Performance Characteristics

Graphs are normalized at T_A=25°C.

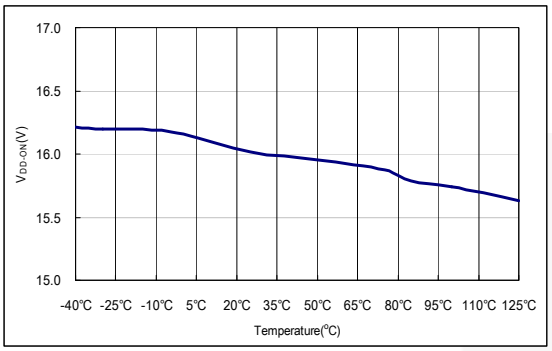


Figure 5. Turn-On Threshold Voltage

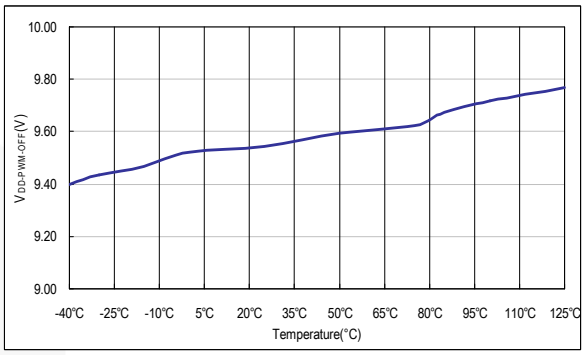


Figure 6. PWM-Off Threshold Voltage

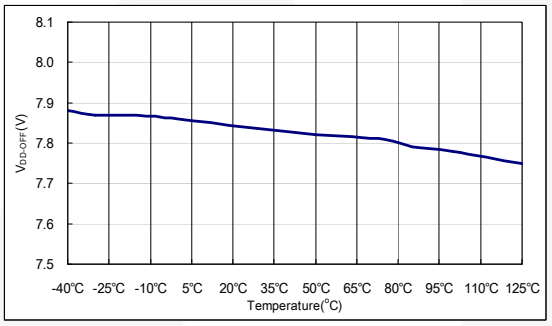


Figure 7. Turn-Off Threshold Voltage

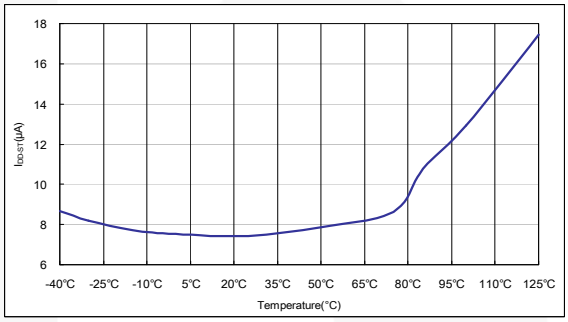


Figure 8. Startup Current

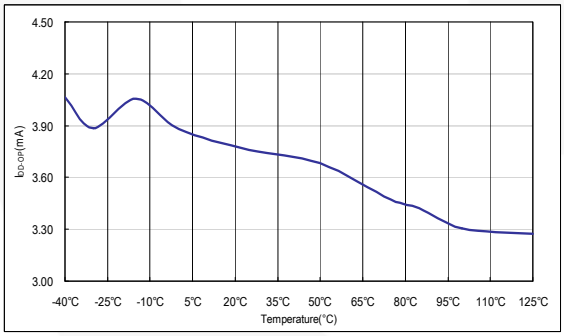


Figure 9. Operating Current

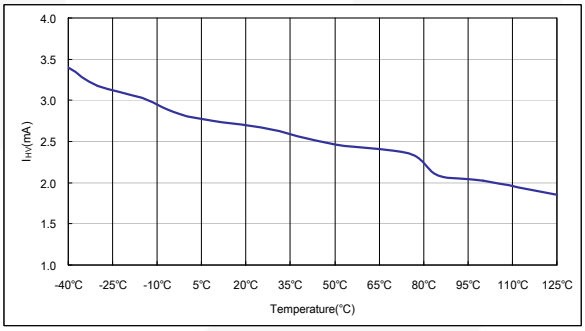


Figure 10. Supply Current Drawn From HV Pin

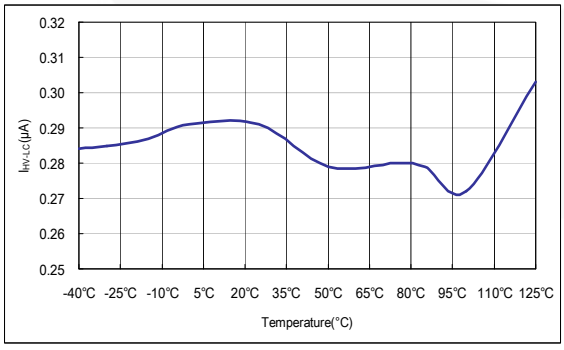


Figure 11. Leakage Current After Startup

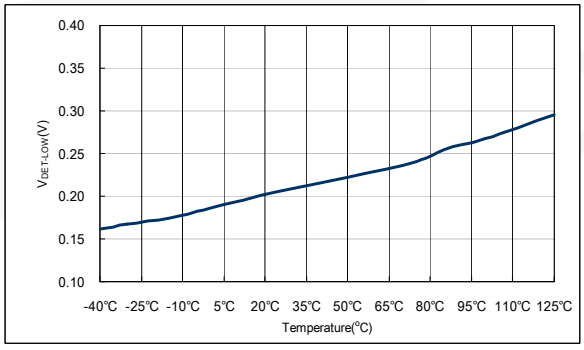


Figure 12. Lower Clamp Voltage

Typical Performance Characteristics (Continued)

These characteristic graphs are normalized at T_A = 25°C.

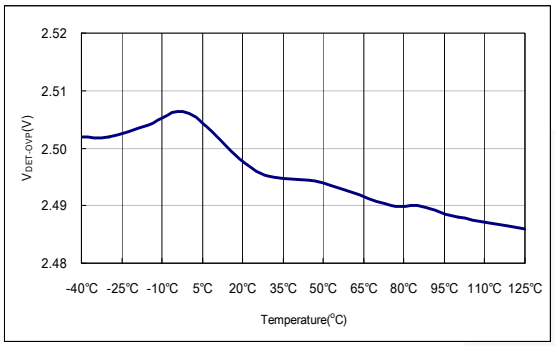


Figure 13. Comparator Reference Voltage

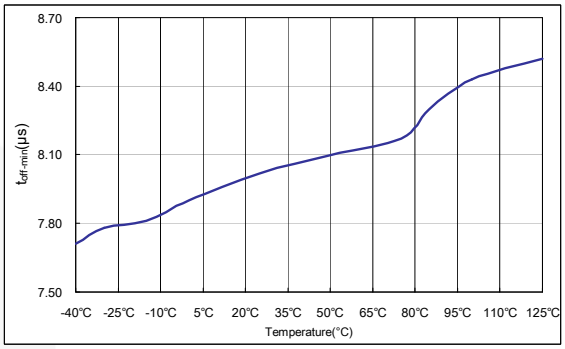


Figure 14. Minimum Off Time (V_{FB}>V_N)

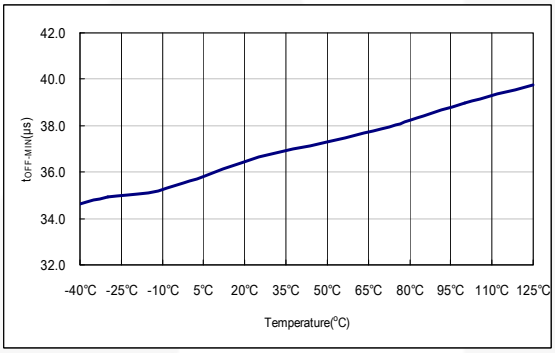


Figure 15. Minimum Off Time (V_{FB}=V_G)

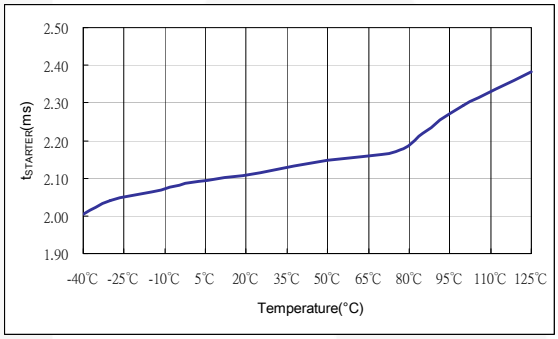


Figure 16. Start Timer (V_{FB}<V_G)

Operation Description

The FL6300A PWM controller integrates features to enhance the performance of flyback converters. An internal valley voltage detector ensures Quasi-Resonant (QR) operation across a wide range of line voltage.

Startup Current

For startup, the HV pin is connected to the line input or bulk capacitor through an external diode and resistor, R_{HV}, which are recommended as 1N4007 and 100 kΩ. Typical startup current drawn from the HV pin is 1.2 mA and it charges the hold-up capacitor through the diode and resistor. When the V_{DD} voltage level reaches V_{DD-ON}, the startup current switches off. At this point, the V_{DD} capacitor only supplies the FL6300A to maintain V_{DD} until the auxiliary winding of the main transformer provides the operating current.

Valley Detection

The DET pin is connected to an auxiliary winding of the transformer via resistors of the divider to generate a valley signal once the secondary-side switching current discharges to zero. It detects the valley voltage of the switching waveform to achieve the valley voltage switching. This ensures QR operation, minimizes switching losses, and reduces EMI. Figure 17 shows divider resistors R_{DET} and R_A. R_{DET} is recommended as 150 kΩ to 220 kΩ to achieve valley voltage switching. When V_{AUX} (in Figure 17) is negative, the DET pin voltage is clamped to 0.3 V.

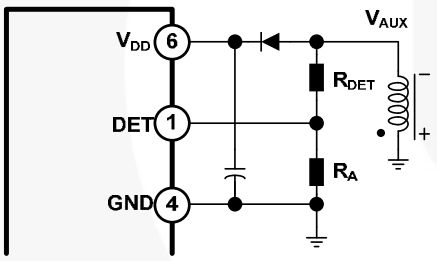


Figure 17. Valley Detect Section

The internal timer (minimum t_{OFF}) prevents gate retriggering within 8 µs after the gate signal going-LOW transition. The minimum t_{OFF} limit prevents system frequency being too high. Figure 18 shows a typical drain voltage waveform with first valley switching.

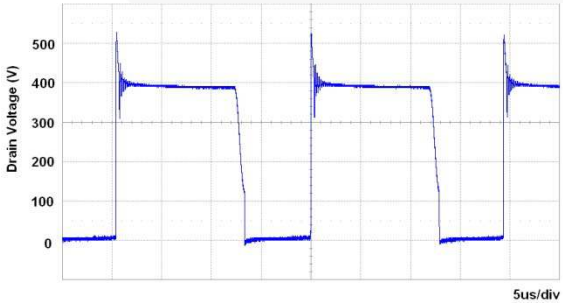


Figure 18. First Valley Switching

Green-Mode Operation

The proprietary green mode provides off-time modulation to linearly decrease the switching frequency under light-load conditions. V_{FB}, which is derived from the voltage feedback loop, is taken as the reference. In Figure 19, once V_{FB} is lower than V_N, $t_{OFF-MIN}$ increases linearly with lower V_{FB}. The valley voltage detection signal does not start until $t_{OFF-MIN}$ finishes. Therefore, the valley-detect circuit is active until $t_{OFF-MIN}$ finishes, which decreases the switching frequency and provides extended valley voltage switching. However, in very light-load condition, it might fail to detect the valley voltage after the $t_{OFF-MIN}$ expires. Under this condition, an internal $t_{TIME-OUT}$ signal initiates a new cycle after a 9 µs delay. Figure 20 and Figure 21 show the two conditions.

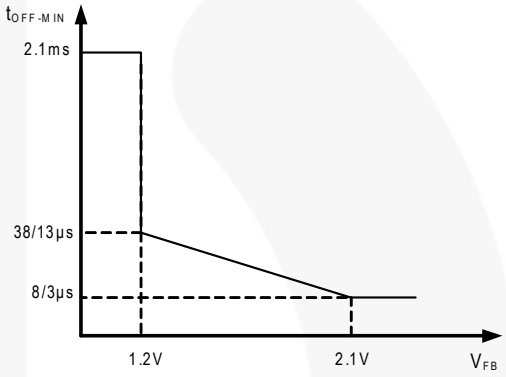


Figure 19. V_{FB} vs. $t_{OFF-MIN}$ Curve

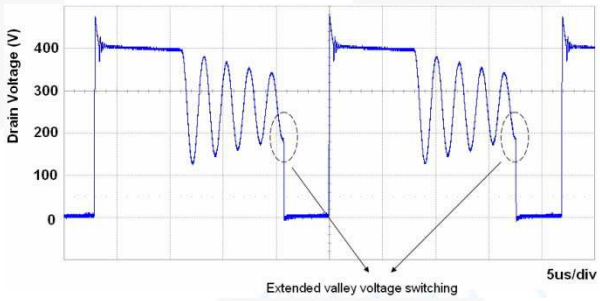


Figure 20. QR Operation in Extended Valley Voltage Detection Mode

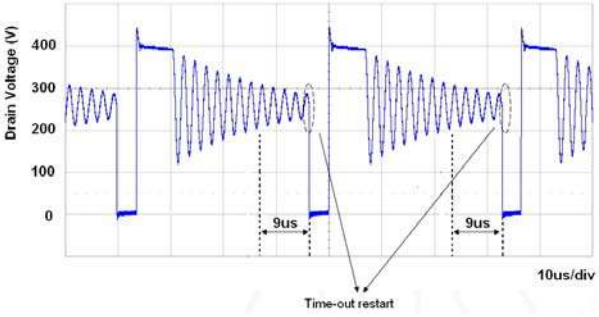


Figure 21. Internal $t_{TIME-OUT}$ Initiates New Cycle After Failure to Detect Valley Voltage

Current Sensing and PWM Current Limiting

Peak-current-mode control is utilized to regulate output voltage and provide pulse-by-pulse current limiting. The switch current is detected by a sense resistor into the CS pin. The PWM duty cycle is determined by this current-sense signal and V_{FB}. When the voltage on CS reaches around $V_{LIMIT}=(V_{FB}-1.2)/3$, the switch cycle is terminated immediately. V_{LIMIT} is internally clamped to a variable voltage around 0.85 V for output power limit.

Leading-Edge Blanking (LEB)

Each time the power MOFFET switches on, a turn-on spike occurs on the sense resistor. To avoid premature termination of the switching pulse, lead-edge blanking time is built in. During the blanking period, the current limit comparator is disabled; it cannot switch off the gate driver.

Under-Voltage Lockout (UVLO)

The turn-on, PWM-off, and turn-off thresholds are fixed internally at 16 V / 10 V / 8 V, respectively. During startup, the startup capacitor must be charged to 16 V through the startup resistor to enable the IC. The hold-up capacitor continues to supply V_{DD} until energy can be delivered from the auxiliary winding of the main transformer. V_{DD} must not drop below 10 V during this startup process. This UVLO hysteresis window ensures that hold-up capacitor is adequate to supply V_{DD} during startup.

Gate Output

The BiCMOS output stage is a fast totem-pole gate driver. Cross conduction has been avoided to minimize heat dissipation, increase efficiency, and enhance reliability. The output driver is clamped by an internal 18 V Zener diode to protect power MOSFET transistors against undesired over-voltage gate signals.

Over-Power Compensation

To compensate for the variation of a wide AC input range, the DET pin produces an offset voltage to compensate the threshold voltage of the peak current limit for a constant-power limit. The offset is generated in accordance with the input voltage when PWM signal is enabled. This results in a lower current limit at high-line inputs than low-line inputs. At fixed-load condition, the CS limit is higher when the value of R_{DET} is higher. R_{DET} also affects the H/L line constant power limit.

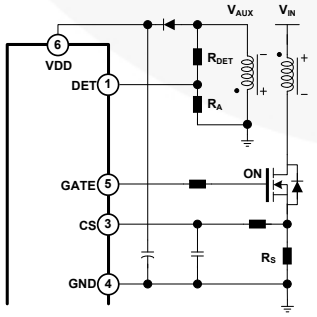


Figure 22. H/L Line Constant Power Limit Compensated by DET Pin

V_{DD} Over-Voltage Protection

V_{DD} over-voltage protection prevents damage due to abnormal conditions. Once the V_{DD} voltage is over the V_{DD} over-voltage protection voltage (V_{DD-OVP}) and lasts for t_{VDDOVP}, the PWM pulse is disabled until the V_{DD} voltage drops below the UVLO, then starts again.

Output Over-Voltage Protection

The output over-voltage protection works by the sampling voltage, as shown in Figure 23, after switch-off sequence. A 4 µs blanking time ignores the leakage inductance ringing. A voltage comparator and a 2.5 V reference voltage develop an output OVP protection. The ratio of the divider determines the sampling voltage of the stop gate, as an optical coupler and secondary shunt regulator are used. If the DET pin OVP is triggered, the power system enters latch-mode until AC power is removed.

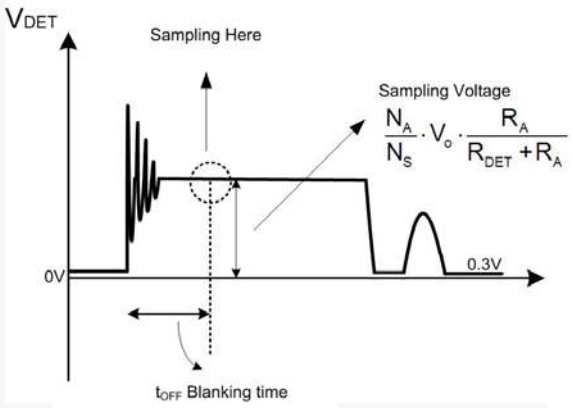


Figure 23. Voltage Sampled After 4 µs Blanking Time After Switch-Off Sequence

Short-Circuit and Open-Loop Protection

The FB voltage increases every time the output of the power supply is shorted or overloaded. If the FB voltage remains higher than a built-in threshold for longer than t_{D-OLP}, PWM output is turned off. As PWM output is turned-off, the supply voltage V_{DD} begins decreasing.

When V_{DD} goes below the PWM-off threshold of 10 V, V_{DD} decreases to 8 V, then the controller is totally shut down. V_{DD} is charged up to the turn-on threshold voltage of 16 V through the startup resistor until PWM output is restarted. This protection feature continues as long as the overloading condition persists. This prevents the power supply from overheating due to overloading.

Physical Dimensions

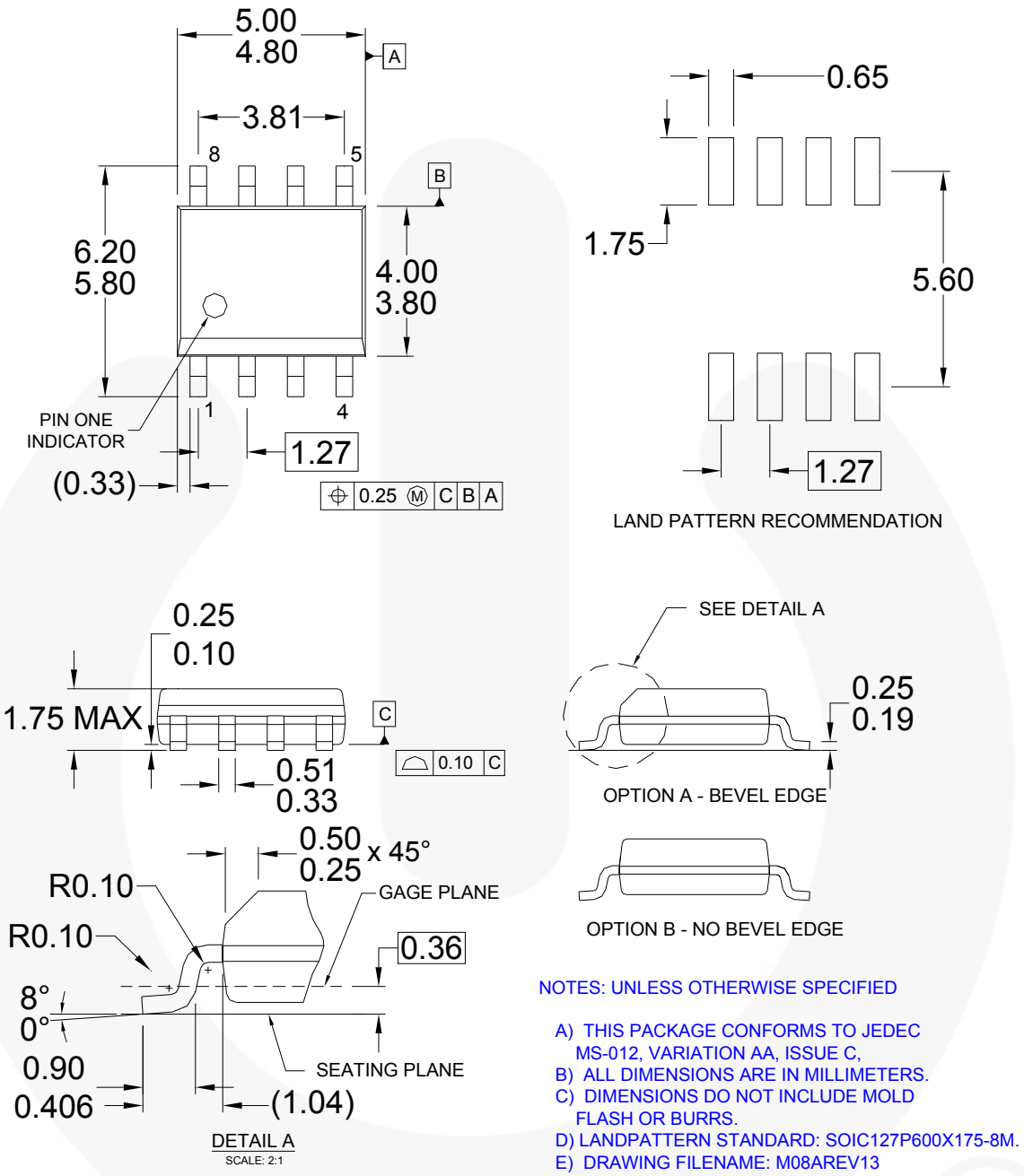


Figure 24. 8-Pin Small Outline Package (SOP)

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