Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

Quality Overview

*   ISO-9001
*   AS9120 certification
*   Qualified Manufacturers List (QML) MIL-PRF-35835
    *   Class Q Military
    *   **Class V Space Level**
*   Qualified Suppliers List of Distributors (QSLD)

    • Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

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FAIRCHILD

SEMICONDUCTOR ™

April 1988
Revised June 2002

74F182
Carry Lookahead Generator

General Description

The 74F182 is a high-speed carry lookahead generator. It is generally used with the 74F181 or 74F381 4-bit arithmetic logic units to provide high-speed lookahead over word lengths of more than four bits.

Features

■ Provides lookahead carries across a group of four ALUs

■ Multi-level lookahead high-speed arithmetic operation over long word lengths

Ordering Code:

| Order Number	Package Number	Package Description
74F182SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74F182PC (Note 1)	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Note 1: This device not available in Tape and Reel.

Logic Symbols
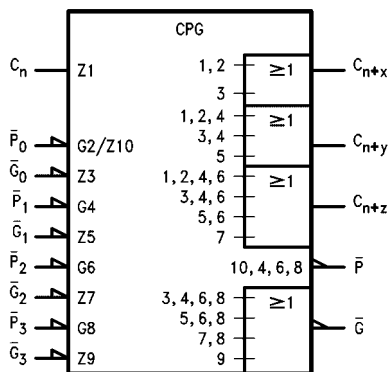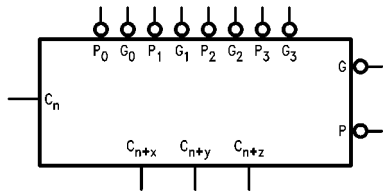
Connection Diagram

www.fairchildsemi.com
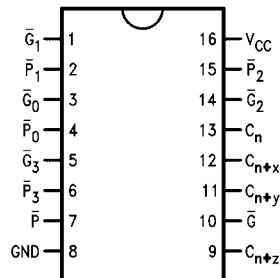
Unit Loading/Fan Out

Pin Names	Description	U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
C_n	Carry Input	1.0/2.0	20 µA/–1.2 mA
$\overline{G}_0, \overline{G}_2$	Carry Generate Inputs (Active LOW)	1.0/14.0	20 µA/–8.4 mA
$\overline{G}_1$	Carry Generate Input (Active LOW)	1.0/16.0	20 µA/–9.6 mA
$\overline{G}_3$	Carry Generate Input (Active LOW)	1.0/8.0	20 µA/–4.8 mA
$\overline{P}_0, \overline{P}_1$	Carry Propagate Inputs (Active LOW)	1.0/8.0	20 µA/–4.8 mA
$\overline{P}_2$	Carry Propagate Input (Active LOW)	1.0/6.0	20 µA/–3.6 mA
$\overline{P}_3$	Carry Propagate Input (Active LOW)	1.0/4.0	20 µA/–2.4 mA
$C_{n+x} - C_{n+z}$	Carry Outputs	50/33.3	–1 mA/20 mA
$\overline{G}$	Carry Generate Output (Active LOW)	50/33.3	–1 mA/20 mA
$\overline{P}$	Carry Propagate Output (Active LOW)	50/33.3	–1 mA/20 mA

Functional Description

The 74F182 carry lookahead generator accepts up to four pairs of Active LOW Carry Propagate ($\overline{P}_0$–$\overline{P}_3$) and Carry Generate ($\overline{G}_0$–$\overline{G}_3$) signals and an Active HIGH Carry input (C_n) and provides anticipated Active HIGH carries (C_{n+x}, C_{n+y}, C_{n+z}) across four groups of binary adders. The 74F182 also has Active LOW Carry Propagate ($\overline{P}$) and Carry Generate ($\overline{G}$) outputs which may be used for further levels of lookahead. The logic equations provided at the outputs are:

$$C_{n+x} = G_0 + P_0 C_n$$
$$C_{n+y} = G_1 + P_1 G_0 + P_1 P_0 C_n$$
$$C_{n+z} = G_2 + P_2 G_1 + P_2 P_1 G_0 + P_2 P_1 P_0 C_n$$
$$G = \overline{G}_3 + \overline{P}_3\,\overline{G}_2 + \overline{P}_3\,\overline{P}_2\,\overline{G}_1 + \overline{P}_3\,\overline{P}_2\,\overline{P}_1\,\overline{G}_0$$
$$P = \overline{P}_2\,\overline{P}_2\,\overline{P}_1\,\overline{P}_0$$

Also, the 74F182 can be used with binary ALUs in an active LOW or active HIGH input operand mode. The connections (Figure 1) to and from the ALU to the carry lookahead generator are identical in both cases. Carries are rippled between lookahead blocks. The critical speed path follows the circled numbers. There are several possible arrangements for the carry interconnects, but all achieve about the same speed. A 28-bit ALU is formed by dropping the last 74F181 or 74F381.
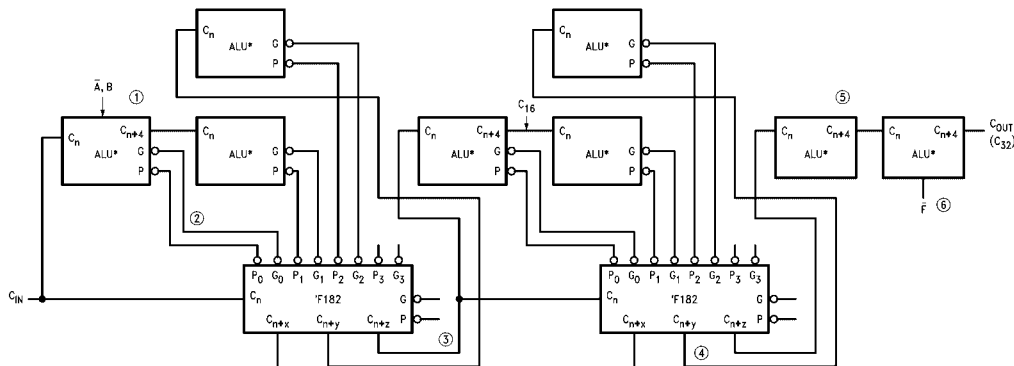

*ALUs may be either 74F181 or 74F381

FIGURE 1. 32-Bit ALU with Rippled Carry between 16-Bit Lookahead ALUs

Truth Table

			Inputs								Outputs		
C_n	$\overline{G}_0$	$\overline{P}_0$	$\overline{G}_1$	$\overline{P}_1$	$\overline{G}_2$	$\overline{P}_2$	$\overline{G}_3$	$\overline{P}_3$	C_{n+x}	C_{n+y}	C_{n+z}	$\overline{G}$	$\overline{P}$
X	H	H							L				
L	H	X							L				
X	L	X							H				
H	X	L							H				
X	X	X	H	H						L			
X	H	H	H	X						L			
L	H	X	H	X						L			
X	X	X	L	X						H			
X	L	X	X	L						H			
H	X	L	X	L						H			
X	X	X	X	X	H	H					L		
X	X	X	H	H	H	X					L		
X	H	H	H	X	H	X					L		
L	H	X	H	X	H	X					L		
X	X	X	X	X	L	X					H		
X	X	X	L	X	X	L					H		
X	L	X	X	L	X	L					H		
H	X	L	X	L	X	L					H		
	X		X	X	X	X	H	H				H	
	X		X	X	H	H	H	X				H	
	X		H	H	H	X	H	X				H	
	H		H	X	H	X	H	X				H	
	X		X	X	X	X	L	X				L	
	X		X	X	L	X	X	L				L	
	X		L	X	X	L	X	L				L	
	L		X	L	X	L	X	L				L	
		H		X		X		X					H
		X		H		X		X					H
		X		X		H		X					H
		X		X		X		H					H
		L		L		L		L					L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Logic Diagram
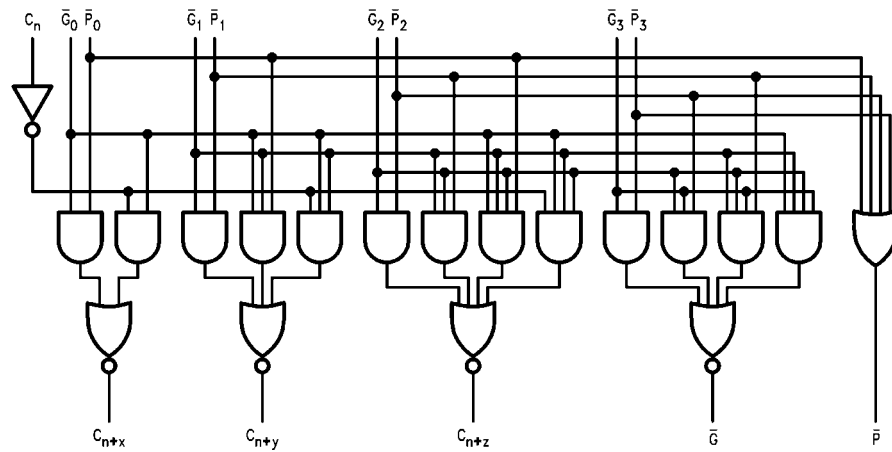
Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings(Note 2)

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 3)	−0.5V to +7.0V
Input Current (Note 3)	−30 mA to +5.0 mA
Voltage Applied to Output	
in HIGH State (with V_{CC} = 0V)	
Standard Output	−0.5V to V_{CC}
3-STATE Output	−0.5V to +5.5V
Current Applied to Output	
in LOW State (Max)	twice the rated I_{OL} (mA)
ESD Last Passing Voltage (Min)	4000V

Recommended Operating Conditions

Free Air Ambient Temperature	0°C to +70°C
Supply Voltage	+4.5V to +5.5V

Note 2: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

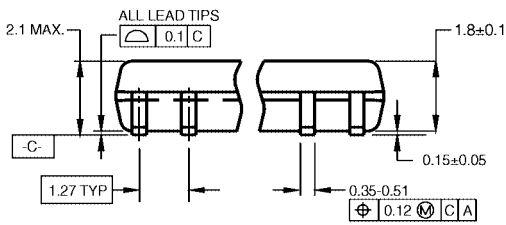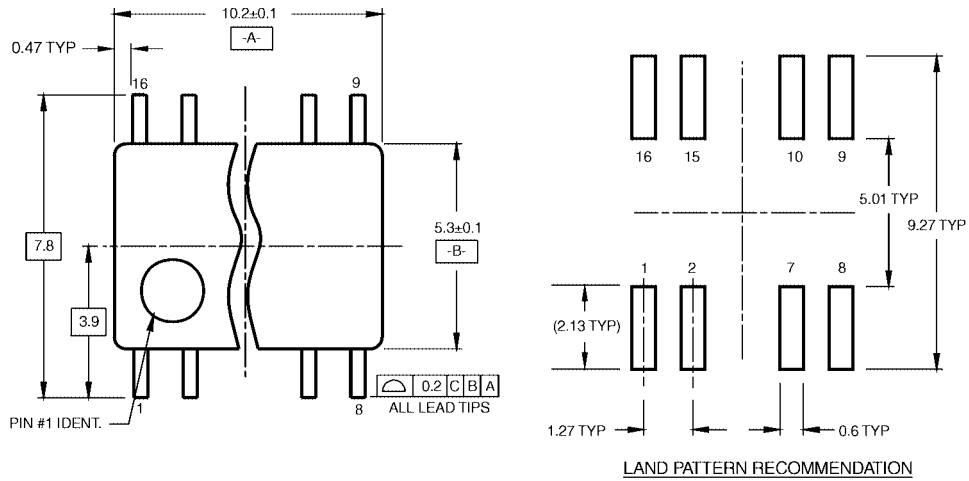**Note 3:** Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter		Min	Typ	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH	10% V_{CC}	2.5			V	Min	I_{OH} = −1 mA
	Voltage	5% V_{CC}	2.7					I_{OH} = −1 mA
V_{OL}	Output LOW	10% V_{CC}			0.5	V	Min	I_{OL} = 20 mA
	Voltage							
I_{IH}	Input HIGH				5.0	µA	Max	V_{IN} = 2.7V
	Current							
I_{BVI}	Input HIGH Current				7.0	µA	Max	V_{IN} = 7.0V
	Breakdown Test							
I_{CEX}	Output HIGH				50	µA	Max	V_{OUT} = V_{CC}
	Leakage Current							
V_{ID}	Input Leakage		4.75			V	0.0	I_{ID} = 1.9 µA
	Test							All Other Pins Grounded
I_{OD}	Output Leakage				3.75	µA	0.0	V_{IOD} = 150 mV
	Circuit Current							All Other Pins Grounded
I_{IL}	Input LOW				−1.2	mA	Max	V_{IN} = 0.5V (C_n)
	Current				−2.4			V_{IN} = 0.5V ($\overline{P}_3$)
					−3.6			V_{IN} = 0.5V ($\overline{P}_2$)
					−4.8			V_{IN} = 0.5V ($\overline{G}_3$, $\overline{P}_0$, $\overline{P}_1$)
					−8.4			V_{IN} = 0.5V ($\overline{G}_0$, $\overline{G}_2$)
					−9.6			V_{IN} = 0.5V ($\overline{G}_1$)
I_{OS}	Output Short-Circuit Current		−60		−150	mA	Max	V_{OUT} = 0V
I_{CCH}	Power Supply Current			18.4	28.0	mA	Max	V_O = HIGH
I_{CCL}	Power Supply Current			23.5	36.0	mA	Max	V_O = LOW

AC Electrical Characteristics

Symbol	Parameter	$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50$ pF			$T_A = -55°C$ to $+125°C$ $V_{CC} = +5.0V$ $C_L = 50$ pF		$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V$ $C_L = 50$ pF		Units
		Min	Typ	Max	Min	Max	Min	Max	
t_{PLH}	Propagation Delay	3.0	6.6	8.5	3.0	12.0	3.0	9.5	ns
t_{PHL}	C_n to C_{n+x}, C_{n+y}, C_{n+z}	3.0	6.8	9.0	3.0	11.0	3.0	10.0	
t_{PLH}	Propagation Delay	2.5	6.2	8.0	2.5	11.0	2.5	9.0	
t_{PHL}	$\overline{P}_0$, $\overline{P}_1$, or $\overline{P}_2$ to	1.5	3.7	5.0	1.0	7.0	1.5	6.0	ns
	C_{n+x}, C_{n+y}, or C_{n+z}								
t_{PLH}	Propagation Delay	2.5	6.5	8.5	2.5	11.0	2.5	9.5	
t_{PHL}	$\overline{G}_0$, $\overline{G}_1$, or $\overline{G}_2$ to	1.5	3.9	5.2	1.0	7.0	1.5	6.0	ns
	C_{n+x}, C_{n+y}, or C_{n+z}								
t_{PLH}	Propagation Delay	3.0	7.9	10.0	3.0	12.0	3.0	11.0	ns
t_{PHL}	$\overline{P}_1$, $\overline{P}_2$, or $\overline{P}_3$ to $\overline{G}$	3.0	6.0	8.0	2.5	10.0	3.0	9.0	
t_{PLH}	Propagation Delay	3.0	8.3	10.5	3.0	12.0	3.0	11.5	ns
t_{PHL}	$\overline{G}_n$ to $\overline{G}$	3.0	5.7	7.5	2.5	10.0	3.0	8.5	
t_{PLH}	Propagation Delay	3.0	5.7	7.5	2.5	10.0	3.0	8.5	ns
t_{PHL}	$\overline{P}_n$ to $\overline{P}$	2.5	4.1	5.5	2.5	8.0	2.5	6.5	

Physical Dimensions inches (millimeters) unless otherwise noted

10.2±0.1
-A-

0.47 TYP

16   9

7.8

5.3±0.1
-B-

3.9

◁ 0.2 C B A
ALL LEAD TIPS

PIN #1 IDENT.

1   8

LAND PATTERN RECOMMENDATION

16 15   10 9

5.01 TYP

9.27 TYP

(2.13 TYP)

1   2   7   8

1.27 TYP   0.6 TYP

2.1 MAX.

ALL LEAD TIPS
◁ 0.1 C

1.8±0.1

-C-

0.15±0.05

1.27 TYP

0.35-0.51
⊕ 0.12 Ⓜ C A

DIMENSIONS ARE IN MILLIMETERS

SEE DETAIL A

0.15-0.25

7° TYP

GAGE PLANE

0°-8° TYP

0.25

0.60±0.15

1.25

SEATING PLANE

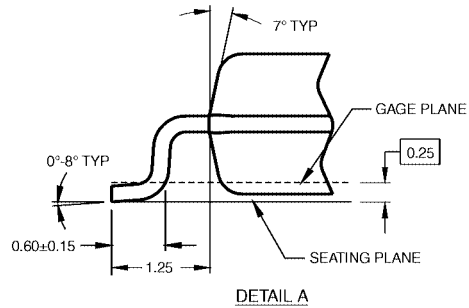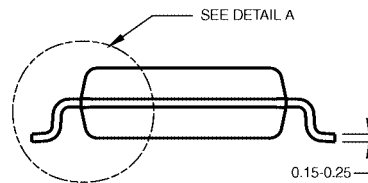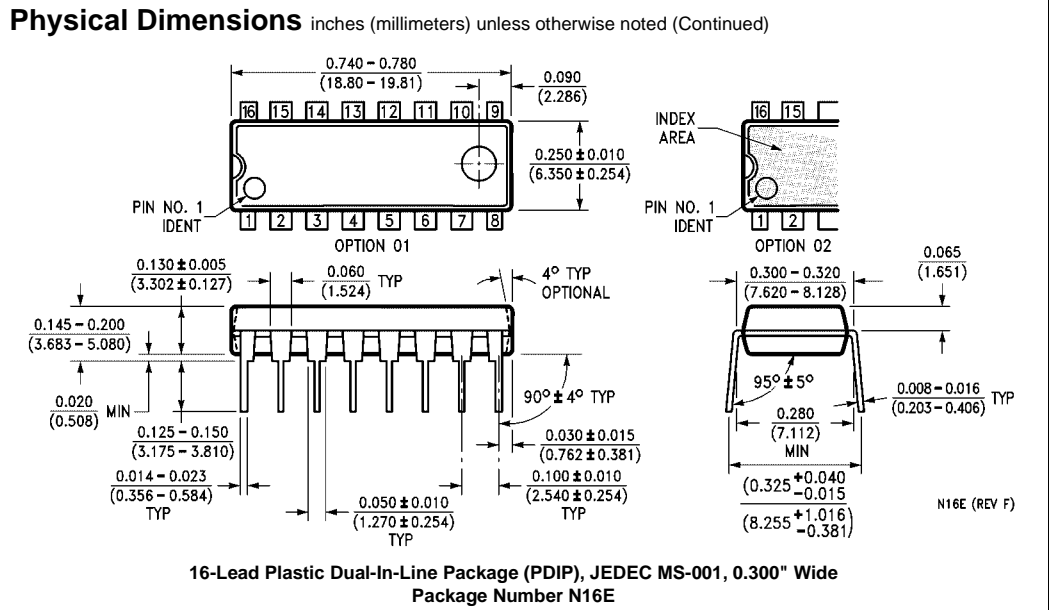### DETAIL A

NOTES:
A. CONFORMS TO EIAJ EDR-7320 REGISTRATION,
   ESTABLISHED IN DECEMBER, 1998.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD
   FLASH, AND TIE BAR EXTRUSIONS.

M16DRevB1

16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M16D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

0.740 − 0.780
(18.80 − 19.81)

0.090
(2.286)

0.250 ± 0.010
(6.350 ± 0.254)

PIN NO. 1
IDENT

OPTION 01

INDEX
AREA

PIN NO. 1
IDENT

OPTION 02

0.065
(1.651)

0.130 ± 0.005
(3.302 ± 0.127)

0.060
(1.524) TYP

4° TYP
OPTIONAL

0.300 − 0.320
(7.620 − 8.128)

0.145 − 0.200
(3.683 − 5.080)

0.020
(0.508) MIN

0.125 − 0.150
(3.175 − 3.810)

90° ± 4° TYP

95° ± 5°

0.008 − 0.016
(0.203 − 0.406) TYP

0.280
(7.112)
MIN

0.014 − 0.023
(0.356 − 0.584)
TYP

0.050 ± 0.010
(1.270 ± 0.254)
TYP

0.030 ± 0.015
(0.762 ± 0.381)

0.100 ± 0.010
(2.540 ± 0.254)
TYP

$(0.325 {+0.040 \atop -0.015})$

$(8.255 {+1.016 \atop -0.381})$

N16E (REV F)

16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N16E

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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