DAC102S085 10-Bit Micro Power DUAL Digital-to-Analog Converter With Rail-to-Rail Output

1 Features

- Ensured Monotonicity
- Low Power Operation
- Rail-to-Rail Voltage Output
- Power-On Reset to 0 V
- Simultaneous Output Updating
- Wide Power Supply Range (2.7 V to 5.5 V)
- Industry's Smallest Package
- Power Down Modes
- Key Specifications
  - Resolution: 10 Bits
  - INL: ±2 LSB (Maximum)
  - DNL: +0.35 or –0.25 LSB (Maximum)
  - Settling Time: 6 µs (Maximum)
  - Zero Code Error: 15 mV (Maximum)
  - Full-Scale Error: –0.75% FS (Maximum)
  - Supply Power
    - Normal: 0.6 mW at 3 V, 1.6 mW at 5 V (Typical)
    - Power Down: 0.3 µW at 3 V, 0.8 µW at 5 V (Typical)

2 Applications

- Battery-Powered Instruments
- Digital Gain and Offset Adjustment
- Programmable Voltage and Current Sources
- Programmable Attenuators

3 Description

The DAC102S085 is a full-featured, general-purpose DUAL 10-bit voltage-output digital-to-analog converter (DAC) that can operate from a single 2.7-V to 5.5-V supply and consumes 0.6 mW at 3 V and 1.6 mW at 5 V. The DAC102S085 is packaged in 10-pin WSON and VSSOP packages. The 10-pin WSON package makes the DAC102S085 the smallest DUAL DAC in its class. The on-chip output amplifier allows rail-to-rail output swing and the three wire serial interface operates at clock rates up to 40 MHz over the entire supply voltage range. Competitive devices are limited to 25-MHz clock rates at supply voltages in the 2.7-V to 3.6-V range. The serial interface is compatible with standard SPI™, QSPI, MICROWIRE and DSP interfaces.

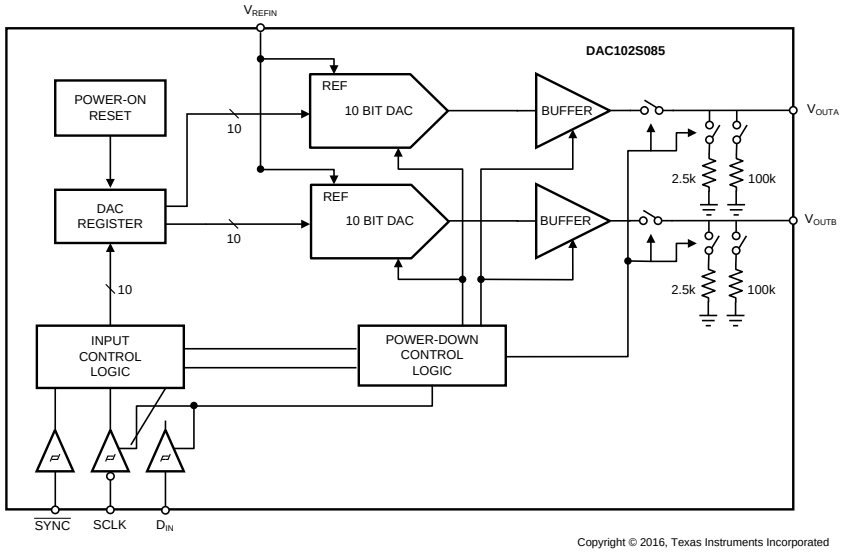
The reference for the DAC102S085 serves both channels and can vary in voltage between 1 V and V_A, providing the widest possible output dynamic range. The DAC102S085 has a 16-bit input shift register that controls the outputs to be updated, the mode of operation, the power-down condition, and the binary input data. Both outputs can be updated simultaneously or individually depending on the setting of the two mode of operation bits.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DAC102S085	VSSOP (10)	3.00 mm × 3.00 mm
	WSON (10)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Block Diagram



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (March 2013) to Revision F — **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1

Changes from Revision D (March 2013) to Revision E — **Page**

- Changed layout of National Data Sheet to TI format ... 23

5 Description (continued)

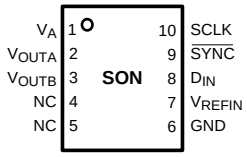
A power-on reset circuit ensures that the DAC output powers up to zero volts and remains there until there is a valid write to the device. A power-down feature reduces power consumption to less than a microWatt with three different termination options.

The low power consumption and small packages of the DAC102S085 make it an excellent choice for use in battery-operated equipment.

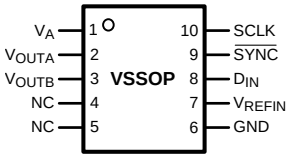
The DAC102S085 is one of a family of pin compatible DACs, including the 8-bit DAC084S085 and the 12-bit DAC122S085. The DAC102S085 operates over the extended industrial temperature range of −40°C to 105°C.

6 Pin Configuration and Functions

DSC Package
10-Pin WSON
Top View



DGS Package
10-Pin VSSOP
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	V_A	Supply	Power supply input. Must be decoupled to GND.
2	V_{OUTA}	Analog Output	Channel A Analog Output Voltage.
3	V_{OUTB}	Analog Output	Channel B Analog Output Voltage.
4, 5	NC	—	Not Connected
6	GND	Ground	Ground reference for all on-chip circuitry.
7	V_{REFIN}	Analog Input	Unbuffered reference voltage shared by all channels. Must be decoupled to GND.
8	D_{IN}	Digital Input	Serial Data Input. Data is clocked into the 16-bit shift register on the falling edges of SCLK after the fall of $\overline{SYNC}$.
9	$\overline{SYNC}$	Digital Input	Frame synchronization input for the data input. When this pin goes low, it enables the input shift register and data is transferred on the falling edges of SCLK. The DAC is updated on the 16th clock cycle unless $\overline{SYNC}$ is brought high before the 16th clock, in which case the rising edge of $\overline{SYNC}$ acts as an interrupt and the write sequence is ignored by the DAC.
10	SCLK	Digital Input	Serial Clock Input. Data is clocked into the input shift register on the falling edges of this pin.
11	PAD(1)	Ground	Exposed die attach pad can be connected to ground or left floating. Soldering the pad to the PCB offers optimal thermal performance and enhances package self-alignment during reflow.

(1) PAD is only applicable for the WSON package.

7 Specifications

7.1 Absolute Maximum Ratings

See (1)(2)(3)

		MIN	MAX	UNIT
Supply voltage	V_A		6.5	V
Voltage	D_{IN}, SCLK, $\overline{SYNC}$, V_{REFIN}	−0.3	6.5	V
Input current (4)			10	mA
Package input current (4)			20	mA
Power consumption at T_A = 25°C		See (5)		
Junction temperature, T_J			150	°C
Storage temperature, T_{stg}		−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) All voltages are measured with respect to GND = 0 V, unless otherwise specified.
(4) When the input voltage at any pin exceeds 5.5 V or is less than GND, the current at that pin should be limited to 10 mA. The 20-mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 10 mA to two.
(5) The maximum allowable power dissipation is dictated by $T_J$max, the junction-to-ambient thermal resistance ($R_{\theta JA}$), and the ambient temperature (T_A), and can be calculated using the formula $P_D$max = ($T_J$max - T_A) / $R_{\theta JA}$.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

See (1)

		MIN	MAX	UNIT
	Operating temperature	–40	105	°C
V_A	Supply voltage	2.7	5.5	V
V_{REFIN}	Reference voltage	1	V_A	V
	Digital input voltage (2)	0	5.5	V
	Output load	0	1500	pF
	SCLK frequency		40	MHz

(1) All voltages are measured with respect to GND = 0 V, unless otherwise specified.
(2) The inputs are protected. Input voltage magnitudes up to 5.5 V, regardless of V_A, do not cause errors in the conversion result. For example, if V_A is 3 V, the digital input pins can be driven with a 5-V logic device.

7.4 Thermal Information

THERMAL METRIC (1)		DAC102S085		UNIT
		DGS (VSSOP)	DSC (WSON)	
		10 PINS	10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	240	250	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

The following specifications apply for V_A = 2.7 V to 5.5 V, V_{REFIN} = V_A, C_L = 200 pF to GND, f_{SCLK} = 30 MHz, input code range 12 to 1011. Minimum and Maximum limits apply for T_A = –40°C to 105°C, Typical values apply for T_A = 25°C, unless otherwise specified. Test limist are specified to AOQL (Average Outgoing Quality Level).(1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
STATIC PERFORMANCE							
	Resolution			10			Bits
	Monotonicity			10			Bits
INL	Integral non-linearity				±0.7	±2	LSB
DNL	Differential non-linearity	V_A = 2.7 V to 5.5 V	T_A = 25°C	–0.03		0.08	LSB
			T_A = –40°C to 105°C	–0.25		0.35	
ZE	Zero code error	I_{OUT} = 0			5	15	mV
FSE	Full-scale error	I_{OUT} = 0			–0.1	–0.75	%FSR
GE	Gain error	All ones loaded to DAC register			–0.2	–1	%FSR
ZCED	Zero code error drift				–20		µV/°C
TC GE	Gain error tempco	V_A = 3 V			–0.7		ppm/°C
		V_A = 5 V			–1		
OUTPUT CHARACTERISTICS							
	Output voltage range			0		V_{REFIN}	V
I_{OZ}	High-impedance output leakage current					±1	µA
ZCO	Zero code output	V_A = 3 V, I_{OUT} = 200 µA			1.3		mV
		V_A = 3 V, I_{OUT} = 1 mA			6		
		V_A = 5 V, I_{OUT} = 200 µA			7		
		V_A = 5 V, I_{OUT} = 1 mA			10		
FSO	Full scale output	V_A = 3 V, I_{OUT} = 200 µA			2.984		V
		V_A = 3 V, I_{OUT} = 1 mA			2.934		
		V_A = 5 V, I_{OUT} = 200 µA			4.989		
		V_A = 5 V, I_{OUT} = 1 mA			4.958		
I_{OS}	Output short-circuit current (source)	V_A = 3 V, V_{OUT} = 0 V, Input Code = 3FFh			–56		mA
		V_A = 5 V, V_{OUT} = 0 V, Input Code = 3FFh			–69		
I_{OS}	Output short-circuit current (sink)	V_A = 3 V, V_{OUT} = 3 V, Input Code = 000h			52		mA
		V_A = 5 V, V_{OUT} = 5 V, Input Code = 000h			75		
I_O	Continuous output current	Available on each DAC output				11	mA
C_L	Maximum load capacitance	R_L = ∞			1500		pF
		R_L = 2 kΩ			1500		
Z_{OUT}	DC output impedance				7.5		Ω
REFERENCE INPUT CHARACTERISTICS							
V_{REFIN}	Input range minimum				0.2	1	V
	Input range maximum					V_A	
Z_{IN}	Input impedance				60		kΩ
LOGIC INPUT CHARACTERISTICS							
I_{IN}	Input current					±1	µA
V_{IL}	Input low voltage	V_A = 3 V			0.9	0.6	V
		V_A = 5 V			1.5	0.8	
V_{IH}	Input high voltage	V_A = 3 V			1.4	2.1	V
		V_A = 5 V			2.1	2.4	
C_{IN}	Input capacitance					3	pF
POWER REQUIREMENTS							
I_N	Normal supply current (output unloaded)	f_{SCLK} = 30 MHz	V_A = 2.7 V to 3.6 V		210	270	µA
			V_A = 4.5 V to 5.5 V		320	410	
		f_{SCLK} = 0 MHz	V_A = 2.7 V to 3.6 V		190		
			V_A = 4.5 V to 5.5 V		290		

(1) To ensure accuracy, it is required that V_A and V_{REFIN} be well bypassed.

Electrical Characteristics (continued)

The following specifications apply for V_A = 2.7 V to 5.5 V, V_{REFIN} = V_A, C_L = 200 pF to GND, f_{SCLK} = 30 MHz, input code range 12 to 1011. Minimum and Maximum limits apply for T_A = –40°C to 105°C, Typical values apply for T_A = 25°C, unless otherwise specified. Test limist are specified to AOQL (Average Outgoing Quality Level).(1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{PD}	Power-down supply current (output unloaded, SYNC = DIN = 0 V after PD mode loaded)	All PD Modes	V_A = 2.7 V to 3.6 V		0.1	1	µA
			V_A = 4.5 V to 5.5 V		0.15	1	
P_N	Normal supply power (output unloaded)	f_{SCLK} = 30 MHz	V_A = 2.7 V to 3.6 V		0.6	1	mW
			V_A = 4.5 V to 5.5 V		1.6	2.3	
		f_{SCLK} = 0 MHz	V_A = 2.7 V to 3.6 V		0.6		
			V_A = 4.5 V to 5.5 V		1.5		
P_{PD}	Power down supply current (output unloaded, SYNC = DIN = 0 V after PD mode loaded)	All PD Modes	V_A = 2.7 V to 3.6 V		0.3	3.6	µW
			V_A = 4.5 V to 5.5 V		0.8	5.5	

7.6 AC and Timing Requirements

Values shown in this table are design targets and are subject to change before product release.
The following specifications apply for V_A = 2.7 V to 5.5 V, V_{REFIN} = V_A, C_L = 200 pF to GND, f_{SCLK} = 30 MHz, input code range 12 to 1011. Minimum and Maximum limits apply for T_A = –40°C to 105°C, Typical values apply for T_A = 25°C, unless otherwise specified. Test limist are specified to AOQL (Average Outgoing Quality Level).

			MIN	TYP	MAX	UNIT
f_{SCLK}	SCLK frequency			40	30	MHz
t_s	Output voltage settling time	100h to 300h code change R_L = 2 kΩ, C_L = 200 pF		4.5	6	µs
SR	Output slew rate			1		V/µs
	Glitch impulse	Code change from 200h to 1FFh		12		nV-sec
	Digital feedthrough			0.5		nV-sec
	Digital crosstalk			1		nV-sec
	DAC-to-DAC crosstalk			3		nV-sec
	Multiplying bandwidth	V_{REFIN} = 2.5 V ± 0.1 V_{PP}		160		kHz
	Total harmonic distortion	V_{REFIN} = 2.5 V ± 1.0 V_{PP} input frequency = 10 kHz		70		dB
t_{WU}	Wake-up time	V_A = 3 V		6		µs
		V_A = 5 V		39		
$1/f_{SCLK}$	SCLK cycle time		33	25		ns
t_{CH}	SCLK high time		10	7		ns
t_{CL}	SCLK low time		10	7		ns
t_{SS}	$\overline{SYNC}$ setup time prior to SCLK falling edge		10	4		ns
t_{DS}	Data setup time prior to SCLK falling edge		3.5	1.5		ns
t_{DH}	Data hold time after SCLK falling edge		3.5	1.5		ns
t_{CFSR}	SCLK fall prior to rise of $\overline{SYNC}$		3	0		ns
t_{SYNC}	$\overline{SYNC}$ high time		10	6		ns

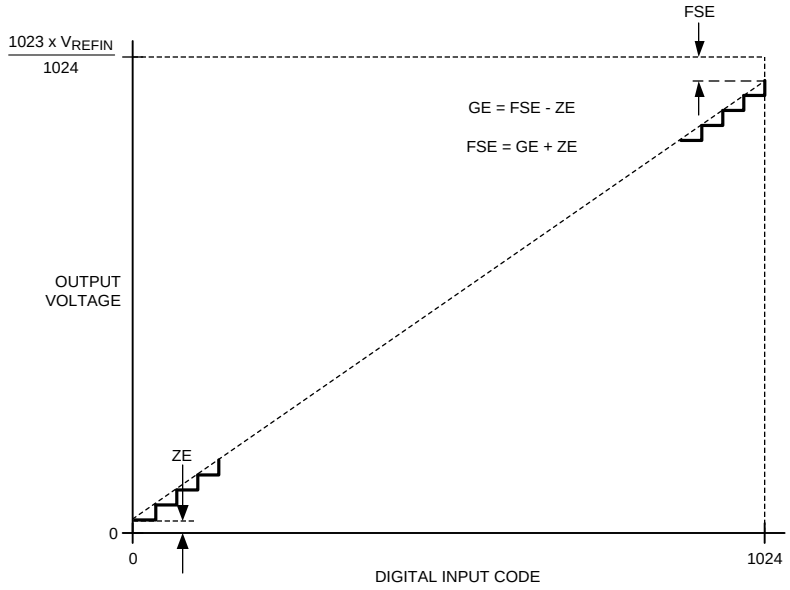


Figure 1. I/O Transfer Characteristic

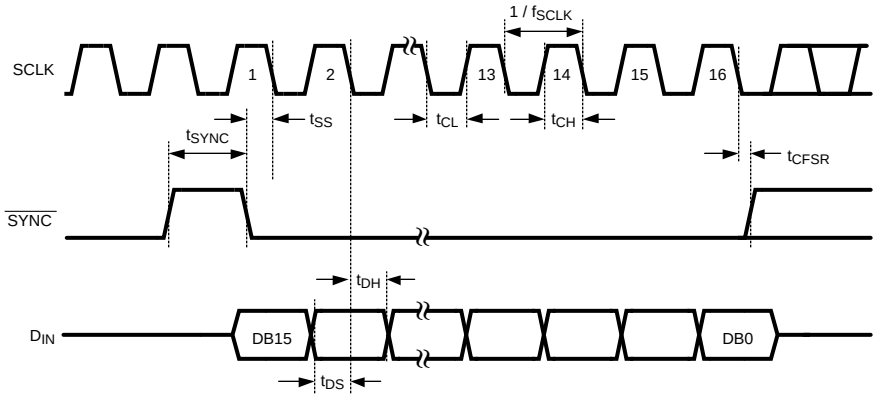


Figure 2. Serial Timing Diagram

7.7 Typical Characteristics

$V_{REF} = V_A$, f_{SCLK} = 30 MHz, T_A = 25C, Input Code Range 12 to 1011, unless otherwise stated

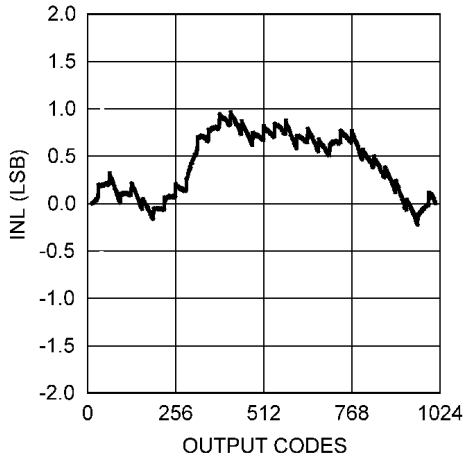


Figure 3. INL at V_A = 3 V

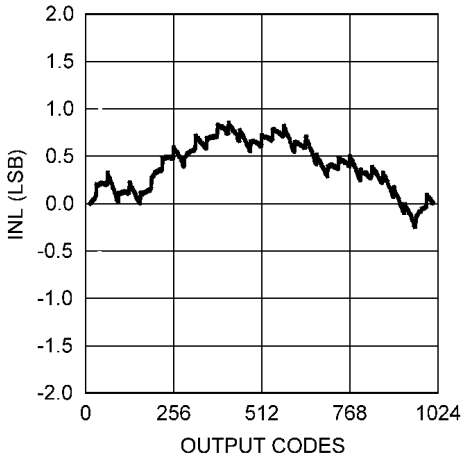


Figure 4. INL at V_A = 5 V

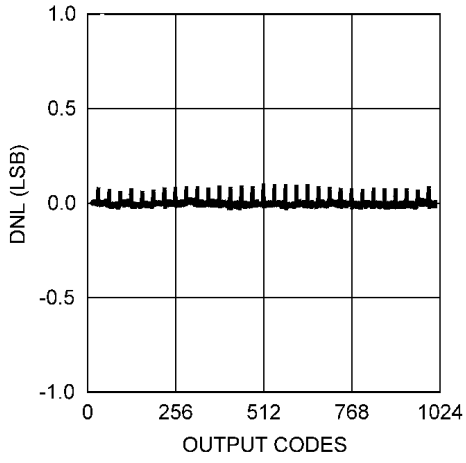


Figure 5. DNL at V_A = 3 V

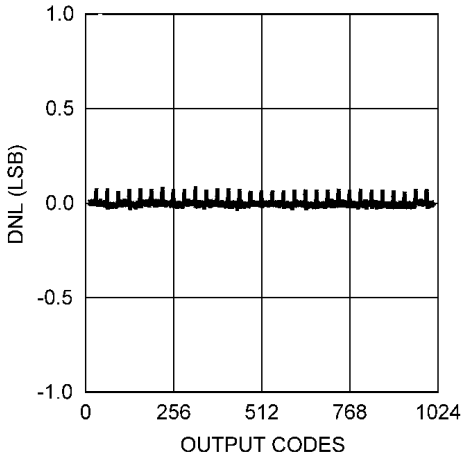


Figure 6. DNL at V_A = 5 V

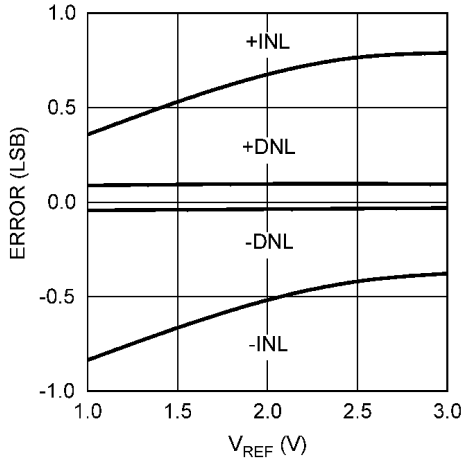


Figure 7. INL and DNL vs V_{REFIN} at V_A = 3 V

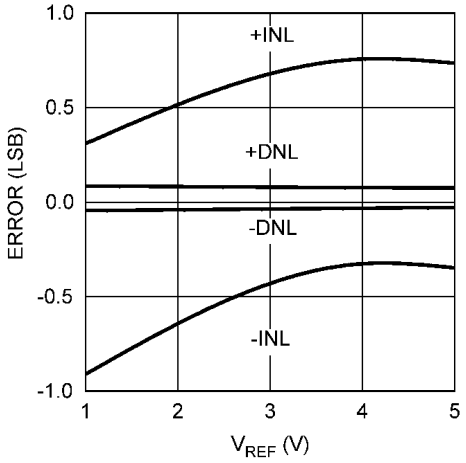


Figure 8. INL and DNL vs V_{REFIN} at V_A = 5 V

Typical Characteristics (continued)

$V_{REF} = V_A$, f_{SCLK} = 30 MHz, T_A = 25C, Input Code Range 12 to 1011, unless otherwise stated

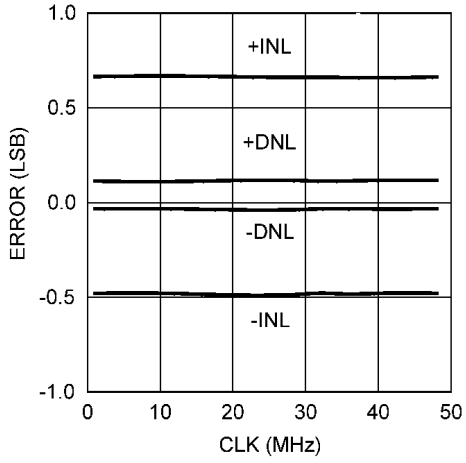


Figure 9. INL and DNL vs f_{SCLK} at V_A = 2.7 V

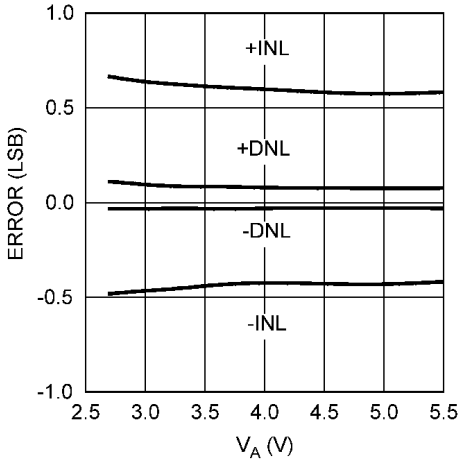


Figure 10. INL and DNL vs V_A

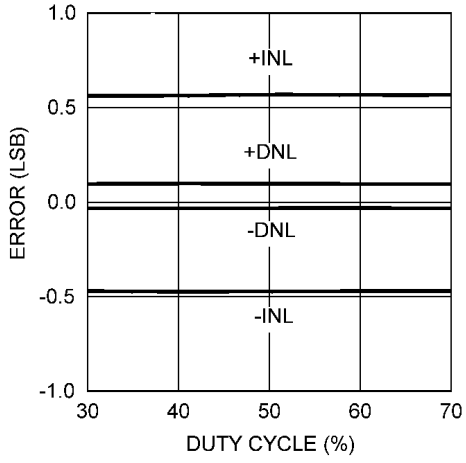


Figure 11. INL and DNL vs Clock Duty Cycle at V_A = 3 V

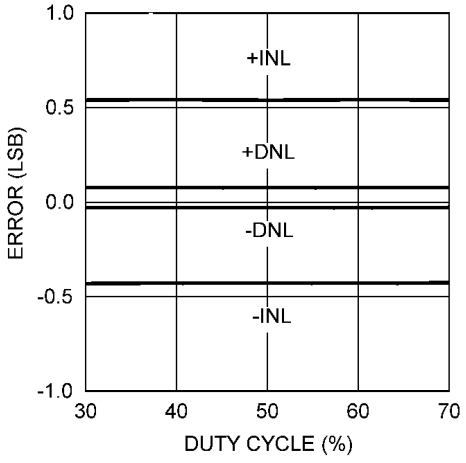


Figure 12. INL and DNL vs Clock Duty Cycle at V_A = 5 V

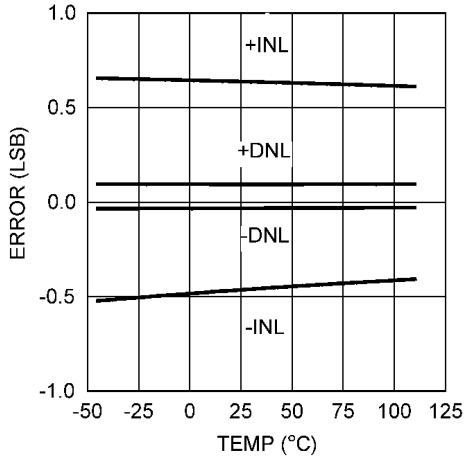


Figure 13. INL and DNL vs Temperature at V_A = 3 V

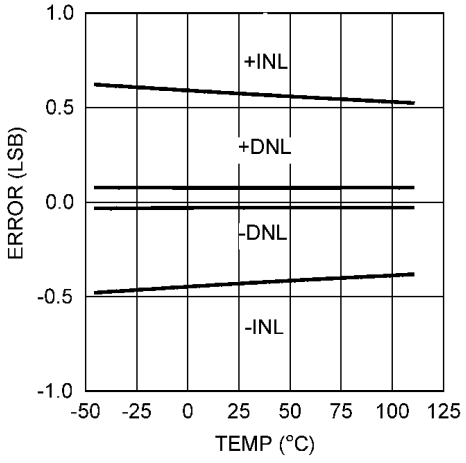


Figure 14. INL and DNL vs Temperature at V_A = 5 V

Typical Characteristics (continued)

$V_{REF} = V_A$, f_{SCLK} = 30 MHz, T_A = 25C, Input Code Range 12 to 1011, unless otherwise stated

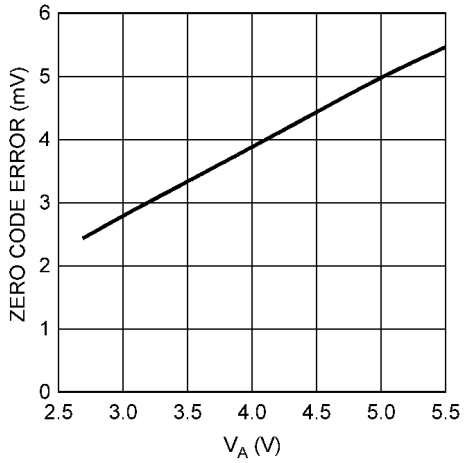


Figure 15. Zero Code Error vs V_A

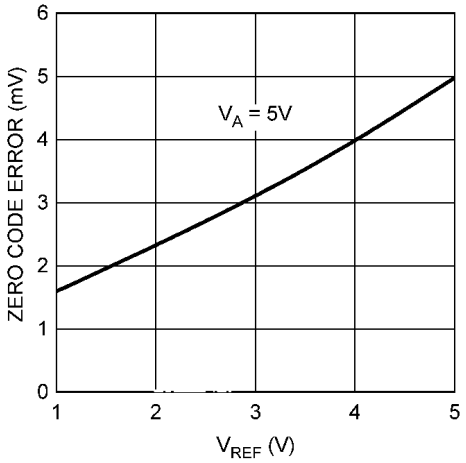


Figure 16. Zero Code Error vs V_{REFIN}

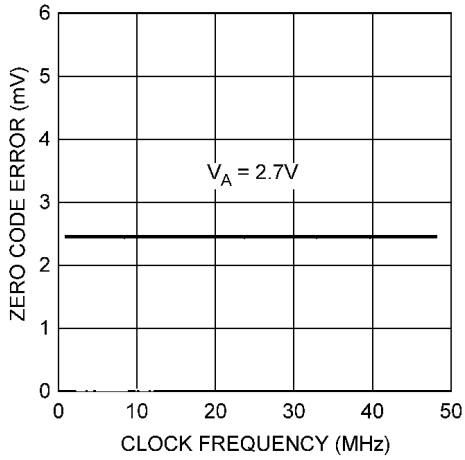


Figure 17. Zero Code Error vs f_{SCLK}

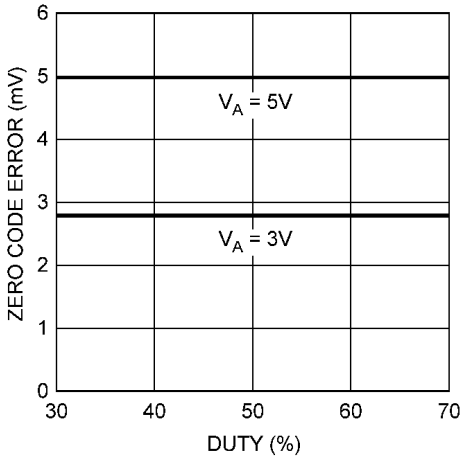


Figure 18. Zero Code Error vs Clock Duty Cycle

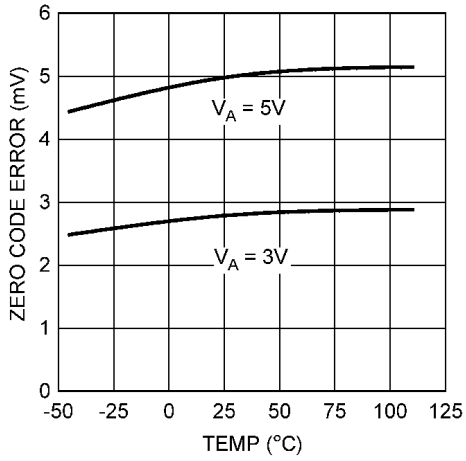


Figure 19. Zero Code Error vs Temperature

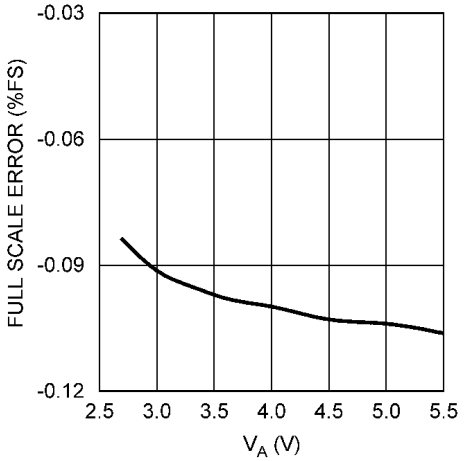


Figure 20. Full-Scale Error vs V_A

Typical Characteristics (continued)

V_{REF} = V_A, f_{SCLK} = 30 MHz, T_A = 25C, Input Code Range 12 to 1011, unless otherwise stated

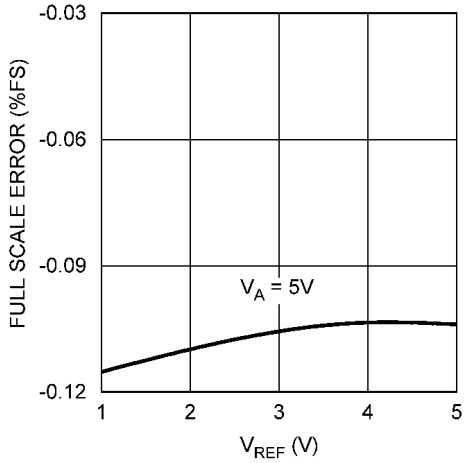


Figure 21. Full-Scale Error vs V_{REFIN}

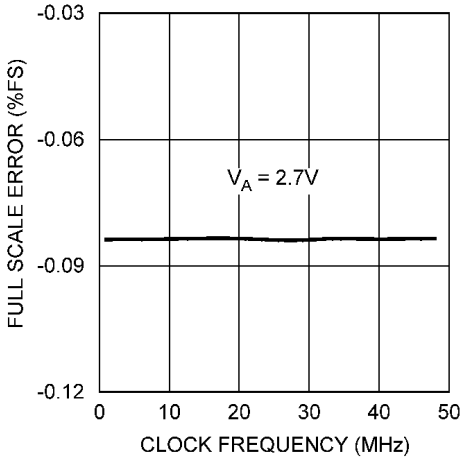


Figure 22. Full-Scale Error vs f_{SCLK}

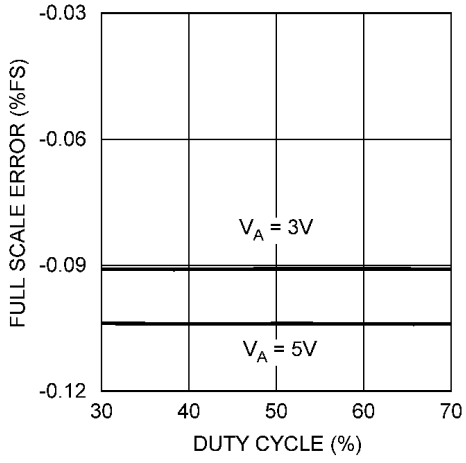


Figure 23. Full-Scale Error vs Clock Duty Cycle

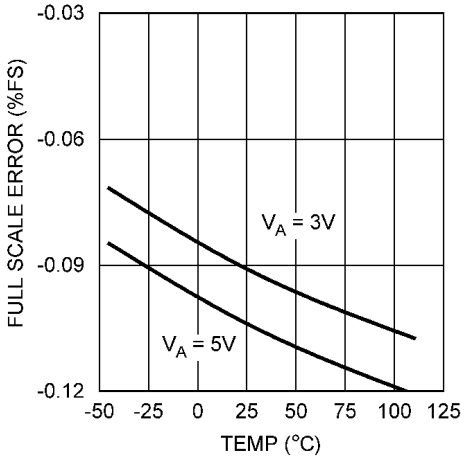


Figure 24. Full-Scale Error vs Temperature

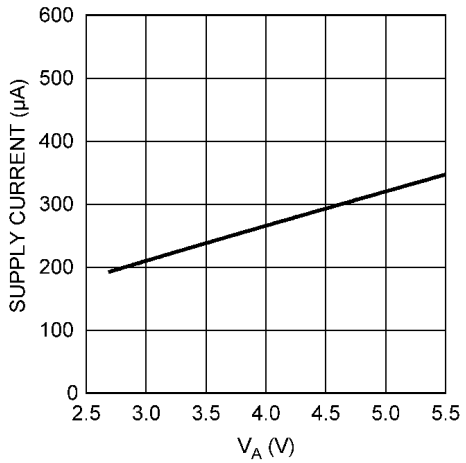


Figure 25. Supply Current vs V_A

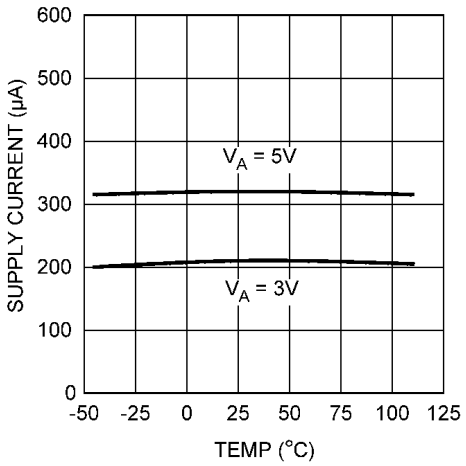


Figure 26. Supply Current vs Temperature

Typical Characteristics (continued)

$V_{REF} = V_A$, f_{SCLK} = 30 MHz, T_A = 25C, Input Code Range 12 to 1011, unless otherwise stated

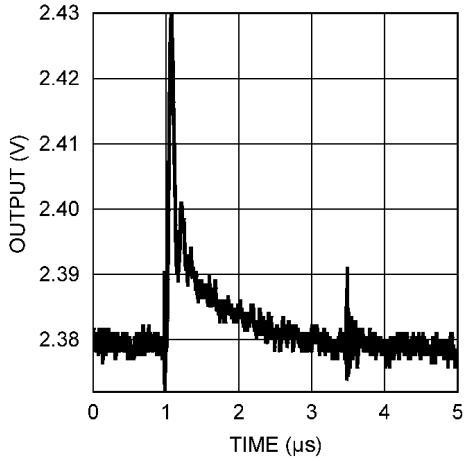


Figure 27. 5-V Glitch Response

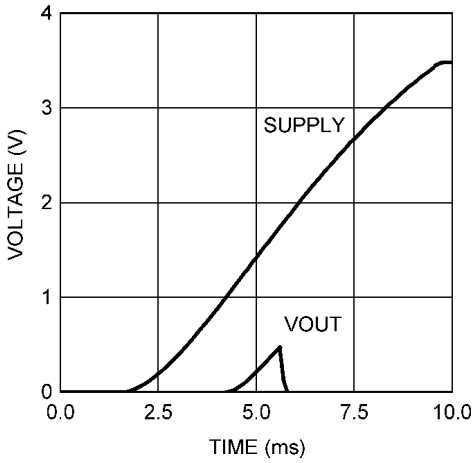


Figure 28. Power-On Reset

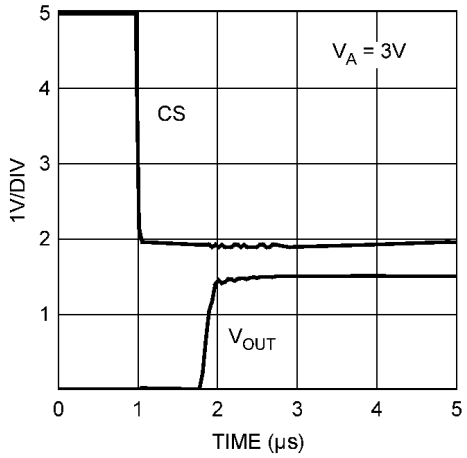


Figure 29. 3-V Wakeup Time

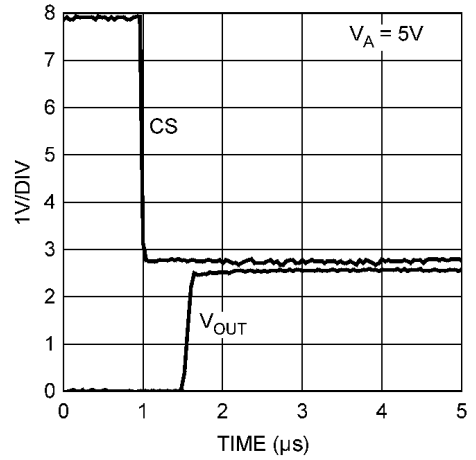


Figure 30. 5-V Wakeup Time

8 Detailed Description

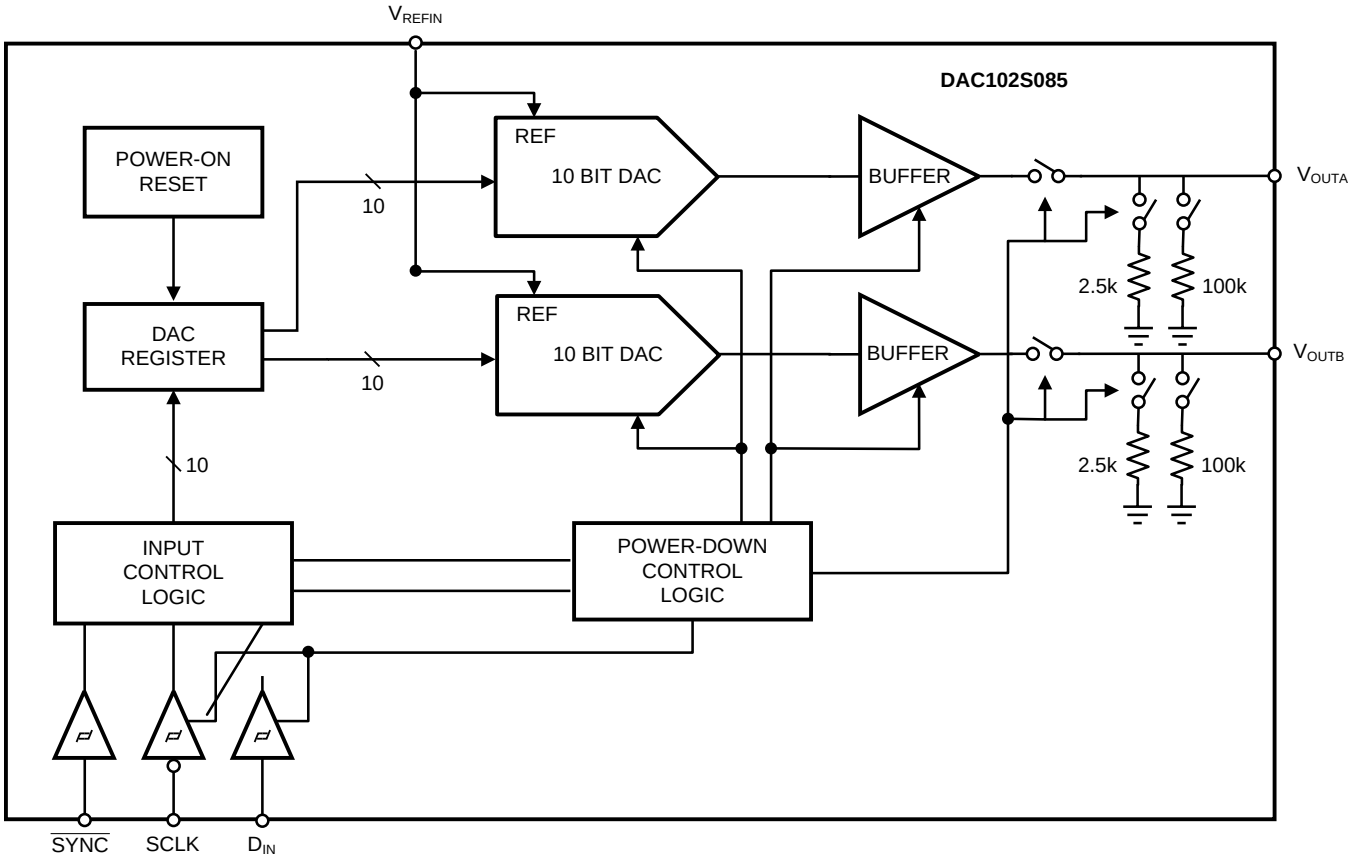
8.1 Overview

The DAC102S085 is a full-featured, general-purpose DUAL 10-bit voltage-output digital-to-analog converter (DAC) that can operate from a single 2.7-V to 5.5-V supply and consumes 0.6 mW at 3 V and 1.6 mW at 5 V. The on-chip output amplifier allows rail-to-rail output swing and the three wire serial interface operates at clock rates up to 40 MHz over the entire supply voltage range. The serial interface is compatible with standard SPI, QSPI, MICROWIRE, and DSP interfaces.

The reference for the DAC102S085 serves both channels and can vary in voltage between 1 V and V_A, providing the widest possible output dynamic range. The DAC102S085 has a 16-bit input shift register that controls the outputs to be updated, the mode of operation, the power-down condition, and the binary input data. Both outputs can be updated simultaneously or individually depending on the setting of the two mode-of-operation bits.

A power-on reset circuit ensures that the DAC output powers up to zero volts and remains there until there is a valid write to the device. A power-down feature reduces power consumption to less than a micro-watt with three different termination options.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 DAC Section

The DAC102S085 is fabricated on a CMOS process with an architecture that consists of switches and resistor strings that are followed by an output buffer. The reference voltage is externally applied at V_{REFIN} and is shared by both DACs.

Feature Description (continued)

For simplicity, a single resistor string is shown in Figure 31. This string consists of 1024 equal valued resistors with a switch at each junction of two resistors, plus a switch to ground. The code loaded into the DAC register determines which switch is closed, connecting the proper node to the amplifier. The input coding is straight binary with an ideal output voltage calculated by Equation 1.

$$V_{OUTA,B} = V_{REFIN} \times (D / 1024) \quad (1)$$

where

- D is the decimal equivalent of the binary code that is loaded into the DAC register. (D can take on any value between 0 and 1023. This configuration ensures that the DAC is monotonic.)

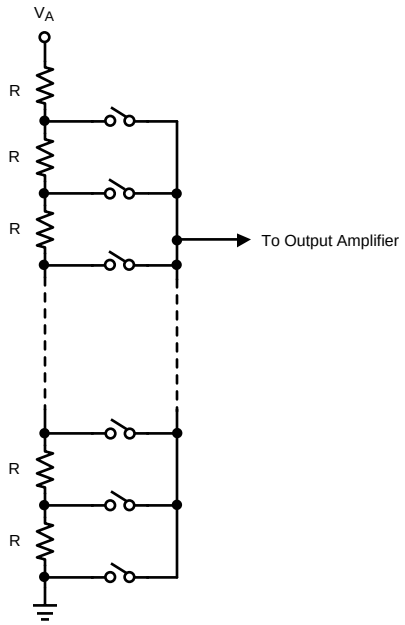


Figure 31. DAC Resistor String

8.3.2 Output Amplifiers

The output amplifiers are rail-to-rail, providing an output voltage range of 0 V to V_A when the reference is V_A. All amplifiers, even rail-to-rail types, exhibit a loss of linearity as the output approaches the supply rails (0 V and V_A, in this case). For this reason, linearity is specified over less than the full output range of the DAC. However, if the reference is less than V_A, there is only a loss in linearity in the lowest codes. The output capabilities of the amplifier are described in *Electrical Characteristics*.

The output amplifiers are capable of driving a load of 2 kΩ in parallel with 1500 pF to ground or to V_A. The zero-code and full-scale outputs for given load currents are available in *Electrical Characteristics*.

8.3.3 Reference Voltage

The DAC102S085 uses a single external reference that is shared by both channels. The reference pin, V_{REFIN}, is not buffered and has an input impedance of 60 kΩ. TI recommends driving the V_{REFIN} by a voltage source with low output impedance. The reference voltage range is 1 V to V_A, providing the widest possible output dynamic range.

8.3.4 Power-On Reset

The power-on reset circuit controls the output voltages of both DACs during power up. Upon application of power, the DAC registers are filled with zeros and the output voltages are 0 V. The outputs remain at 0 V until a valid write sequence is made to the DAC.

8.4 Device Functional Modes

8.4.1 Power-Down Modes

The DAC102S085 has four power-down modes, two of which are identical. In power-down mode, the supply current drops to 20 µA at 3 V and 30 µA at 5 V. The DAC102S085 is set in power-down mode by setting OP1 and OP0 to 11. Since this mode powers down both DACs, the first two bits of the shift register are used to select different output terminations for the DAC outputs. Setting A1 and A0 to 00 or 11 causes the outputs to be tri-stated (a high impedance state). While setting A1 and A0 to 01 or 10 causes the outputs to be terminated by 2.5 kΩ or 100 kΩ to ground respectively (see Table 1).

Table 1. Power-Down Modes

A1	A0	OP1	OP0	OPERATING MODE
0	0	1	1	High-Z outputs
0	1	1	1	2.5 kΩ to GND
1	0	1	1	100 kΩ to GND
1	1	1	1	High-Z outputs

The bias generator, output amplifiers, resistor strings, and other linear circuitry are all shut down in any of the power-down modes. However, the contents of the DAC registers are unaffected when in power-down. Each DAC register maintains its value prior to the DAC102S085 being powered down unless it is changed during the write sequence which instructed it to recover from power down. Minimum power consumption is achieved in the power-down mode with $\overline{SYNC}$ and D_{IN} idled low and SCLK disabled. The time to exit power down (Wake-Up Time) is typically t_{WU} µs as stated in *AC and Timing Requirements*.

8.5 Programming

8.5.1 Serial Interface

The three-wire interface is compatible with SPI™, QSPI and MICROWIRE, as well as most DSPs and operates at clock rates up to 40 MHz. See *AC and Timing Requirements* for information on a write sequence.

A write sequence begins by bringing the $\overline{SYNC}$ line low. Once $\overline{SYNC}$ is low, the data on the D_{IN} line is clocked into the 16-bit serial input register on the falling edges of SCLK. To avoid misclocking data into the shift register, it is critical that $\overline{SYNC}$ not be brought low simultaneously with a falling edge of SCLK (see Figure 2). On the 16th falling clock edge, the last data bit is clocked in and the programmed function (a change in the DAC channel address, mode of operation, or register contents) is executed. At this point the $\overline{SYNC}$ line may be kept low or brought high. Any data and clock pusles after the 16th falling clock edge are ignored. In either case, $\overline{SYNC}$ must be brought high for the minimum specified time before the next write sequence is initiated with a falling edge of $\overline{SYNC}$.

Since the $\overline{SYNC}$ and D_{IN} buffers draw more current when they are high, they should be idled low between write sequences to minimize power consumption.

8.5.2 Input Shift Register

The input shift register, Figure 32, has sixteen bits. The first bit must be set to 0 and the second bit is an address bit. The address bit determines whether the register data is for DAC A or DAC B. This bit is followed by two bits that determine the mode of operation (writing to a DAC register without updating the outputs of both DACs, writing to a DAC register and updating the outputs of both DACs, writing to the register of both DACs and updating their outputs, or powering down both outputs). The final twelve bits of the shift register are the data bits. The data format is straight binary (MSB first, LSB last), with all 0s corresponding to an output of 0 V and all 1s corresponding to a full-scale output of V_{REFIN} - 1 LSB. The contents of the serial input register are transferred to the DAC register on the sixteenth falling edge of SCLK. See Figure 2.

Programming (continued)

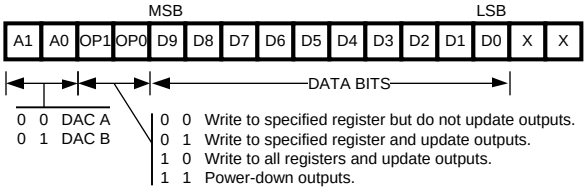


Figure 32. Input Register Contents

Normally, the $\overline{\text{SYNC}}$ line is kept low for at least 16 falling edges of SCLK and the DAC is updated on the 16th SCLK falling edge. However, if $\overline{\text{SYNC}}$ is brought high before the 16th falling edge, the data transfer to the shift register is aborted and the write sequence is invalid. Under this condition, the DAC register is not updated and there is no change in the mode of operation or in the DAC output voltages.

8.5.3 DSP and Microprocessor Interfacing

Interfacing the DAC102S085 to microprocessors and DSPs is quite simple. The following guidelines are offered to hasten the design process.

8.5.3.1 ADSP-2101 and ADSP-2103 Interfacing

Figure 33 shows a serial interface between the DAC102S085 and the ADSP-2101 or ADSP-2103. The DSP should be set to operate in the SPORT Transmit Alternate Framing Mode. It is programmed through the SPORT control register and should be configured for Internal Clock Operation, Active Low Framing and 16-bit Word Length. Transmission is started by writing a word to the Tx register after the SPORT mode has been enabled.

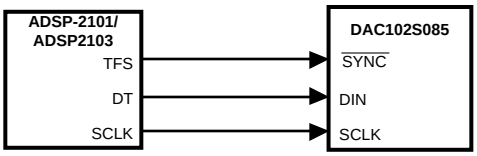


Figure 33. ADSP-2101 and ADSP-2103 Interface

8.5.3.2 80C51 and 80L51 Interface

A serial interface between the DAC102S085 and the 80C51 or 80L51 microcontroller is shown in Figure 34. The $\overline{\text{SYNC}}$ signal comes from a bit-programmable pin on the microcontroller. The example shown here uses port line P3.3. This line is taken low when data is transmitted to the DAC102S085. Since the 80C51 and 80L51 transmit 8-bit bytes, only eight falling clock edges occur in the transmit cycle. To load data into the DAC, the P3.3 line must be left low after the first eight bits are transmitted. A second write cycle is initiated to transmit the second byte of data, after which port line P3.3 is brought high. The 80C51 and 80L51 transmit routine must recognize that the 80C51 and 80L51 transmit data with the LSB first while the DAC102S085 requires data with the MSB first.

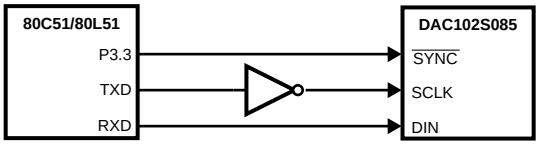


Figure 34. 80C51 and 80L51 Interface

Programming (continued)

8.5.3.3 68HC11 Interface

A serial interface between the DAC102S085 and the 68HC11 microcontroller is shown in Figure 35. The $\overline{\text{SYNC}}$ line of the DAC102S085 is driven from a port line (PC7 in the figure), similar to the 80C51 and 80L51.

The 68HC11 should be configured with its CPOL bit as a zero and its CPHA bit as a one. This configuration causes data on the MOSI output to be valid on the falling edge of SCLK. PC7 is taken low to transmit data to the DAC. The 68HC11 transmits data in 8-bit bytes with eight falling clock edges. Data is transmitted with the MSB first. PC7 must remain low after the first eight bits are transferred. A second write cycle is initiated to transmit the second byte of data to the DAC, after which PC7 should be raised to end the write sequence.

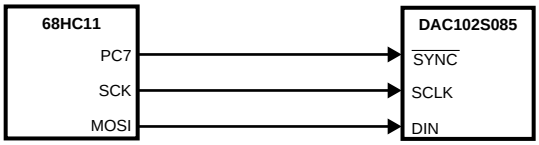


Figure 35. 68HC11 Interface

8.5.3.4 Microwire Interface

Figure 36 shows an interface between a Microwire compatible device and the DAC102S085. Data is clocked out on the rising edges of the SK signal. As a result, the SK of the Microwire device needs to be inverted before driving the SCLK of the DAC102S085.

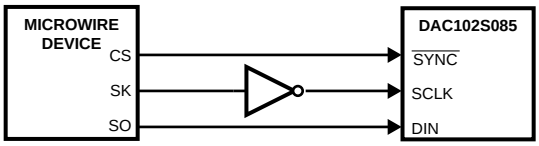


Figure 36. Microwire Interface

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Bipolar Operation

The DAC102S085 is designed for single supply operation and thus has a unipolar output. However, a bipolar output may be obtained with the circuit shown in Figure 37. This circuit provides an output voltage range of ±5 V. A rail-to-rail amplifier should be used if the amplifier supplies are limited to ±5 V.

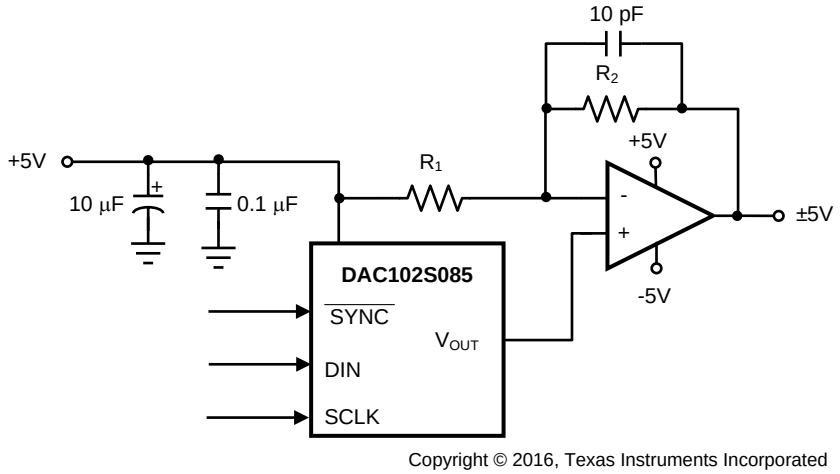


Figure 37. Bipolar Operation

The output voltage of this circuit for any code is found using Equation 2.

$$V_O = (V_A \times (D / 1024) \times ((R1 + R2) / R1) - V_A \times R2 / R1) \quad (2)$$

$$V_O = (10 \times D / 1024) - 5\ V \quad (3)$$

where

- D is the input code in decimal form
- V_A = 5 V
- R1 = R2

A list of rail-to-rail amplifiers suitable for this application are indicated in Table 2.

Table 2. Some Rail-to-Rail Amplifiers

AMP	PKGS	Typical V_{OS}	Typical I_{SUPPLY}
LMC7111	DIP-8, SOT23-5	0.9 mV	25 µA
LM7301	SO-8, SOT23-5	0.03 mV	620 µA
LM8261	SOT23-5	0.7 mV	1 mA

9.2 Typical Application

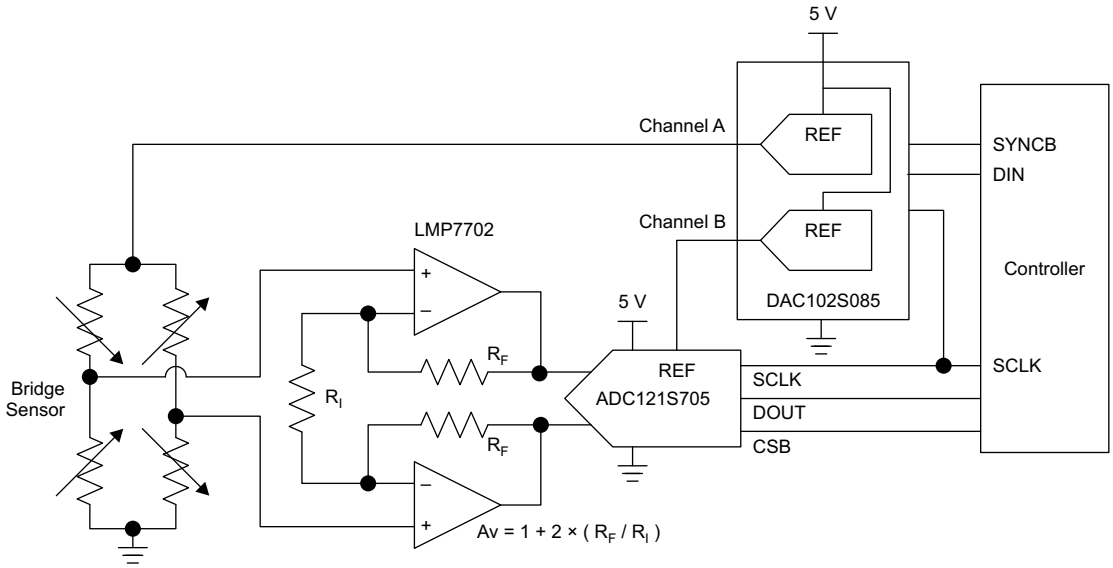


Figure 38. Driving an ADC Reference

9.2.1 Design Requirements

Figure 38 shows Channel A of the DAC102S085 providing the drive or supply voltage for a bridge sensor. By having the sensor supply voltage adjustable, the output of the sensor can be optimized to the input level of the ADC monitoring it.

9.2.2 Detailed Design Procedure

The output of the sensor is amplified by a fixed gain amplifier stage with a differential gain of $1 + 2 \times (R_F / R_I)$. The advantage of this amplifier configuration is the high input impedance seen by the output of the bridge sensor. The disadvantage is the poor common-mode rejection ratio (CMRR). The common-mode voltage (V_{CM}) of the bridge sensor is half of DAC output of Channel A. The V_{CM} is amplified by a gain of 1 V/V by the amplifier stage and thus becomes the bias voltage for the input of the ADC121S705. Channel B of the DAC102S085 is providing the reference voltage to the ADC121S705. The reference for the ADC121S705 may be set to any voltage from 1 V to 5 V, providing the widest dynamic range possible.

The reference voltage for Channel A and B is powered by an external 5-V power supply. Because the 5-V supply is common to the sensor supply voltage and the reference voltage of the ADC, fluctuations in the value of the 5-V supply has a minimal effect on the digital output code of the ADC. This type of configuration is often referred to as a *ratiometric* design. For example, an increase of 5% to the 5-V supply causes the sensor supply voltage to increase by 5%. This causes the gain or sensitivity of the sensor to increase by 5%. The gain of the amplifier stage is unaffected by the change in supply voltage. The ADC121S705 on the other hand, also experiences a 5% increase to its reference voltage. This causes the size of the least significant bit (LSB) of the ADC to increase by 5%. As a result of the gain of the sensor increasing by 5% and the LSB size of the ADC increasing by the same 5%, there is no net effect on the performance of the circuit. It is assumed that the amplifier gain is set low enough to allow for a 5% increase in the sensor output. Otherwise, the increase in the sensor output level may cause the output of the amplifiers to clip.

Typical Application (continued)

9.2.3 Application Curve

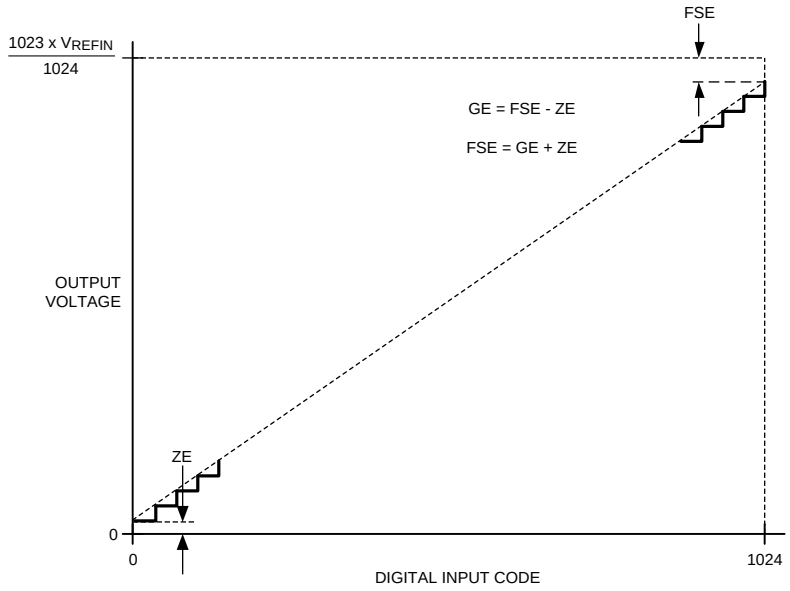


Figure 39. I/O Transfer Characteristic

10 Power Supply Recommendations

10.1 Using References as Power Supplies

While the simplicity of the DAC102S085 implies ease of use, it is important to recognize that the path from the reference input (V_{REFIN}) to the VOUTs has essentially zero Power Supply Rejection Ratio (PSRR). Therefore, it is necessary to provide a noise-free supply voltage to V_{REFIN}. To use the full dynamic range of the DAC102S085, the supply pin (V_A) and V_{REFIN} can be connected together and share the same supply voltage. Since the DAC102S085 consumes very little power, a reference source may be used as the reference input or the supply voltage. The advantages of using a reference source over a voltage regulator are accuracy and stability. Some low-noise regulators can also be used. Listed below are a few reference and power supply options for the DAC102S085.

10.1.1 LM4130

The LM4130, with its 0.05% accuracy over temperature, is a good choice as a reference source for the DAC102S085. The 4.096-V version is useful if a 0 to 4.095-V output range is desirable or acceptable. Bypassing the LM4130 VIN pin with a 0.1-µF capacitor and the VOUT pin with a 2.2-µF capacitor improves stability and reduce output noise. The LM4130 comes in a space-saving 5-pin SOT-23 package.

Using References as Power Supplies (continued)

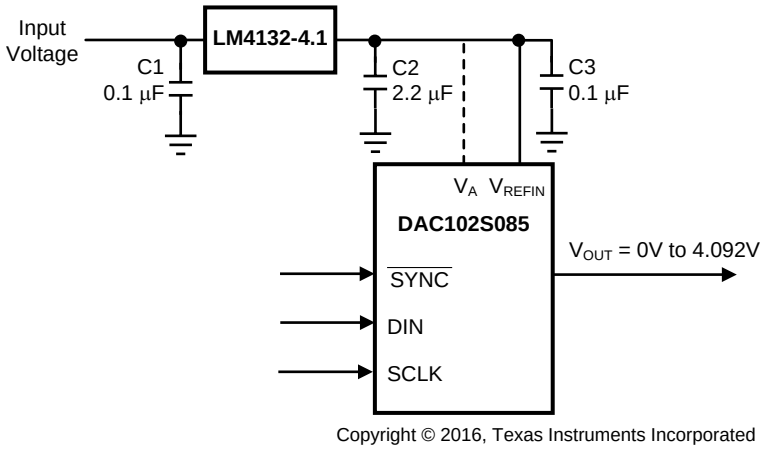


Figure 40. The LM4130 as a Power Supply

10.1.2 LM4050

Available with accuracy of 0.44%, the LM4050 shunt reference is also a good choice as a reference for the DAC102S085. It is available in 4.096-V and 5-V versions and comes in a space-saving 3-pin SOT-23 package.

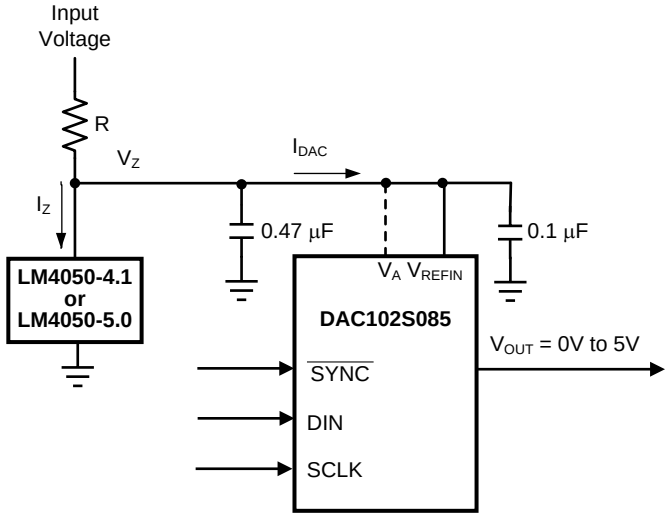


Figure 41. The LM4050 as a Power Supply

The minimum resistor value in the circuit of Figure 41 must be chosen such that the maximum current through the LM4050 does not exceed its 15-mA rating. The conditions for maximum current include the input voltage at its maximum, the LM4050 voltage at its minimum, and the DAC102S085 drawing zero current. The maximum resistor value must allow the LM4050 to draw more than its minimum current for regulation plus the maximum DAC102S085 current in full operation. The conditions for minimum current include the input voltage at its minimum, the LM4050 voltage at its maximum, the resistor value at its maximum due to tolerance, and the DAC102S085 draws its maximum current. Equation 4 and Equation 5 summarize these conditions.

$$R(min) = (V_{IN}(max) - V_Z(min)) / I_Z(max) \quad (4)$$

$$R(max) = (V_{IN}(min) - V_Z(max)) / ((I_{DAC}(max) + I_Z(min))$$

where

- $V_Z(min)$ and $V_Z(max)$ are the nominal LM4050 output voltages ± the LM4050 output tolerance over temperature

Using References as Power Supplies (continued)

- I_Z(max) is the maximum allowable current through the LM4050
- I_Z(min) is the minimum current required by the LM4050 for proper regulation
- I_{DAC}(max) is the maximum DAC102S085 supply current (5)

10.1.3 LP3985

The LP3985 is a low-noise, ultra-low dropout voltage regulator with a 3% accuracy over temperature. It is a good choice for applications that do not require a precision reference for the DAC102S085. It comes in 3-V, 3.3-V and 5-V versions, among others, and sports a low 30-µV noise specification at low frequencies. Because low frequency noise is relatively difficult to filter, this specification could be important for some applications. The LP3985 comes in a space-saving 5-pin SOT-23 and 5-bump DSBGA packages.

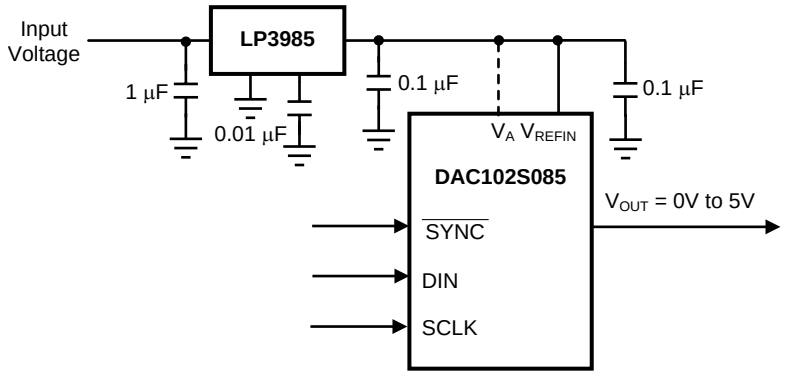


Figure 42. Using the LP3985 Regulator

An input capacitance of 1 µF without any ESR requirement is required at the LP3985 input, while a 1-µF ceramic capacitor with an ESR requirement of 5 mΩ to 500 mΩ at the output. Careful interpretation and understanding of the capacitor specification is required to ensure correct device operation.

10.1.4 LP2980

The LP2980 is an ultra-low dropout regulator with a 0.5% or 1% accuracy over temperature, depending upon grade. It is available in 3-V, 3.3-V and 5-V versions, among others.

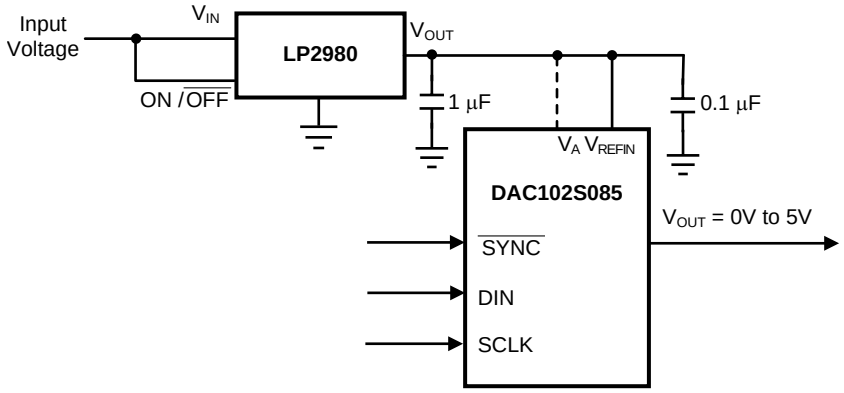


Figure 43. Using the LP2980 Regulator

Using References as Power Supplies (continued)

Like any low dropout regulator, the LP2980 requires an output capacitor for loop stability. This output capacitor must be at least 1 µF over temperature, but values of 2.2 µF or more provide even better performance. The ESR of this capacitor should be within the range specified in the LP2980 data sheet (SNOS733). Surface-mount solid tantalum capacitors offer a good combination of small size and ESR. Ceramic capacitors are attractive due to their small size but generally have ESR values that are too low for use with the LP2980. Aluminum electrolytic capacitors are typically not a good choice due to their large size and have ESR values that may be too high at low temperatures.

11 Layout

11.1 Layout Guidelines

For best accuracy and minimum noise, the printed-circuit board containing the DAC102S085 should have separate analog and digital areas. The areas are defined by the locations of the analog and digital power planes. Both of these planes should be located in the same board layer. There should be a single ground plane. A single ground plane is preferred if digital return current does not flow through the analog ground area. Frequently a single ground plane design uses a *fencing* technique to prevent the mixing of analog and digital ground current. Separate ground planes must only be used when the fencing technique is inadequate. The separate ground planes must be connected in one place, preferably near the DAC102S085. Special care is required to ensure that digital signals with fast edge rates do not pass over split ground planes. They must always have a continuous return path below their traces.

The DAC102S085 power supply should be bypassed with a 10-µF and a 0.1-µF capacitor as close as possible to the device with the 0.1-µF capacitor right at the device supply pin. The 10-µF capacitor should be a tantalum type and the 0.1-µF capacitor should be a low ESL, low ESR type. The power supply for the DAC102S085 should only be used for analog circuits.

Avoid crossover of analog and digital signals and keep the clock and data lines on the component side of the board. The clock and data lines should have controlled impedances.

11.2 Layout Example

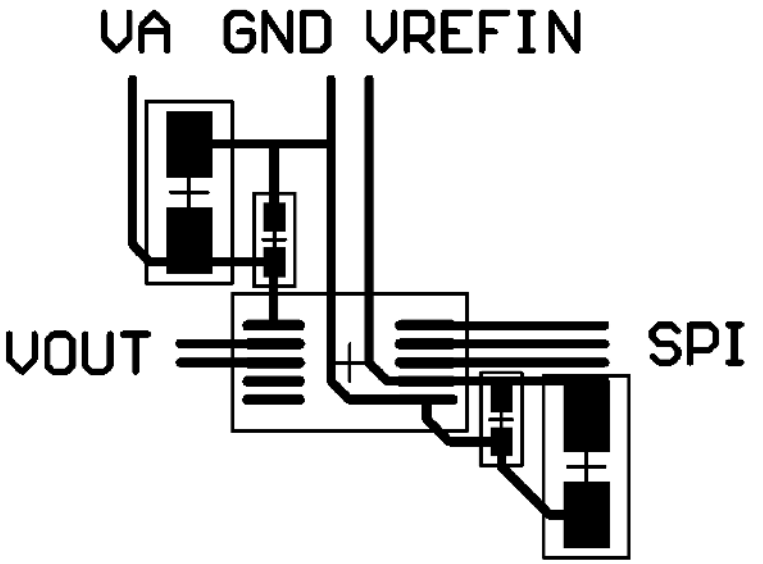


Figure 44. DAC102S085 Layout Diagram

12 Device and Documentation Support

12.1 Device Support

12.1.1 Device Nomenclature

12.1.1.1 Specification Definitions

DIFFERENTIAL NON-LINEARITY (DNL) The measure of the maximum deviation from the ideal step size of 1 LSB, which is V_{REF} / 1024 = V_A / 1024.

DAC-to-DAC CROSSTALK The glitch impulse transferred to a DAC output in response to a full-scale change in the output of another DAC.

DIGITAL CROSSTALK The glitch impulse transferred to a DAC output at mid-scale in response to a full-scale change in the input register of another DAC.

DIGITAL FEEDTHROUGH A measure of the energy injected into the analog output of the DAC from the digital inputs when the DAC outputs are not updated. It is measured with a full-scale code change on the data bus.

FULL-SCALE ERROR The difference between the actual output voltage with a full scale code (3FFh) loaded into the DAC and the value of $V_A \times 1023 / 1024$.

GAIN ERROR The deviation from the ideal slope of the transfer function. It can be calculated from Zero and Full-Scale Errors as GE = FSE - ZE, where GE is Gain error, FSE is Full-Scale Error and ZE is Zero Error.

GLITCH IMPULSE The energy injected into the analog output when the input code to the DAC register changes. It is specified as the area of the glitch in nanovolt-seconds.

INTEGRAL NON-LINEARITY (INL) A measure of the deviation of each individual code from a straight line through the input to output transfer function. The deviation of any given code from this straight line is measured from the center of that code value. The end point method is used. INL for this product is specified over a limited range, per the Electrical Tables.

LEAST SIGNIFICANT BIT (LSB) The bit that has the smallest value or weight of all bits in a word.

$$LSB = V_{REF} / 2^n \quad (6)$$

where

- V_{REF} is the supply voltage for this product
- n is the DAC resolution in bits, which is 10 for the DAC102S085

MAXIMUM LOAD CAPACITANCE The maximum capacitance that can be driven by the DAC with output stability maintained.

MONOTONICITY The condition of being monotonic, where the DAC has an output that never decreases when the input code increases.

MOST SIGNIFICANT BIT (MSB) The bit that has the largest value or weight of all bits in a word.

Its value is 1/2 of V_A.

MULTIPLYING BANDWIDTH The frequency at which the output amplitude falls 3 dB below the input sine wave on V_{REFIN} with a full-scale code loaded into the DAC.

POWER EFFICIENCY The ratio of the output current to the total supply current. The output current comes from the power supply. The difference between the supply and output currents is the power consumed by the device without a load.

SETTLING TIME The time for the output to settle to within 1/2 LSB of the final value after the input code is updated.

TOTAL HARMONIC DISTORTION (THD) The measure of the harmonics present at the output of the DACs with an ideal sine wave applied to V_{REFIN}.

THD is measured in dB.

Device Support (continued)

WAKE-UP TIME The time for the output to exit power-down mode.

This is the time from the falling edge of the 16th SCLK pulse to when the output voltage deviates from the power-down voltage of 0 V.

ZERO CODE ERROR The output error, or voltage, present at the DAC output after a code of 000h has been entered.

12.2 Documentation Support

12.2.1 Related Documentation

For related documentation, see the following:

LP2980-N Micropower 50 mA Ultra Low-Dropout Regulator In SOT-23 Package (SNOS733)

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.
SPI is a trademark of Motorola, Inc..
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DAC102S085CIMM/NOPB	ACTIVE	VSSOP	DGS	10	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 105	X74C	Samples
DAC102S085CIMMX/NOPB	ACTIVE	VSSOP	DGS	10	3500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 105	X74C	Samples
DAC102S085CISD/NOPB	ACTIVE	WSON	DSC	10	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 105	X75C	Samples
DAC102S085CISDX/NOPB	ACTIVE	WSON	DSC	10	4500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 105	X75C	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

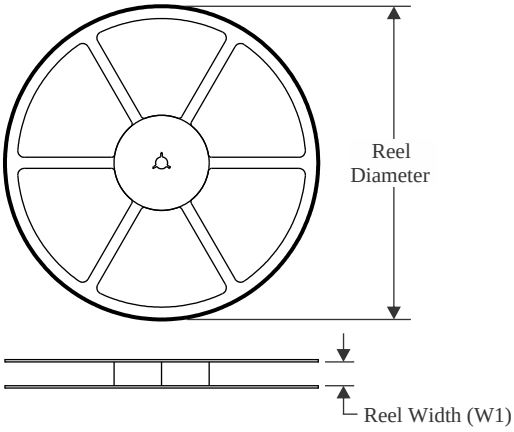
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

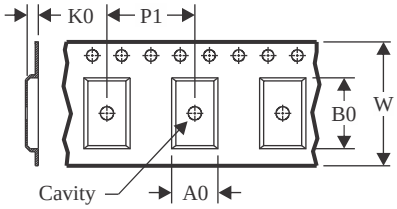
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

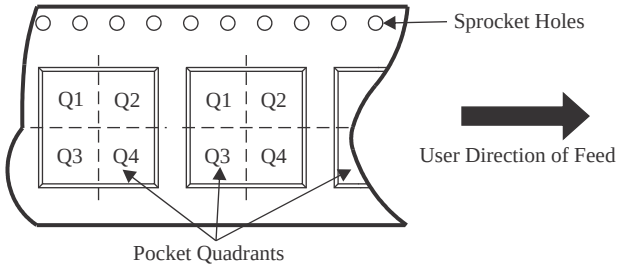


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

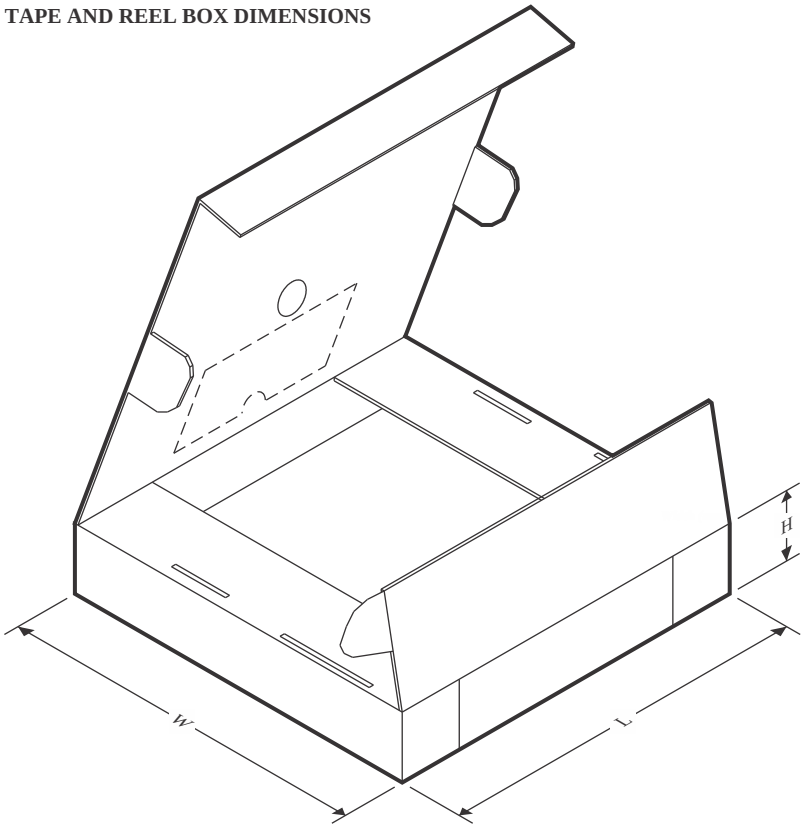
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC102S085CIMM/NOPB	VSSOP	DGS	10	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
DAC102S085CIMMX/ NOPB	VSSOP	DGS	10	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
DAC102S085CISD/NOPB	WSON	DSC	10	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
DAC102S085CISDX/ NOPB	WSON	DSC	10	4500	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

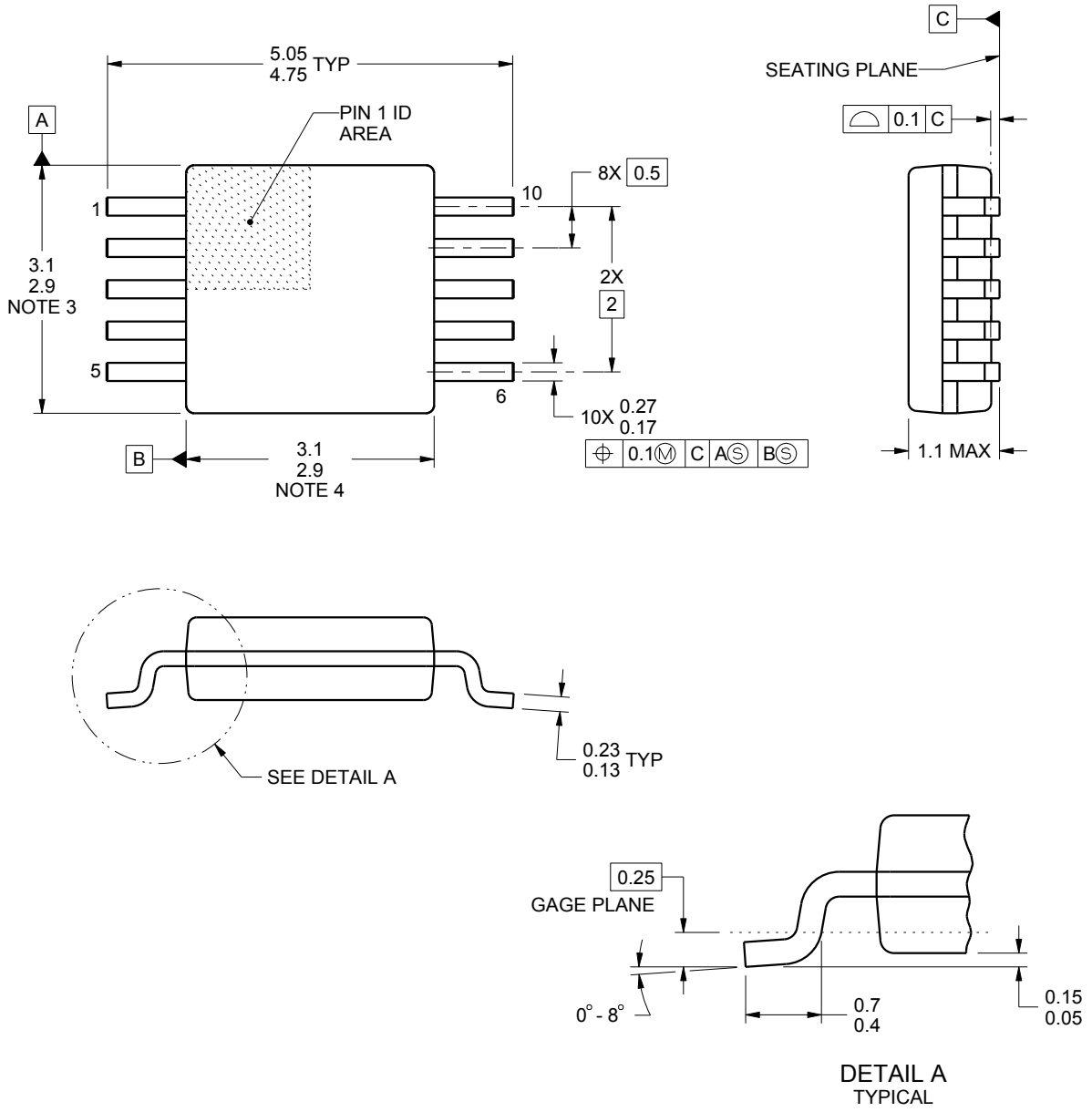
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC102S085CIMM/NOPB	VSSOP	DGS	10	1000	210.0	185.0	35.0
DAC102S085CIMMX/ NOPB	VSSOP	DGS	10	3500	367.0	367.0	35.0
DAC102S085CISD/NOPB	WSON	DSC	10	1000	210.0	185.0	35.0
DAC102S085CISDX/ NOPB	WSON	DSC	10	4500	367.0	367.0	35.0

PACKAGE OUTLINE

DGS0010A

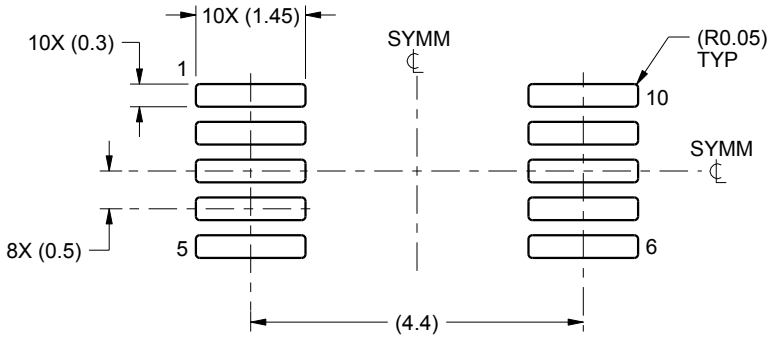
VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

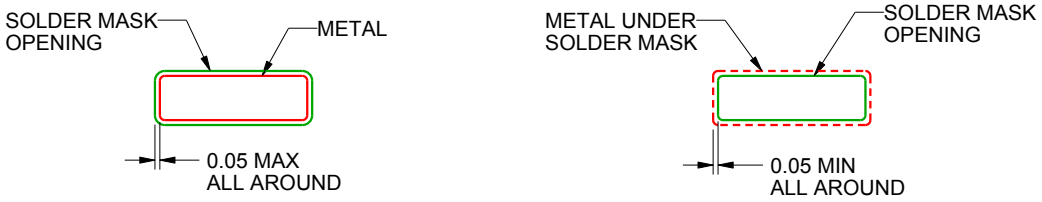


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X

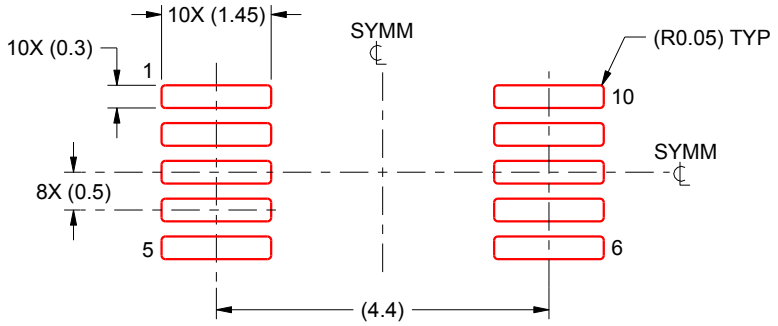


SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



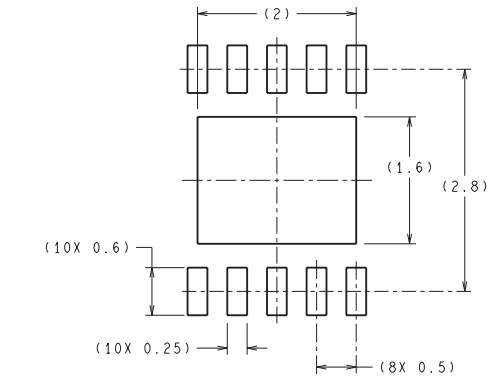
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

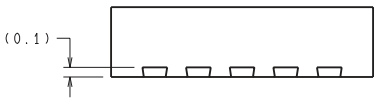
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

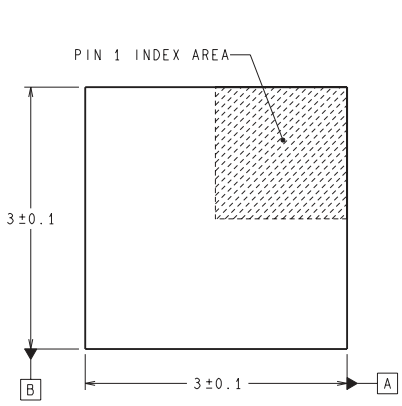
DSC0010A

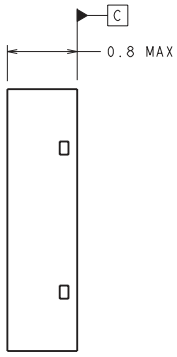


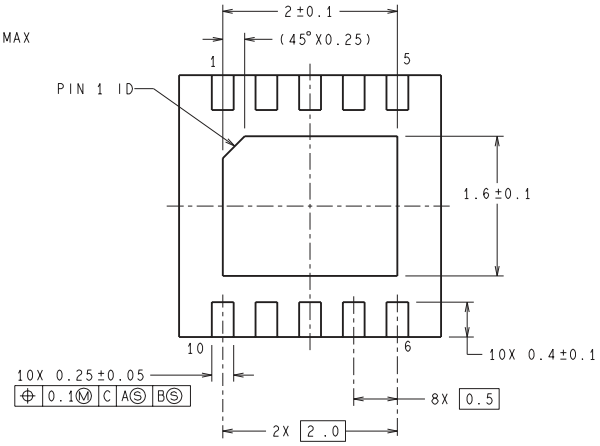
RECOMMENDED LAND PATTERN

DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY









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