



November 2013

# FDP150N10A N-Channel PowerTrench<sup>®</sup> MOSFET 100 V, 50 A, 15 mΩ



## Features

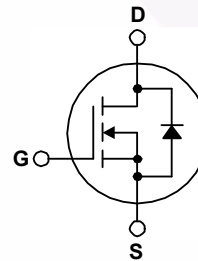
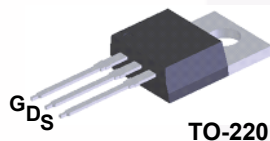
- $R_{DS(on)} = 12.5 \text{ m}\Omega$  (Typ.) @  $V_{GS} = 10 \text{ V}$ ,  $I_D = 50 \text{ A}$
- Fast Switching Speed
- Low Gate Charge,  $Q_G = 16.2 \text{ nC}$  (Typ.)
- High Performance Trench Technology for Extremely Low  $R_{DS(on)}$
- High Power and Current Handling Capability
- RoHS Compliant

## Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench<sup>®</sup> process that has been tailored to minimize the on-state resistance while maintaining superior switching performance.

## Applications

- Synchronous Rectification for ATX / Server / Telecom PSU
- Motor Drives and Uninterruptible Power Supplies
- Micro Solar Inverter



## Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	FDP150N10A_F102	Unit
$V_{DSS}$	Drain to Source Voltage	100	V
$V_{GSS}$	Gate to Source Voltage	$\pm 20$	V
$I_D$	Drain Current	- Continuous ( $T_C = 25^\circ\text{C}$ )	50
		- Continuous ( $T_C = 100^\circ\text{C}$ )	36
$I_{DM}$	Drain Current	- Pulsed (Note 1)	200
$E_{AS}$	Single Pulsed Avalanche Energy	(Note 2)	84.6
$dv/dt$	Peak Diode Recovery $dv/dt$	(Note 3)	6.0
$P_D$	Power Dissipation	( $T_C = 25^\circ\text{C}$ )	91
		- Derate Above $25^\circ\text{C}$	0.61
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +175	$^\circ\text{C}$
$T_L$	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds	300	$^\circ\text{C}$

## Thermal Characteristics

Symbol	Parameter	FDP150N10A_F102	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	1.6	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	62.5	

FDP150N10A — N-Channel PowerTrench<sup>®</sup> MOSFET

## Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FDP150N10A_F102	FDP150N10A	TO-220	Tube	N/A	N/A	50 units

## Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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### Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250 \mu\text{A}, V_{GS} = 0 \text{ V}$	100	-	-	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$ , Referenced to $25^\circ\text{C}$	-	0.08	-	$\text{V}/^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 80 \text{ V}, V_{GS} = 0 \text{ V}$	-	-	1	$\mu\text{A}$
		$V_{DS} = 80 \text{ V}, T_C = 150^\circ\text{C}$	-	-	500	
$I_{GSS}$	Gate to Body Leakage Current	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$	-	-	$\pm 100$	nA

### On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250 \mu\text{A}$	2.0	-	4.0	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10 \text{ V}, I_D = 50 \text{ A}$	-	12.5	15.0	m $\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = 10 \text{ V}, I_D = 50 \text{ A}$	-	40	-	S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 50 \text{ V}, V_{GS} = 0 \text{ V},$ $f = 1 \text{ MHz}$	-	1080	1440	pF
$C_{oss}$	Output Capacitance		-	267	355	pF
$C_{rss}$	Reverse Transfer Capacitance		-	11	-	pF
$C_{oss(er)}$	Energy Related Output Capacitance	$V_{DS} = 50 \text{ V}, V_{GS} = 0 \text{ V}$	-	436	-	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	$V_{DS} = 50 \text{ V}, V_{GS} = 10 \text{ V},$ $I_D = 50 \text{ A}$	-	16.2	21.0	nC
$Q_{gs}$	Gate to Source Gate Charge		-	5.3	-	nC
$Q_{gs2}$	Gate Charge Threshold to Plateau		-	2.6	-	nC
$Q_{gd}$	Gate to Drain "Miller" Charge		(Note 4)	-	3.7	-
ESR	Equivalent Series Resistance (G-S)	$f = 1 \text{ MHz}$	-	1.3	-	$\Omega$

### Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 50 \text{ V}, I_D = 50 \text{ A},$ $V_{GS} = 10 \text{ V}, R_G = 4.7 \Omega$	-	13	36	ns
$t_r$	Turn-On Rise Time		-	16	42	ns
$t_{d(off)}$	Turn-Off Delay Time		-	21	52	ns
$t_f$	Turn-Off Fall Time		(Note 4)	-	5	20

### Drain-Source Diode Characteristics

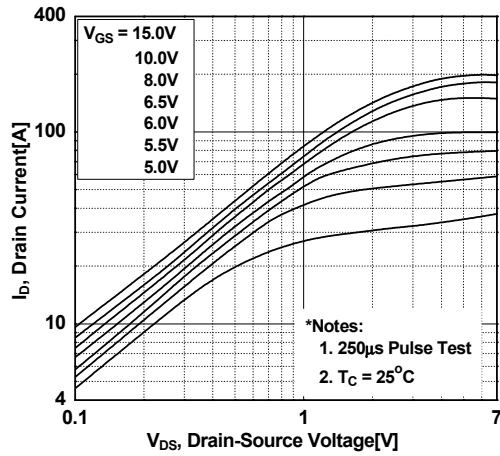
$I_S$	Maximum Continuous Drain to Source Diode Forward Current	-	-	50	A	
$I_{SM}$	Maximum Pulsed Drain to Source Diode Forward Current	-	-	200	A	
$V_{SD}$	Drain to Source Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_{SD} = 50 \text{ A}$	-	-	1.3	V
$t_{rr}$	Reverse Recovery Time	$V_{GS} = 0 \text{ V}, V_{DD} = 50 \text{ V}, I_{SD} = 50 \text{ A},$ $di_F/dt = 100 \text{ A}/\mu\text{s}$	-	50	-	ns
$Q_{rr}$	Reverse Recovery Charge		-	55	-	nC

#### Notes:

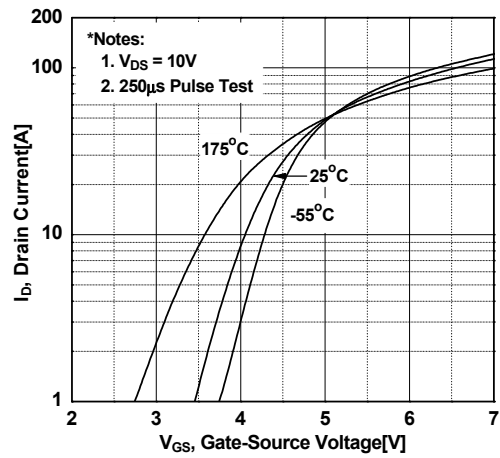
1. Repetitive rating; pulse-width limited by maximum junction temperature.
2.  $L = 2 \text{ mH}, I_{AS} = 9.2 \text{ A}, R_G = 25 \Omega$ , starting  $T_J = 25^\circ\text{C}$ .
3.  $I_{SD} \leq 100 \text{ A}, di/dt \leq 200 \text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$ , starting  $T_J = 25^\circ\text{C}$ .
4. Essentially independent of operating temperature typical characteristics.

## Typical Performance Characteristics

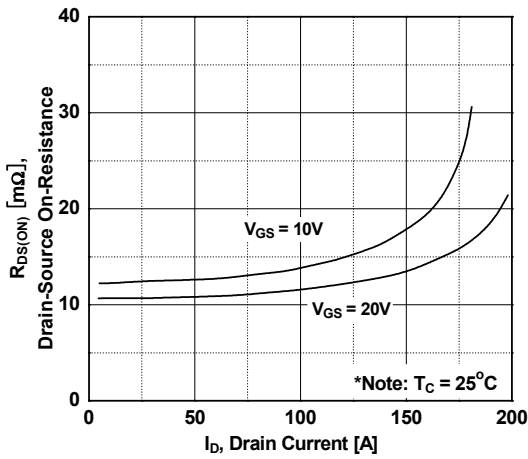
**Figure 1. On-Region Characteristics**



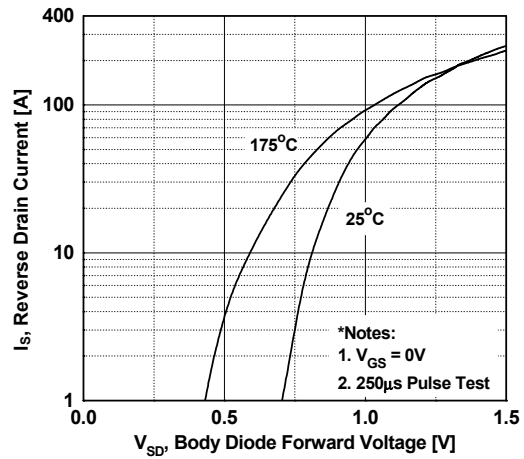
**Figure 2. Transfer Characteristics**



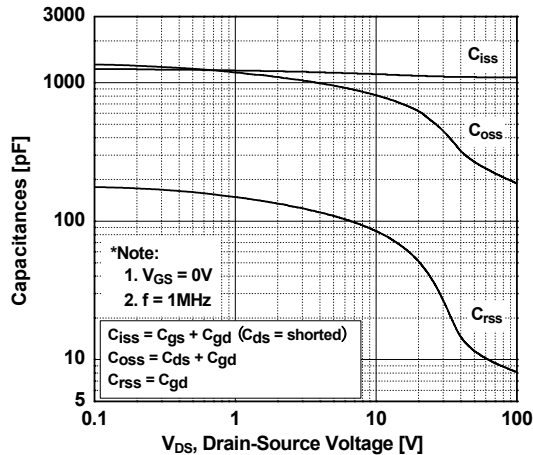
**Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage**



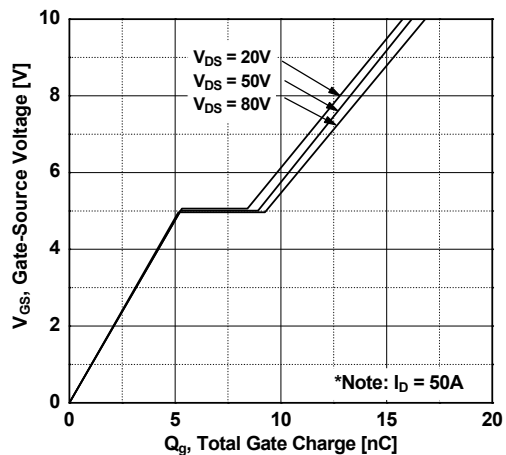
**Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature**



**Figure 5. Capacitance Characteristics**

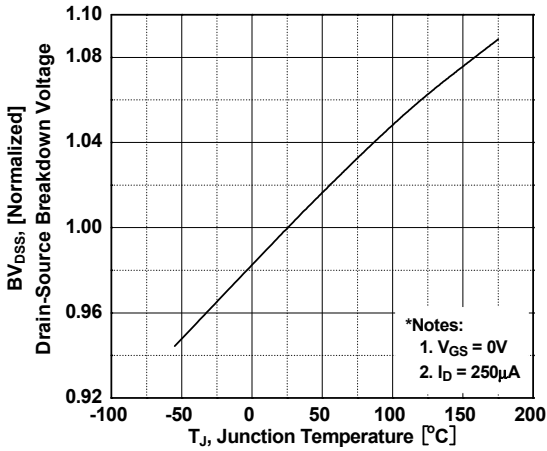


**Figure 6. Gate Charge Characteristics**

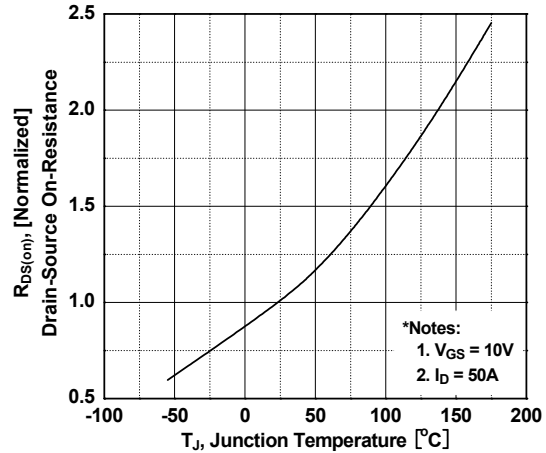


**Typical Performance Characteristics** (Continued)

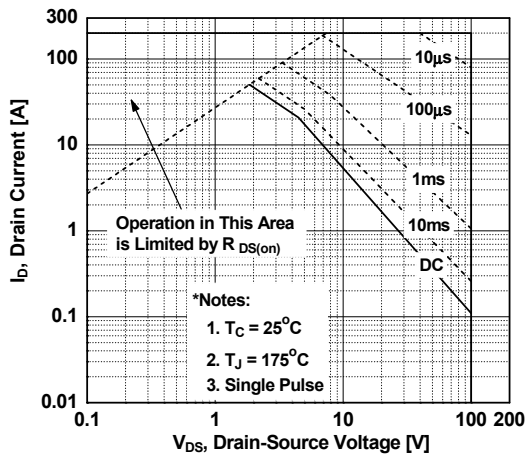
**Figure 7. Breakdown Voltage Variation vs. Temperature**



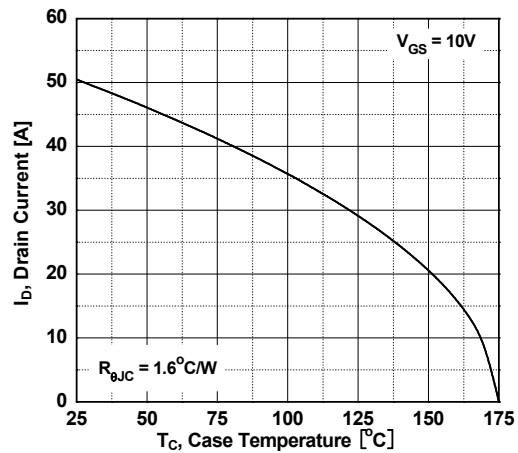
**Figure 8. On-Resistance Variation vs. Temperature**



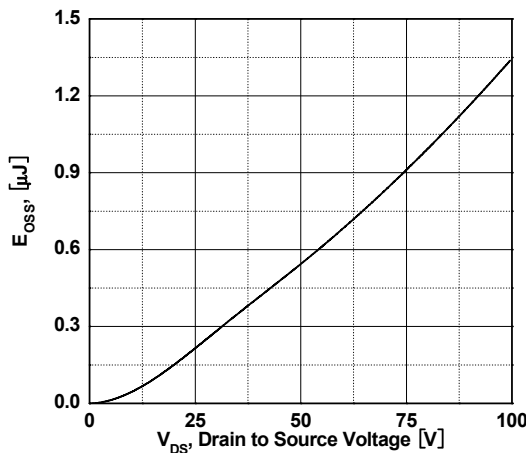
**Figure 9. Maximum Safe Operating Area**



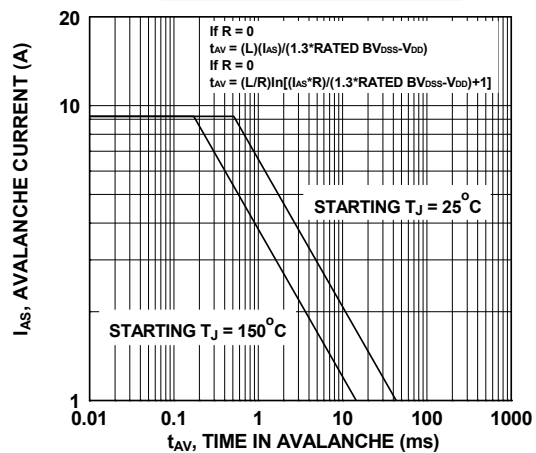
**Figure 10. Maximum Drain Current vs. Case Temperature**



**Figure 11. E\_oss vs. Drain to Source Voltage**

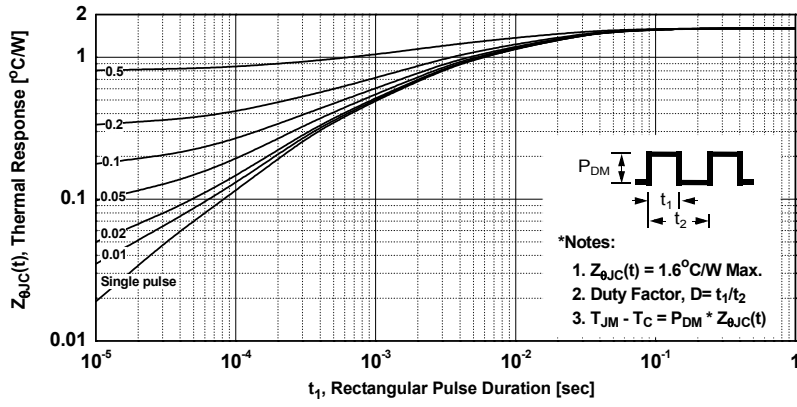


**Figure 12. Unclamped Inductive Switching Capability**



Typical Performance Characteristics (Continued)

Figure 13. Transient Thermal Response Curve



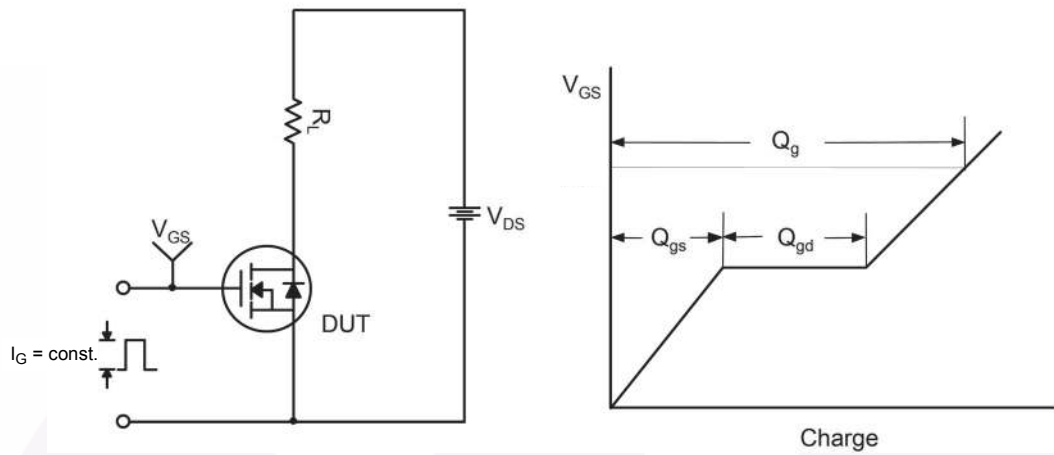


Figure 14. Gate Charge Test Circuit & Waveform

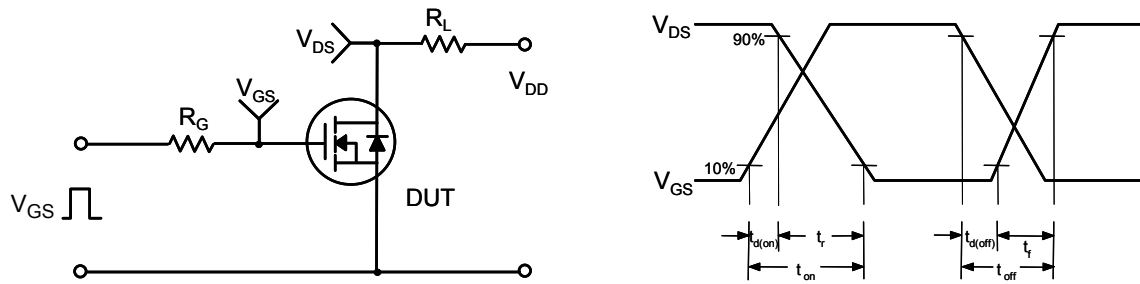


Figure 15. Resistive Switching Test Circuit & Waveforms

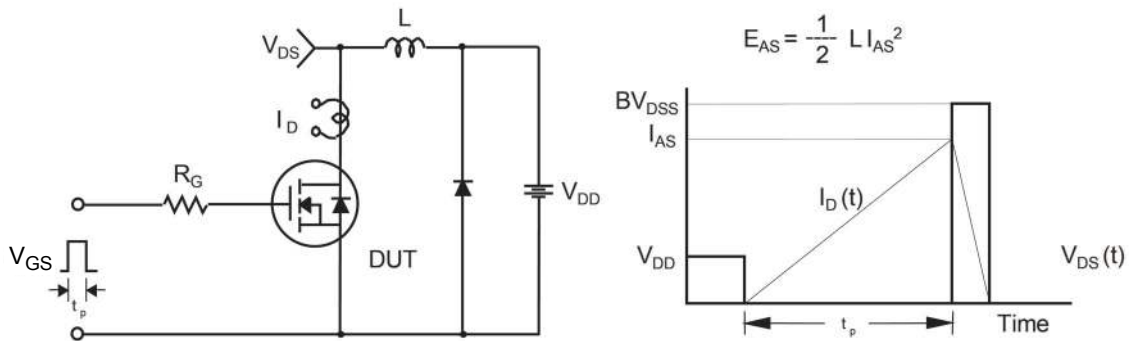


Figure 16. Unclamped Inductive Switching Test Circuit & Waveforms

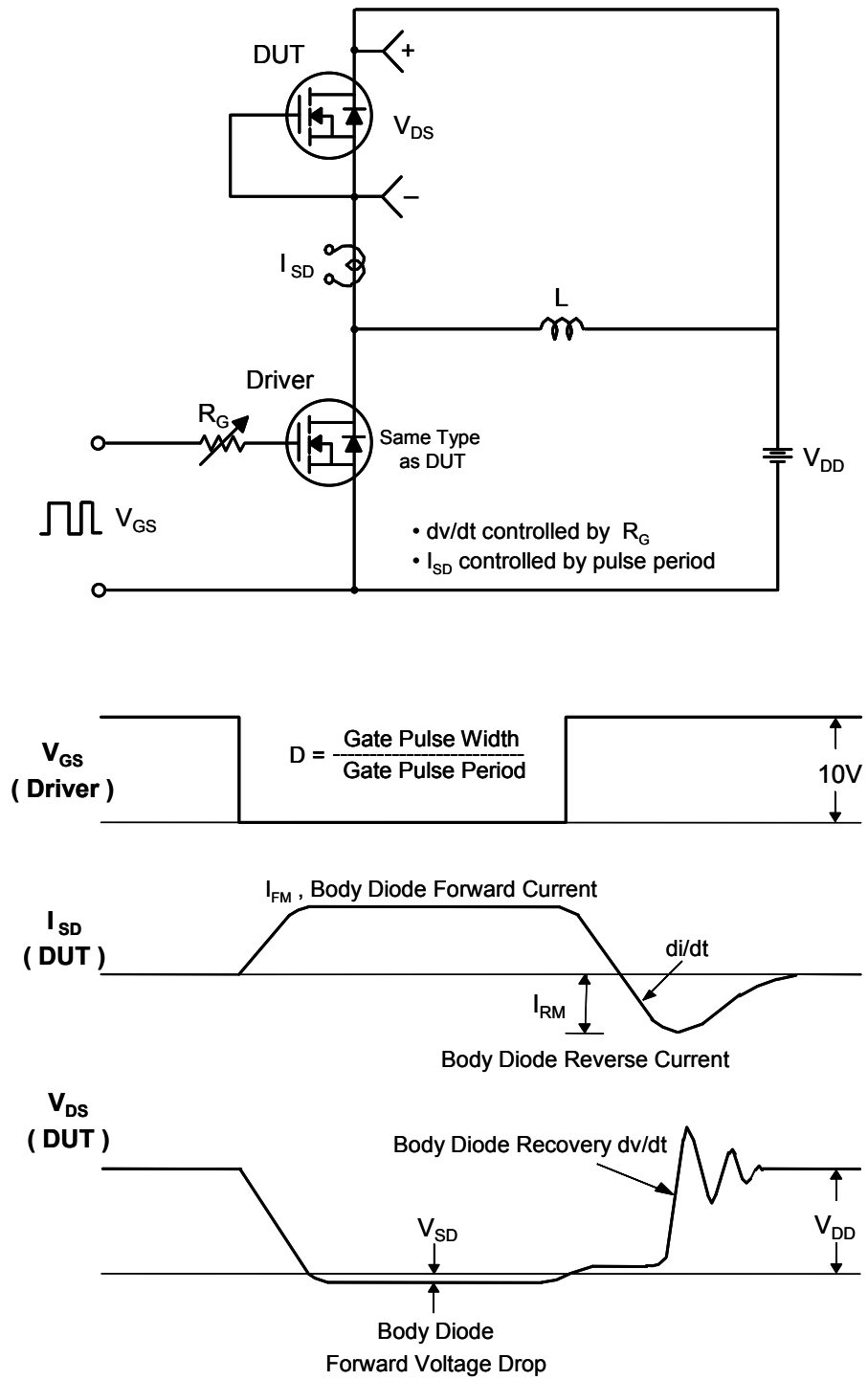
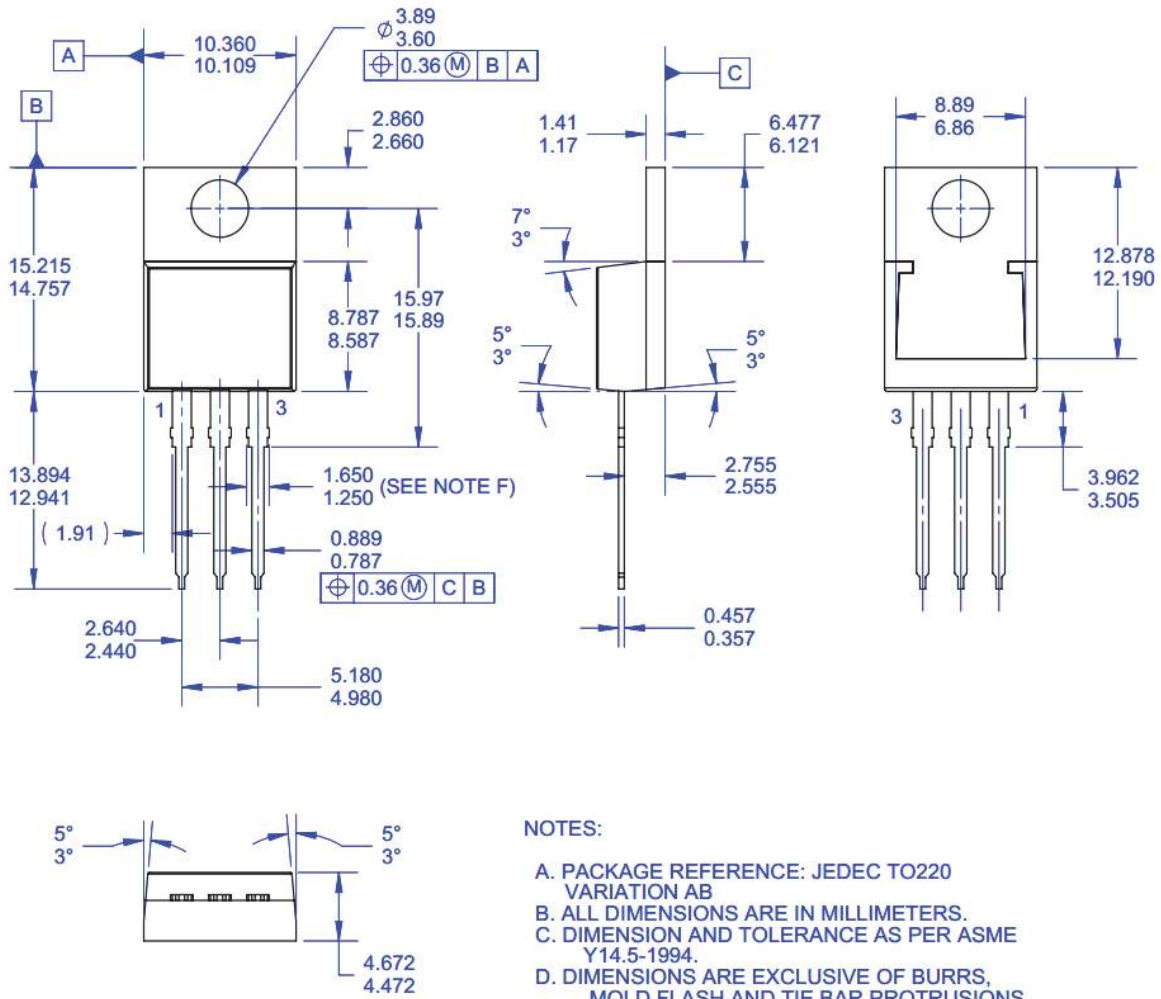


Figure 17. Peak Diode Recovery  $dv/dt$  Test Circuit & Waveforms

## Mechanical Dimensions



**Figure 18. TO-220, Molded, 3-Lead, Jedec Variation AB (Delta)**

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Rev. I68