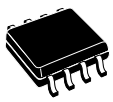
A6932H1.2

2 A ULDO linear regulator for automotive applications

Datasheet - production data



HSOP-8

Features

- AEC-Q100 compliant
- 2 V to 14 V input voltage range
- 200 mΩ $R_{DS(on)}$ max.
- 200 µA quiescent current at any load
- Excellent load and line regulation
- Adjustable from 1.2 V to 5 V
- 1% voltage regulation accuracy
- Short-circuit protection
- Thermal shutdown
- HSOP-8 package

Applications

- Dedicated to automotive applications

Description

The A6932H1.2 ultra low drop output linear regulator operates from 2 V to 14 V and is able to support output current up to 2 A. Designed with an internal 50 mΩ N-channel MOSFET, it can be used for on-board DC-DC conversions saving in real estate, list of components, low noise generation and power dissipation.

The A6932H1.2 device is available as adjustable version from 1.2 V to 5 V with a voltage regulation accuracy of 1%.

The upper current limit is fixed at 2.5 A to control the current in short-circuit condition within ± 8%. The current is sensed in the power MOS in order to limit the power dissipation.

The device is also provided with a thermal shutdown that limits the internal temperature at 150 °C with a hysteresis of 20 °C. The A6932H1.2 device provides the enable and the Power Good functions.

Figure 1. Typical operating circuit

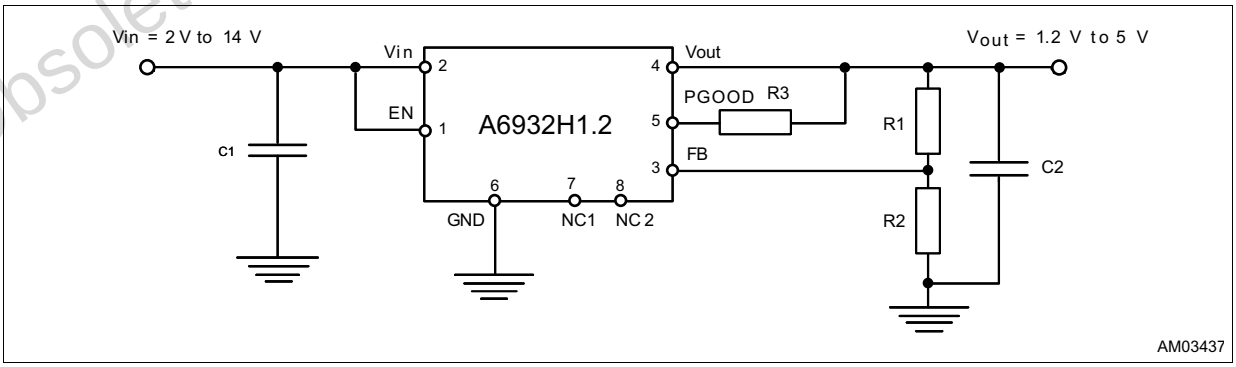


Table 1. Device summary

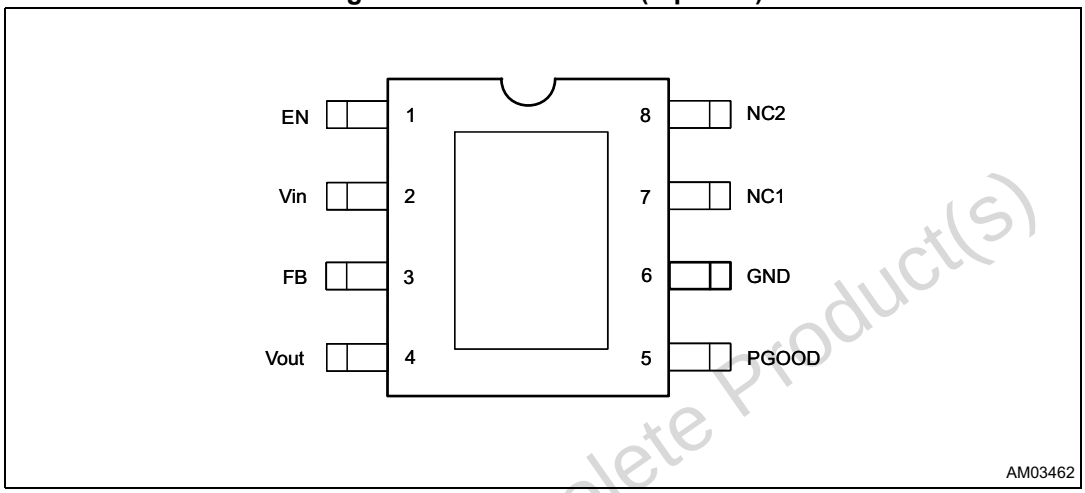
Part number	Package	Packaging
A6932H1.2	HSOP-8	Tube
A6932H1.2TR	HSOP-8	Tape and reel

Contents

1 Pin settings

1.1 Pin connection

Figure 2. Pin connection (top view)



1.2 Pin description

Table 2. Pin description

Name	Pin no.	Description
1	EN	Enables the device when connected to Vin and disables it when forced to GND.
2	VIN	Supply voltage. This pin is connected to the drain of the internal N-MOS. Connect this pin to a capacitor larger than 10 µF.
3	FB	Connecting this pin to a voltage divider it is possible to program the output voltage between 1.2 V and 5 V.
4	VOUT	Regulated output voltage. This pin is connected to the source of the internal N-MOS. Connect this pin to a capacitor of 10 µF.
5	PGOOD	Power Good output. The pin is open drain and detects the output voltage. It is forced low if the output voltage is lower than 90% of the programmed voltage.
6	GND	Ground pin
7, 8	NC1 - NC2	Internally not connected.

2 Maximum ratings

2.1 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{IN}	VIN and PGOOD	14.5	V
	EN, OUT and ADJ	-0.3 to (Vin +0.3)	V

2.2 Thermal data

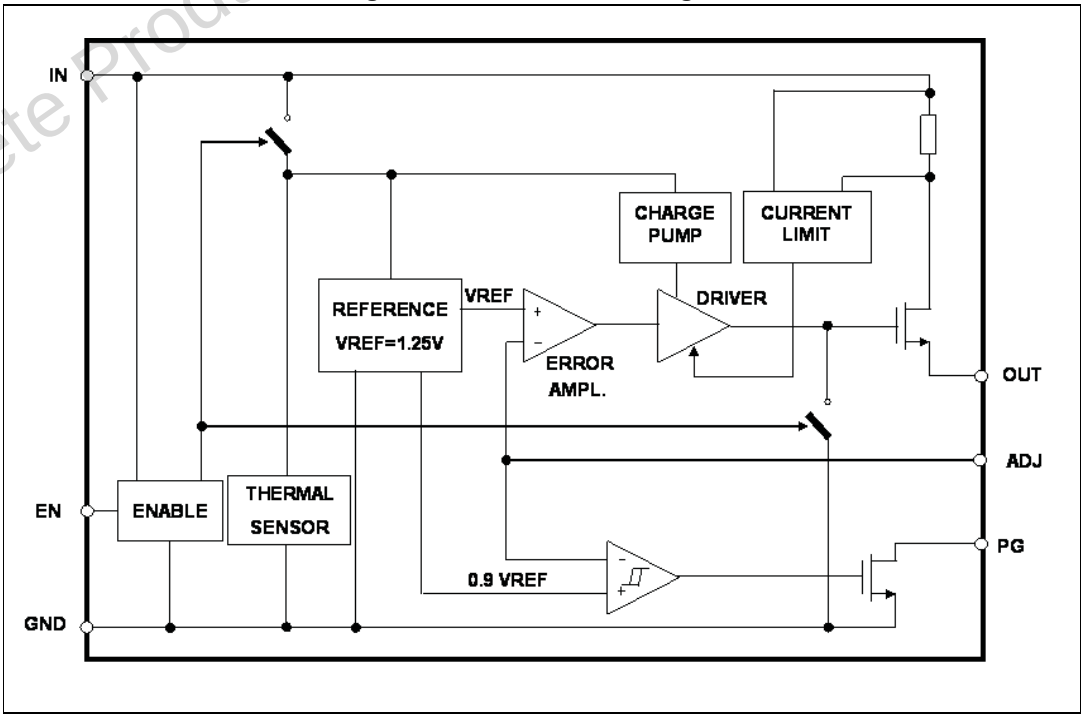
Table 4. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Maximum thermal resistance junction ambient	34(1)	°C/W
T_{MAX}	Maximum junction temperature	150	°C
T_{STG}	Storage temperature range	-65 to 150	°C

1. Package mounted on board.

3 Block diagram

Figure 3. Internal block diagram



4 Electrical characteristics

Table 5. Electrical characteristics (T_a = -40 °C to 85 °C, V_{IN} = 5 V unless otherwise specified)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{IN}	Operating supply voltage		2		14	V
V_O	Output voltage	T_a = 25 °C	1.188	1.2	1.212	V
			1.175		1.212	
	Line regulation	V_{IN} = 2.5 V ± 10%; I_O = 10 mA			5	mV
		V_{IN} = 3.3 V ± 10%; I_O = 10 mA			5	mV
		V_{IN} = 5 V ± 10%; I_O = 10 mA			5	mV
	Load regulation	V_{IN} = 3.3 V; 0.1 A < I_O < 2 A			15	mV
$R_{DS(on)}$	Drain source ON resistance				200	mΩ
I_{OCC}	Current limiting	T_a = 25 °C	2.3	2.5	2.7	A
					2.85	
Iq	Quiescent current			0.2	0.4	mA
Ish	Shutdown current	T_a = 25 °C			25	µA
					29	
	Ripple rejection	f = 120 Hz, I_O = 1 A V_{IN} = 5 V, ΔV_{IN} = 2 Vpp	60	75		dB
Ven	EN input threshold		0.5	0.65	0.8	V
	Pgood threshold	Vo rise		90		%Vo
	Pgood hysteresis			10		%Vo
	Pgood saturation	Ipgood = 1 mA		0.2	0.4	V

5 Typical electrical performance

Figure 4. Output voltage vs. junction temperature

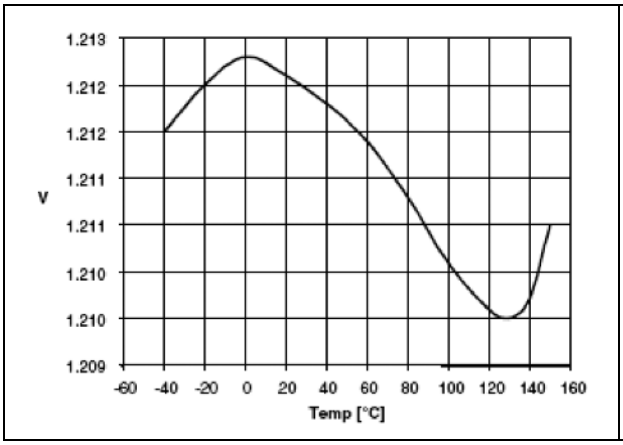


Figure 5. Quiescent current vs. junction temperature

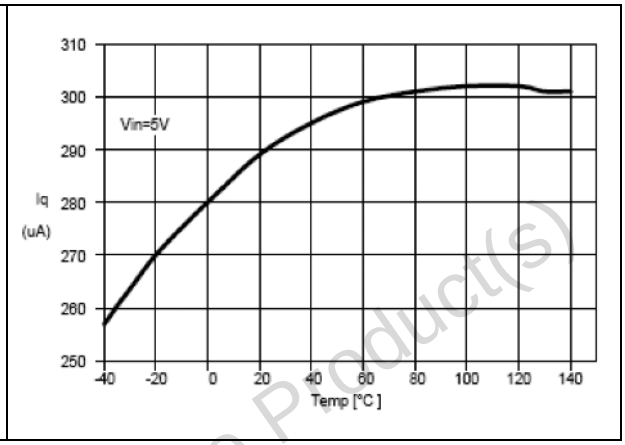
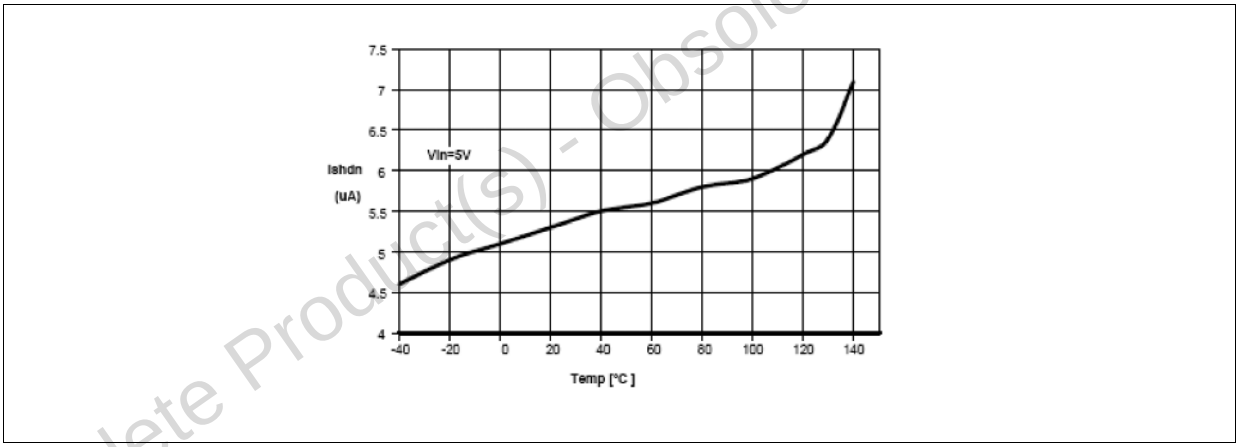


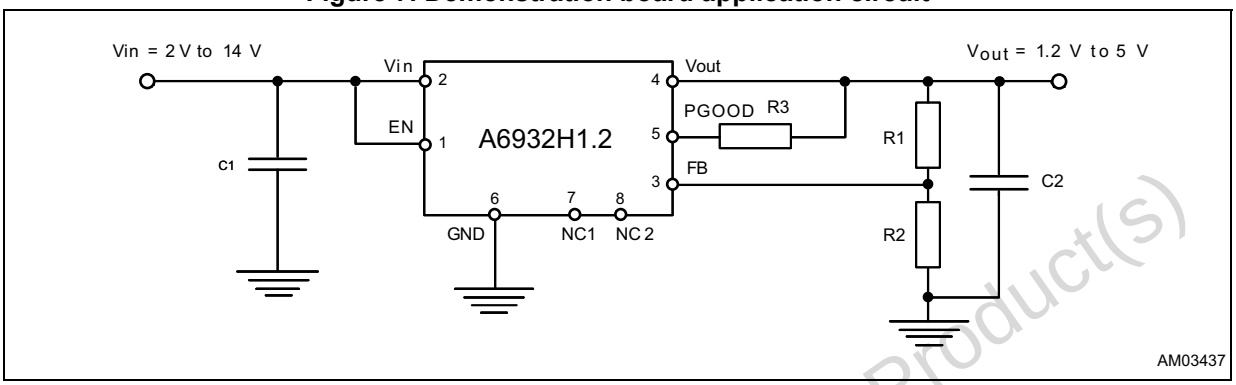
Figure 6. Shutdown current vs. junction temperature



6 Application information

6.1 Application circuit

Figure 7. Demonstration board application circuit

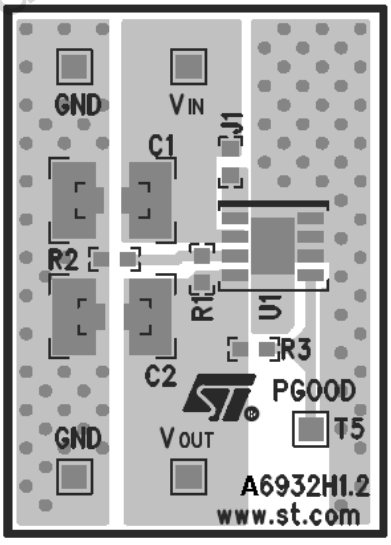


Equation 1

$$V_{OUT} = \frac{1.2}{R_2} \times (R_1 + R_2)$$

6.2 Demonstration board layout

Figure 8. Demonstration board layout



6.3 Component part list

Table 6. Component part list

Reference	Part number	Description	Manufacturer
C1	GRM32ER6C226KE20B	22 µF, 16 V	Murata
C2	GRM32ER6C226KE20B	22 µF, 16 V	Murata
R1		N. M.	
R2		0 Ω	
R3		100 KΩ	

7 Component selection

7.1 Input capacitor

The input capacitor value depends on a lot of factors such as load transient requirements, input source (battery or DC/DC converter) and its distance from the input cap. Usually a 47 µF is enough for any application but a much lower value can be sufficient in many cases.

7.2 Output capacitor

The output capacitor choice depends basically on the load transient requirements. Tantalum, Special Polymer, POSCAP and aluminum capacitors are good and offer very low ESR values. Multilayer ceramic caps have the lowest ESR and can be required for particular applications. Nevertheless in several applications they are OK, the loop stability issue has to be considered (see loop stability section).

In *Table 7* is a list of some suggested capacitor manufacturers.

Table 7. Suggested capacitor

Manufacturer	Type	Cap value (µF)	Rated voltage (V)
Murata	Ceramic	1 to 47	4 to 16
Panasonic	Ceramic	1 to 47	4 to 16
TAIYO YUDEN	Ceramic	1 to 47	4 to 16
TDK	Ceramic	1 to 47	4 to 16
TOKIN	Ceramic	1 to 47	4 to 16
SANYO	POSCAP	1 to 47	4 to 16
Panasonic	SP	1 to 47	4 to 16
KEMET	Tantalum	1 to 47	4 to 16

7.3 Loop stability

The stability of the loop is affected by the zero introduced by the output capacitor. The time constant of the zero is given by:

Equation 2

$$T = ESR \times C_{OUT}$$

Equation 3

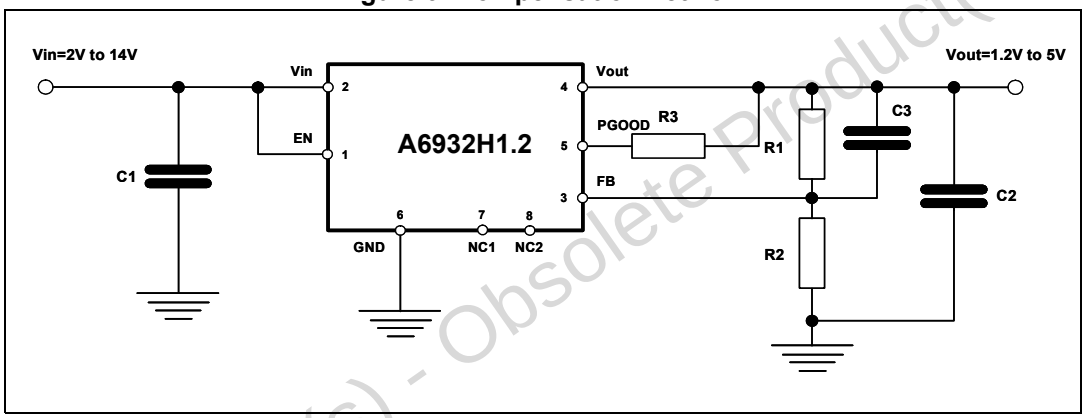
$$F_{ZERP} = \frac{1}{2\pi \times ESR \times C_{OUT}}$$

This zero helps to increase the phase margin of the loop until the time constant is higher than some hundreds of ns, depending also on the output voltage and current.

So, using very low ESR ceramic capacitors could produce oscillations at the output, in particular when regulating high output voltages (adjustable version).

To solve this issue is sufficient to add a small capacitor (e.g. 1 nF to 10 nF) in parallel to the high side resistor of the external divider, as shown in *Figure 9*.

Figure 9. Compensation network



The thermal resistance junction to ambient of the demonstration board is approximately 34 °C/W.

This mean that, considering an ambient temperature of 60 °C and, a maximum junction temperature of 150 °C, the maximum power that the device can handle is 2.7 W.

This means that the device is able to deliver a DC output current of 2 A only with a very low dropout.

8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

Figure 10. HSOP-8 package outline

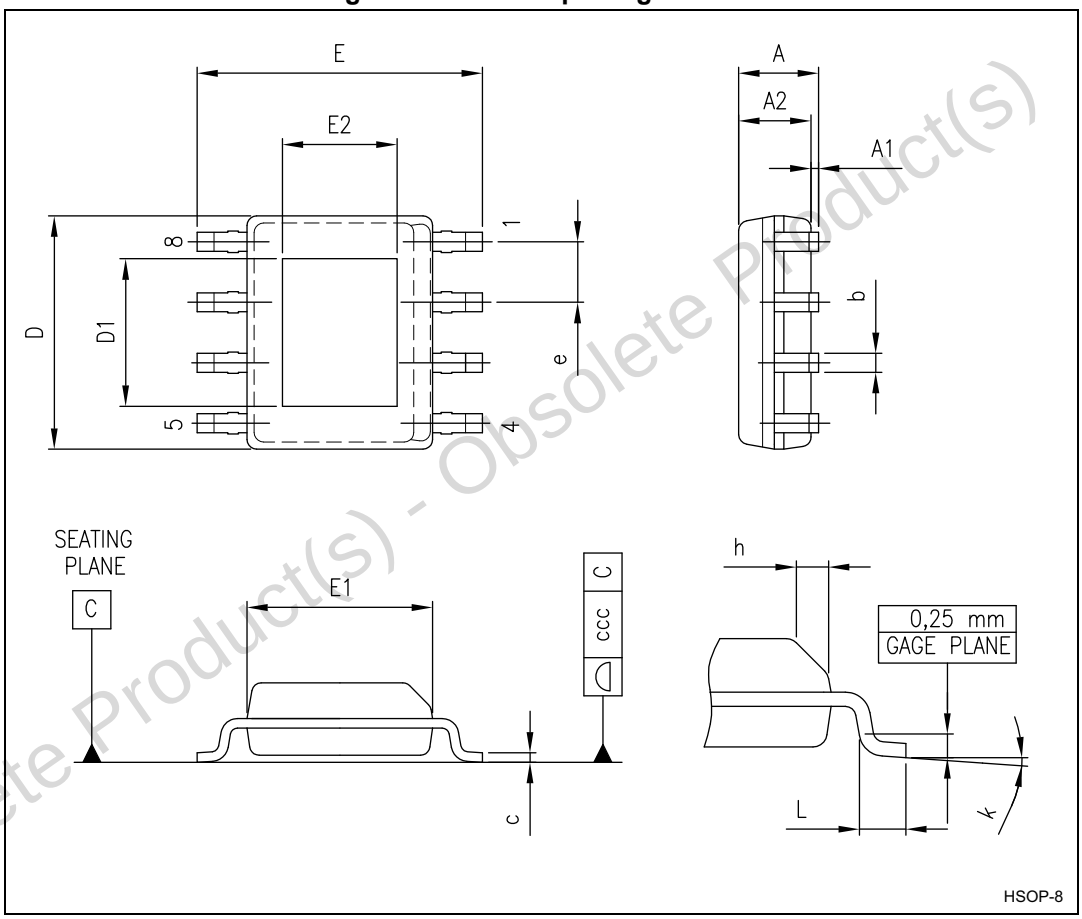


Table 8. HSOP-8 package mechanical data

Symbol	Dimensions (mm)			Note
	Min.	Typ.	Max.	
A	1.43	1.55	1.68	
A1	0.03	0.08	0.13	
A2	1.40	1.47	1.55	
b	0.35	0.41	0.49	
c	0.19	0.20	0.25	
D	4.80	4.93	4.98	(1)
D1	According to pad size			(2)
E	5.84	5.99	6.20	
E1	3.81	3.94	3.99	(3)
E2	According to pad size			(2)
e		1.27		
h	0.25	0.33	0.41	
L	0.41	0.64	0.89	
k	0	5	8	Degrees
ccc			0.10	

1. Dimension “D” does not include mold flash, protrusions or gate burrs.
2. The size of exposed pad is variable depending of leadframe design pad size. End user should verify “D1” and “E2” dimensions for each device application.
3. Dimension “E1” does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25 mm per side.

9 Revision history

Table 9. Document revision history

Date	Revision	Changes
29-Nov-2013	1	Initial release.

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