9A, 6.5V, 1MHz Synchronous Step-Down Converter

General Description

The RT5758 is a high-performance, synchronous step-down DC-DC converter that can deliver up to 9A output current from a 3V to 6.5V input supply. The device integrates low $R_{DS(ON)}$ power MOSFETs, accurate 0.6V reference and an integrated diode of bootstrap circuit to offer a very compact solution.

The RT5758 adopts Advanced Constant On-Time (ACOT^{TM}) control architecture that provides ultrafast transient response and further reduce the external-component count. In steady states, the ACOT^{TM} operates in nearly constant switching frequency over line, load and output voltage ranges and makes the EMI filter design easier.

The device offers Independent enable control input pin and power good indicator for easily sequence control. To control the inrush current during the startup, the device provides a programmable soft-start up by an external capacitor connected to the SS pin. Fully protection features are also integrated in the device including the cycle-by-cycle current limit control, UVP, input UVLO and OTP.

The RT5758 is available in a thermally enhanced UQFN-13L 3x3 (FC) package.

Features

- **Dramatically Fast Transient Response**
- **Steady 1MHz ±20% Switching Frequency**
- **1.5% Reference Voltage**
- **Advanced COT Control Loop**
- **Auto PWM/Pulse Skipping Mode for High Light-Load Efficiency**
- **Optimized for Ceramic Output Capacitors**
- **3V to 6.5V Input Voltage Range**
- **Integrated 12mΩ/8mΩ MOSFETs**
- **Pre-Biased Start Up**
- **Adjustable Soft-Start**
- **Power Good Indicator**
- **Enable Control**
- **Over-Current and Over-Temperature Protections**
- **Under-Voltage Protection with Hiccup Mode**

Applications

- Mobile Phones and Handheld Devices
- STB, Cable Modem, and xDSL Platform
- WLAN ASIC Power / Storage (SSD and HDD)
- General Purpose for POL LV Buck Converter
- TV

Ordering Information

RT5758 □ □

          └─ Package Type
              QUF : UQFN-13L 3x3 (FC) (U-Type)

     └─ Lead Plating System
            G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

‣ RoHS compliant and compatible with the current require-ments of IPC/JEDEC J-STD-020.
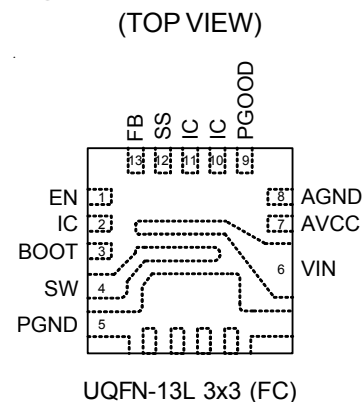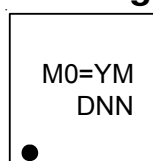
‣ Suitable for use in SnPb or Pb-free soldering processes.

Pin Configuration

(TOP VIEW)

UQFN-13L 3x3 (FC)

Marking Information

M0=YM
DNN

M0= : Product Code
YMDNN : Date Code

Typical Application Circuit
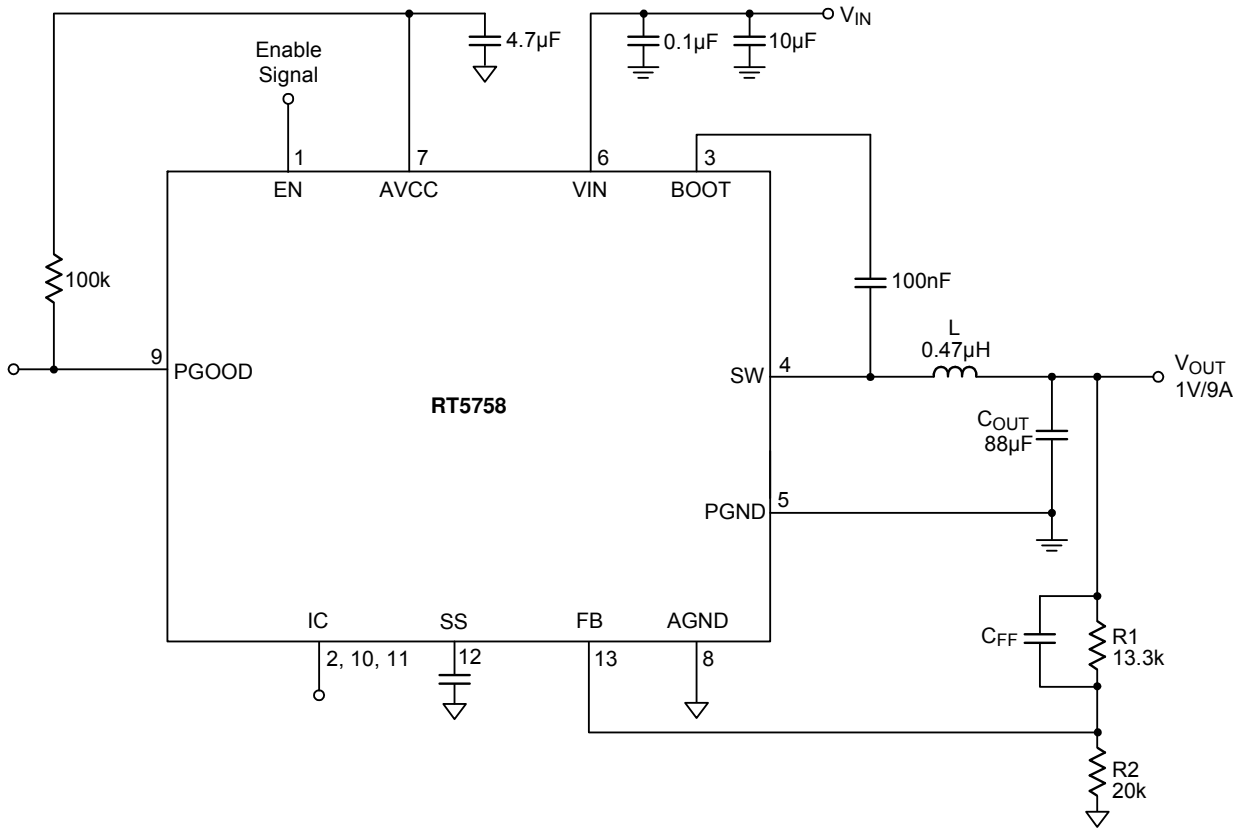
Table 1. Suggested Component Values

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	C_{FF} (pF)	L (μH)	C_{OUT} (μF)
1	13.3	20	--	0.47	88
1.2	20	20	--	0.47	88
1.5	30	20	--	0.47	88
2.5	63.4	20	22	0.47	88
3.3	90	20	22	0.47	88

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Functional Pin Description

Pin No.	Pin Name	Pin Function
1	EN	Enable control input. A logic-high enables the converter; a logic-low forces the IC into shutdown mode and reduces the supply current.
2, 10, 11	IC	Internal connected for testing. Leave these pins floating in normal operation.
3	BOOT	Bootstrap, supply for high-side gate driver. Connect a 0.1μF ceramic capacitor between BOOT and SW pins.
4	SW	Switch node. Connect this pin to an external L-C filter.
5	PGND	System GND. The power GND of the controller circuit. Use wide PCB traces to make the connections.
6	VIN	Input voltage. Support 3V to 6.5V input voltage. Connect this pin with a suitable capacitance for noise decoupling. The bypass capacitor should be placed as close to VIN pin as possible.
7	AVCC	LDO output for internal analog power. Connect a 4.7μF capacitor as close to the VCC pin as possible.
8	AGND	Analog GND. AGND and PGND are connected with a short trace and at only one point to reduce circulating currents.
9	PGOOD	Power good indicator output. This pin has an open drain structure. Pull this pin high to a voltage source with a 100kΩ resistor.
12	SS	Soft-start time control pin. Connect a capacitor between the SS pin and AGND to set the soft-start time. The default internal start-up time is 1.045ms without external capacitor.
13	FB	Feedback input. The pin is used to set the output voltage of the converter via a resistor divider. Suggest placing the FB resistor divider as close to FB pin and AGND as possible.

Functional Block Diagram
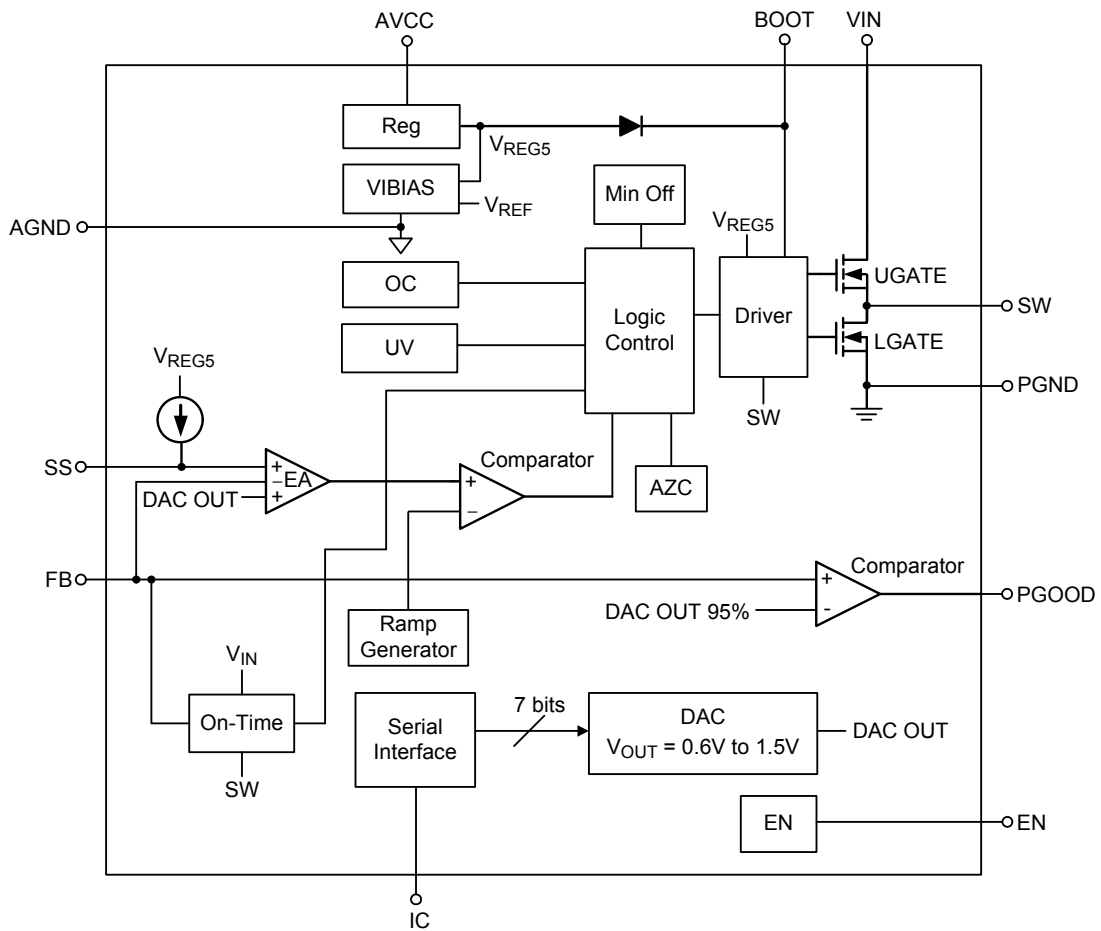
Operation

The RT5758 is a low voltage synchronous step-down converter that can support input voltage ranging from 3V to 6.5V and the output current can be up to 9A. The RT5758 uses ACOT^{TM} mode control. To achieve good stability with low-ESR ceramic capacitors, the ACOT uses a virtual inductor current ramp generated inside the IC.

This internal ramp signal replaces the ESR ramp normally provided by the output capacitor's ESR. The ramp signal and other internal compensations are optimized for low-ESR ceramic output capacitors. In steady-state operation, the feedback voltage, with the virtual inductor current ramp added, is compared to the reference voltage. When the combined signal is less than the reference, the on-time one-shot is triggered, as long as the minimum off-time one-shot is clear and the measured inductor current (through the synchronous rectifier) is below the current limit. The on-time one-shot turns on the high-side switch and the inductor current ramps up linearly. After the on-time, the high-side switch is turned off and the synchronous rectifier is turned on and the inductor current ramps down linearly. At the same time, the minimum off-time one-shot is triggered to prevent another immediate on-time during the noisy switching time and allow the feedback voltage and current sense signals to settle. The minimum off-time is kept short so that rapidly-repeated on-times can raise the inductor current quickly when needed.

Shutdown, Start-Up and Enable (EN)

The enable input (EN) has a logic-low level of 0.74V. When V$_{EN}$ is below this level the IC enters shutdown mode and supply current drops to less than 1μA. When V$_{EN}$ exceeds its logic-high level of 0.92V the IC is fully operational. When V$_{EN}$ exceeds its logic-high level, the pre-regulator turns on first.

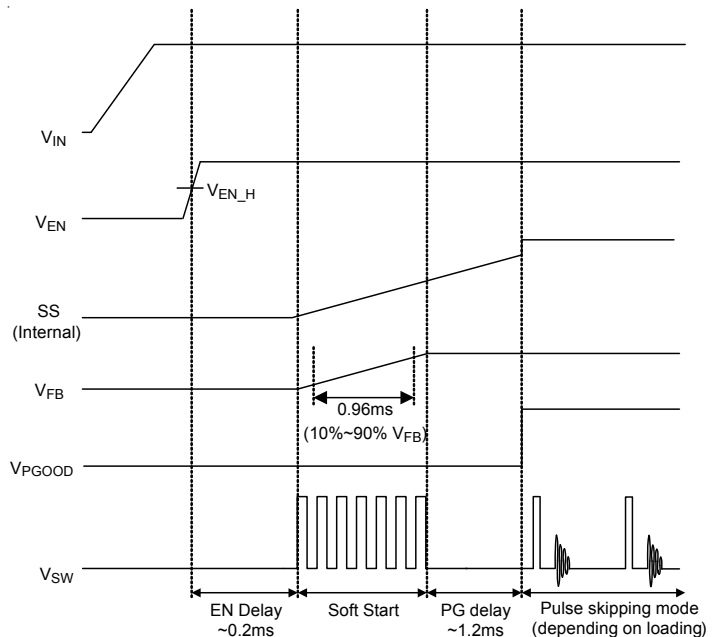The power up sequence from EN logic high to PGOOD go high is shown as Figure 1.

Figure 1. Power Up Sequence which is Following Internal Soft-Start

Under-Voltage Protection (UVLO)

The UVLO continuously monitors the AVCC voltage to make sure the device works properly. When the AVCC is high enough to reach the UVLO high threshold voltage, the step-down converter softly starts or pre-bias to its regulated output voltage. When the AVCC decreases to its low threshold voltage, the device shuts down.

Power Good

Power Good pin is an open-drain logic output that is pulled to ground when the output voltage is lower or higher than its specified threshold under the conditions of OVP, OTP, dropout, EN shutdown, or during start up time. Start up time is the time of V$_{OUT}$ soft-start when power up or enable up. During the start up time, the PGOOD is low even the output voltage is within the specified threshold voltage. Only the PGOOD indicator is high and output voltage is within the specified threshold voltage, then PGOOD is high.

External Bootstrap Capacitor (C$_{BOOT}$)

Connect a 0.1µF low ESR ceramic capacitor between BOOT and SW. This bootstrap capacitor provides the gate driver supply voltage for the high-side N-MOSFET switch.

Output Under-Voltage Protection (UVP)

When the output voltage is lower than 70% reference voltage after soft-start, the UVP is triggered.

Over-Temperature Protection (OTP)

The RT5758 includes an Over-Temperature Protection (OTP) circuitry to prevent overheating due to excessive power dissipation. The OTP will shut down switching operation when the junction temperature exceeds 150°C. Once the junction temperature cools down and returns to 100°C the IC will resume normal operation with a complete soft-start. For continuous operation, provide adequate cooling so that the junction temperature does not exceed 150°C.

Absolute Maximum Ratings　(Note 1)

- Supply Input Voltage, VIN -- −0.3V to 7V
- Switch Node Voltage, SW --- −0.3V to 7V
- Other Pins Voltage --- −0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C
  UQFN-13L 3x3 (FC) --- 2.62W
- Package Thermal Resistance　(Note 2)
  UQFN-13L 3x3 (FC), $θ_{JA}$ --- 38.1°C/W
  UQFN-13L 3x3 (FC), $θ_{JC}$ -- 4.1°C/W
- Junction Temperature Range -- 150°C
- Lead Temperature (Soldering, 10 sec.) --- 260°C
- Storage Temperature Range --- −65°C to 150°C
- ESD Susceptibility　(Note 3)
  HBM (Human Body Model) -- 2kV

Recommended Operating Conditions　(Note 4)

- Supply Input Voltage, VIN -- 3V to 6.5V
- Junction Temperature Range -- −40°C to 125°C
- Ambient Temperature Range --- −40°C to 85°C
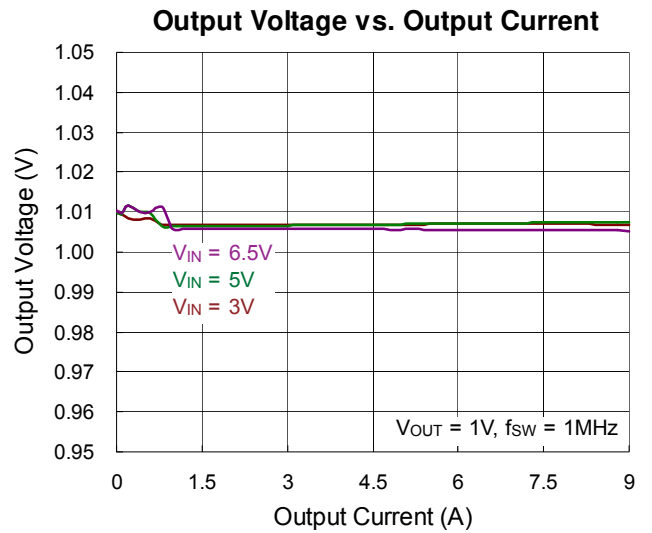
Electrical Characteristics

(V_{IN} = 5V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage						
Input Voltage	V_{IN}		3	--	6.5	V
Supply Current						
Sleep Supply Current	I_Q	V_{FB} > 0.6V	--	--	100	µA
Shutdown Supply Current	I_{SHDN}	V_{EN} = 0V	--	--	1	µA
UVLO						
UVLO Rising Threshold	V_{UVLO_R}	V_{AVCC} rising	--	2.625	2.8	V
UVLO Falling Threshold	V_{UVLO_F}	V_{AVCC} falling	--	2.5	--	V
Logic Threshold						
EN Input Rising Threshold	V_{ENH}		0.77	0.92	1.07	V
EN Input Falling Threshold	V_{ENL}		0.58	0.74	0.9	V
EN Hysteresis	$ΔV_{EN}$		--	0.18	--	V
Input Current	I_{EN}	V_{EN} = 2V	--	1	5	µA

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Thermal Shutdown							
Thermal Shutdown Threshold		T_{SD}		--	150	--	°C
Thermal Recovery Threshold		T_{RC}		--	100	--	°C
Reference and Soft-Start							
Reference Voltage		V_{REF}	CCM	0.591	0.6	0.609	V
Soft-Start Time		t_{SS}	Leave SS pin floating, 10% to 90%V_{OUT}	--	0.96	--	ms
$R_{DS(ON)}$							
Switch On-Resistance	High-Side	$R_{DS(ON)\_H}$		--	12	--	mΩ
	Low-Side	$R_{DS(ON)\_L}$		--	8	--	
Current Limit							
Current Limit		I_{LIM}	Valley current	9.1	10.8	12.5	A
Switching Frequency and Minimum Off-Time							
Switching Frequency		f_{SW}	CCM	0.8	1	1.2	MHz
Minimum Off-Time		t_{OFF_MIN}		--	100	--	ns
Protections							
UVP Trip Threshold		V_{UVP}		--	70	--	%
UVP Time Delay		t_{UVPDLY}		--	5	--	μs
Power Good							
PGOOD Rising Threshold		V_{TH_PGLH}	V_{FB} rising (Good)	--	95	--	%V_{FB}
		ΔV_{TH_PGLH}	V_{FB} rising (Fault)	--	110	--	
PG Falling Threshold		V_{TH_PGHL}	V_{FB} falling (Fault)	--	90	--	
		ΔV_{TH_PGHL}	V_{FB} falling (Good)	--	105	--	
PGOOD Enable Delay Time				--	10	--	μs
Discharge Resistor							
Discharge Resistor		R_{DISCHG}	V_{EN} = 0V, V_{AVCC} = 5V	--	50	--	Ω
Regulation							
Line Regulation			CCM	--	0.5	--	%
Load Regulation (Note 5)			CCM	--	0.5	--	%

Note 1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured under natural convection (still air) at $T_A = 25°C$ with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Note 5. Guaranteed by design.
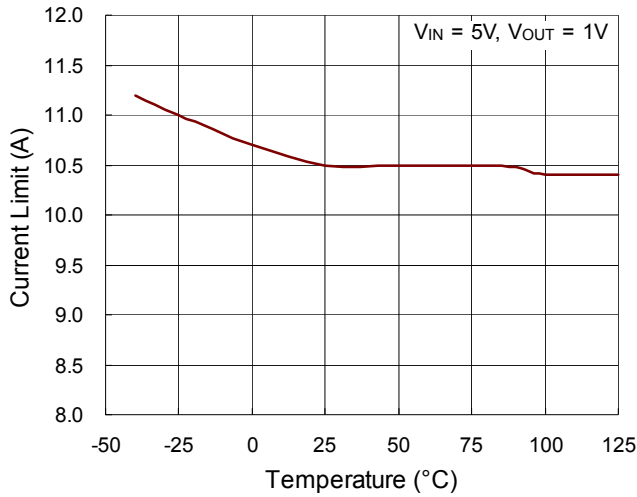
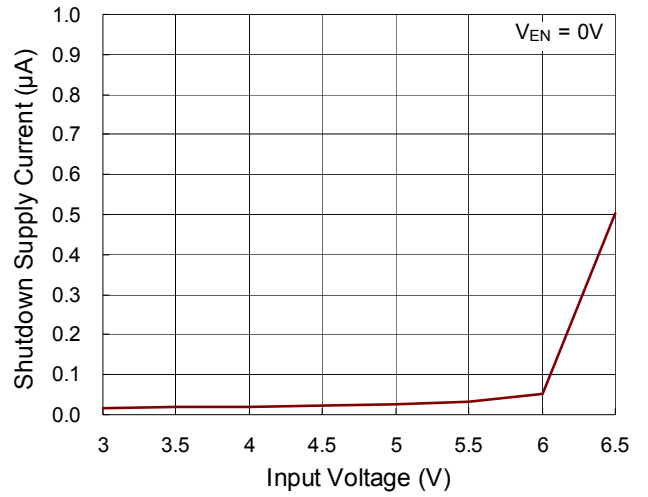## Typical Operating Characteristics

Efficiency vs. Output Current

V_{IN} = 3V, f_{SW} = 1MHz

V_{OUT} = 1.5V
V_{OUT} = 1.2V
V_{OUT} = 1V
V_{OUT} = 0.8V
V_{OUT} = 0.6V

Efficiency vs. Output Current

V_{IN} = 5V, f_{SW} = 1MHz

V_{OUT} = 3.3V
V_{OUT} = 2.5V
V_{OUT} = 1.5V
V_{OUT} = 1.2V
V_{OUT} = 1V
V_{OUT} = 0.8V
V_{OUT} = 0.6V

Efficiency vs. Output Current

V_{IN} = 6.5V, f_{SW} = 1MHz

V_{OUT} = 3.3V V_{OUT} = 0.8V
V_{OUT} = 2.5V V_{OUT} = 0.6V
V_{OUT} = 1.5V
V_{OUT} = 1.2V
V_{OUT} = 1V

Output Voltage vs. Output Current

V_{IN} = 6.5V
V_{IN} = 5V
V_{IN} = 3V

V_{OUT} = 1V, f_{SW} = 1MHz

Output Voltage vs. Input Voltage

I_{OUT} = 0A
I_{OUT} = 3A
I_{OUT} = 6A
I_{OUT} = 9A

V_{OUT} = 1V, f_{SW} = 1MHz

Switching Frequency vs. Input Voltage

V_{OUT} = 1V

Switching Frequency vs. Temperature

V_IN = 5V, V_OUT = 1V
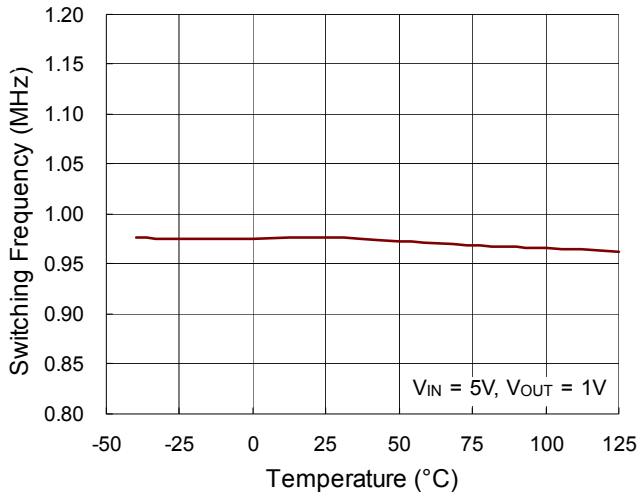
Current Limit vs. Input Voltage

V_OUT = 1V
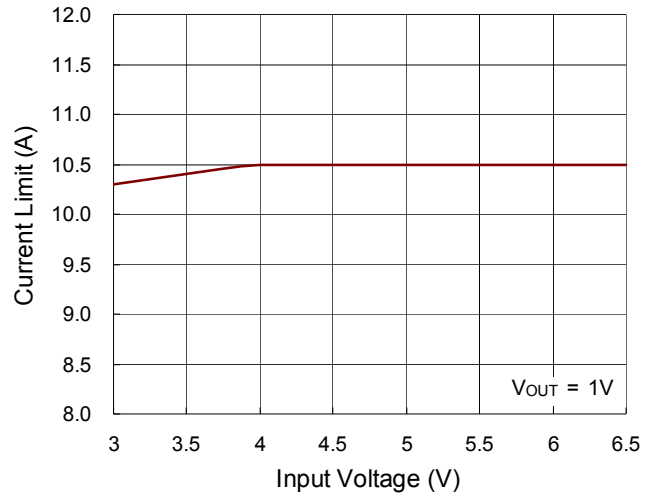
Current Limit vs. Temperature

V_IN = 5V, V_OUT = 1V

Shutdown Supply Current vs. Input Voltage

V_EN = 0V

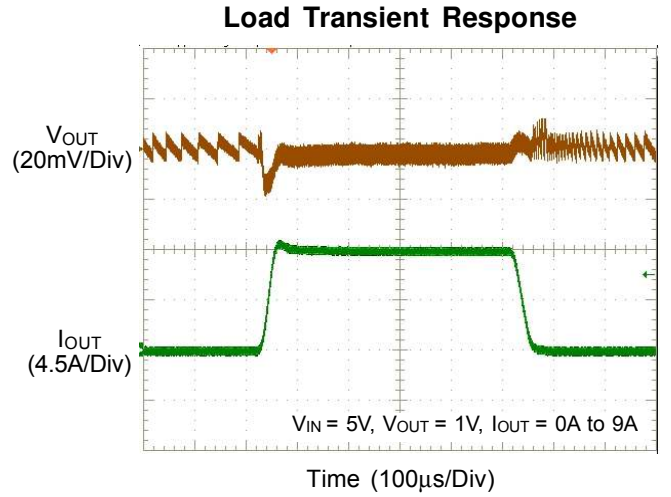**Shutdown Supply Current vs. Temperature**

V_IN = 5V, V_EN = 0V

Sleep Supply Current vs. Input Voltage

V_EN = high

Sleep Supply Current vs. Temperature

V_{IN} = 5V, V_{EN} = high

Reference Voltage vs. Input Voltage

Reference Voltage vs. Temperature

V_{IN} = 5V

Load Transient Response

V_{OUT}
(20mV/Div)

I_{OUT}
(4.5A/Div)

V_{IN} = 5V, V_{OUT} = 1V, I_{OUT} = 0A to 9A

Time (100μs/Div)

Load Transient Response

V_{OUT}
(10mV/Div)

I_{OUT}
(4.5A/Div)

V_{IN} = 5V, V_{OUT} = 1V, I_{OUT} = 4.5A to 9A

Time (100μs/Div)

Output Ripple Voltage

V_{SW}
(2V/Div)

V_{OUT}
(10mV/Div)

V_{IN} = 5V, V_{OUT} = 1V, I_{OUT} = 0A

Time (20ms/Div)

Output Ripple Voltage

V_SW (2V/Div)

V_OUT (10mV/Div)

V_IN = 5V, V_OUT = 1V, I_OUT = 9A

Time (400ns/Div)

Power On from EN

V_EN (2V/Div)

V_OUT (1V/Div)

V_SW (5V/Div)

I_L (10A/Div)

V_IN = 5V, V_OUT = 1V, I_OUT = 9A

Time (4ms/Div)

Power Off from EN

V_EN (2V/Div)

V_OUT (1V/Div)

V_SW (5V/Div)

I_L (10A/Div)

V_IN = 5V, V_OUT = 1V, I_OUT = 9A

Time (4ms/Div)

UVP Short (Hiccup Mode)

V_IN (5V/Div)

V_OUT (1V/Div)

V_SW (5V/Div)

I_L (10A/Div)

V_IN = 5V, V_OUT = 1V, I_OUT = short

Time (10ms/Div)

Application Information

Inductor Selection

When designing the output stage of the synchronous buck converter, it is recommended to start with the inductor. However, it may require several iterations because the exact inductor value is generally flexible and is optimized for low cost, small form factor, and high overall performance of the converter. Further, inductors vary with manufacturers in both material and value, and typically have a tolerance of ±20%.

Three key inductor parameters to be specified for operation with the device are inductance (L), inductor saturation current (I_{SAT}), and DC resistance (DCR), which affects performance of the output stage. An inductor with lower DCR is recommended for applications of higher peak current or load current, and it can improve system performance. Lower inductor values are beneficial to the system in physical size, cost, DCR, and transient response, but they will cause higher inductor peak current and output voltage ripple to decrease system efficiency. Conversely, higher inductor values can increase system efficiency at the expense of larger physical size, slower transient response due to the longer response time of the inductor. A good compromise among size, efficiency, and transient response can be achieved by setting an inductor current ripple (ΔI_L) of about 20% to 50% of the desired full output load current. To meet the inductor current ripple (ΔI_L) requirements, a minimum inductance must be chosen and the approximate inductance can be calculated by the selected input voltage, output voltage, switching frequency (f_{SW}), and inductor current ripple (ΔI_L), as below :

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times \Delta I_L}$$

Once the inductance is chosen, the inductor ripple current (ΔI_L) and peak inductor current (I_{L_PEAK}) can be calculated, as below :

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L}$$

$$I_{L\_PEAK} = I_{OUT\_MAX} + \frac{1}{2} \Delta I_L$$

$$I_{L\_VALLEY} = I_{OUT\_MAX} - \frac{1}{2} \Delta I_L$$

where I_{OUT_MAX} is the maximum rated output current or the required peak current.

The inductor must be selected to have a saturation current and thermal rating which exceed the required peak inductor current I_{L_PEAK}. For a robust design to maintain control of inductor current in overload or short-circuit conditions, some applications may desire inductor saturation current rating up to the switch current limits of the device. However, the built-in output under-voltage protection (UVP) feature makes this unnecessary for most applications.

For best efficiency, a low-loss inductor having the lowest possible DCR that still fits in the allotted dimensions will be chosen. Ferrite cores are often the best choice. However, a shielded inductor, possibly larger or more expensive, will probably give fewer EMI and other noise problems.

The following design example is illustrated to walk through the steps to apply the equations defined above. The RT5758's Typical Application Circuit for output voltage of 1V at maximum output current of 9A and an input voltage of 5V with inductor current ripple of 1.8A (i.e. 20%, in the recommended range of 20% to 50%, of the maximum rated output current) is taken as the design example. The approximate minimum inductor value can first be calculated as below :

$$L = \frac{1 \times (5 - 1)}{5 \times 1MHz \times 1.8A} = 0.44\mu H$$

where f_{SW} is 1MHz. The inductor current ripple will be set at 1.8A, as long as the calculated inductance of 0.44μH is used. However, the inductor of the exact inductance value may not be readily available, and therefore an inductor of a nearby value will be chosen. In this case, 0.47μH inductance is available and actually used in the Typical Application Circuit. The actual inductor current ripple (ΔI_L) and required peak inductor current (I_{L_PEAK}) can be calculated as below :

$$\Delta I_L = \frac{1 \times (5 - 1)}{5 \times 1MHz \times 0.47\mu H} = 1.702A$$

$$I_{L\_PEAK} = I_{OUT\_MAX} + \frac{1}{2} \Delta I_L = 9 + \frac{1.702}{2} = 9.851A$$

For the 0.47µH inductance value, the inductor saturation current and thermal rating should exceed 9.851A.

Input Capacitor Selection

Input capacitors are needed to smooth out the RMS ripple current (I_{RMS}) imposed by the switching currents and drawn from the input power source, by reducing the ripple voltage amplitude seen at the input of the converters. The voltage rating of the input filter capacitors must be greater than the maximum input voltage. It's also important to consider the ripple current capabilities of capacitors.

The RMS ripple current (I_{RMS}) of the regulator can be determined by the input voltage (V_{IN}), output voltage (V_{OUT}), and rated output current (I_{OUT}) as the following equation :

$$I_{RMS} = I_{OUT} \times \frac{V_{OUT}}{V_{IN}} \times \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

From the above, the maximum RMS input ripple current occurs at maximum output load, which will be used as the requirements to consider the current capabilities of the input capacitors. Furthermore, for a single phase buck converter, the duty cycle is approximately the ratio of output voltage to input voltage. The maximum ripple voltage usually occurs at 50% duty cycle, that is, V_{IN} = 2 x V_{OUT}. The maximum I_{RMS}, as I_{RMS} (Max), can be approximated as 0.5 x I_{OUT_MAX}, where I_{OUT_MAX} is the maximum rated output current. Besides, the variation of the capacitance value with temperature, DC bias voltage, switching frequency, and allowable peal-to-peak ripple voltage that reflects back to the input, also need to be taken into consideration. For example, the capacitance value of a capacitor decreases as the DC bias across the capacitor increases; also, higher switching frequency allows the use of input capacitors of smaller capacitance values.

Ceramic capacitors are most commonly used to be placed right at the input of the converter to reduce ripple voltage amplitude because only ceramic capacitors have extremely low ESR which is required to reduce the ripple voltage. Note that the capacitors need to be placed as close as to the input pins as possible for highest effectiveness. Ceramic capacitors are preferred also due to their low cost, small size, high RMS current ratings, robust inrush surge current capabilities, and low parasitic

inductance, which helps reduce the high-frequency ringing on the input supply.

However, care must be taken when ceramic capacitors are used at the input, and the input power is supplied by a wall adapter, connected through a long and thin wire. When a load step occurs at the output, a sudden inrush current will surge through the long inductive wire, which can induce ringing at the device's power input and potentially cause a very large voltage spike at the VIN pin to damage the device. For applications where the input power is located far from the device input, it may be required that the low-ESR ceramic input capacitors be placed in parallel with a bulk capacitor of other types, such as tantalum, electrolytic, or polymer, to dampen the voltage ringing and overshoot at the input, caused by the long input power path and input ceramic capacitor.

It is suggested to choose capacitors with higher temperature ratings than required. Several ceramic capacitors may be parallel to meet application requirements, such as the RMS current, size, and height. The Typical Application Circuit can use one 10µF and one high-frequency- noise-filtering 0.1µF low-ESR ceramic capacitors at the input.

Output Capacitor Selection

Output capacitance affects the output voltage of the converter, the response time of the output feedback loop, and the requirements for output voltage sag and soar. The sag occurs after a sudden load step current applied, and the soar occurs after a sudden load removal. Increasing the output capacitance reduces the output voltage ripple and output sag and soar, while it increases the response time that the output voltage feedback loop takes to respond to step loads, Therefore, there is a tradeoff between output capacitance and output response. It is recommended to choose a minimum output capacitance to meet the output voltage requirements of the converter, and have a quick transient response to step loads.

The ESR of the output capacitor affects the damping of the output filter and the transient response. In general, low-ESR capacitors are good choices due to their excellent capability in energy storage and transient performance. The RT5758, therefore, is specially optimized

RT5758

for ceramic capacitors. Consider also DC bias and aging effects while selecting the output capacitor.

Output Voltage Ripple

The output voltage ripple at the switching frequency is a function of the inductor current ripple going through the output capacitor's impedance. To derive the output voltage ripple, the output capacitor with capacitance, C_{OUT}, and its equivalent series resistance, R_{ESR}, must be taken into consideration. The output peak-to-peak ripple voltage ΔV_{P-P}, caused by the inductor current ripple ΔI_L, is characterized by two components, which are ESR ripple ΔV_{P-P_ESR} and capacitive ripple ΔV_{P-P_C}, can be expressed as below :

$$\Delta V_{P-P} = \Delta V_{P-P\_ESR} + \Delta V_{P-P\_C}$$

$$\Delta V_{P-P\_ESR} = \Delta I_L \times R_{ESR}$$

$$\Delta V_{P-P\_C} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}}$$

If ceramic capacitors are used as the output capacitors, both the components need to be considered due to the extremely low ESR and relatively small capacitance.

For the RT5758's Typical Application Circuit for output voltage of 1V, and actual inductor current ripple (ΔI_L) of 1.702A, using four paralleled 22µF ceramic capacitors with ESR of about 5mΩ as output capacitors, the two output ripple components are as below :

$$\Delta V_{P-P\_ESR} = \Delta I_L \times R_{ESR} = 1.702A \times 5m\Omega = 8.51mV$$

$$\Delta V_{P-P\_C} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}} = \frac{1.702A}{8 \times 88\mu F \times 1MHz}$$
$$= 2.42mV$$

$$\Delta V_{P-P} = \Delta V_{P-P\_ESR} + \Delta V_{P-P\_C} = 10.93mV$$

Output Transient Undershoot and Overshoot

In addition to the output voltage ripple at the switching frequency, the output capacitor and its ESR also affect output voltage sag, which is undershoot on a positive load step, and output voltage soar, which is overshoot on a negative load step. With the built-in ACOT^{TM} architecture, the IC can have very fast transient responses to the load steps and small output transients.

However, the combination of a small ceramic output capacitor (that is, of little capacitance) and a low output voltage (that is, only little charge stored in the output

capacitor), used in low-duty-cycle applications (which require high inductance to get reasonable ripple currents for high input voltages), causes an increase in the size of voltage variations (i.e. sag/soar) in response to very quick load changes. Typically, the load changes slowly, compared with the IC's switching frequency. However, for present-day applications, more and more digital blocks may exhibit nearly instantaneous large transient load changes. Therefore, in the following section, how to calculate the worst-case voltage swings in response to very fast load steps will be explained in details.

Both of the output transient undershoot and overshoot have two components : a voltage step caused by the output capacitor's ESR, and a voltage sag or soar due to the finite output capacitance and the inductor current slew rate. The following formulas can be used to check if the ESR is low enough (which is usually not a problem with ceramic capacitors) and if the output capacitance is large enough to prevent excessive sag or soar on very fast load steps, with the chosen inductor value.

The voltage step (ΔV_{OUT_ESR}) caused by the ESR is a function of the load step (ΔI_{OUT}) and the ESR (R_{ESR}) of the output capacitor, described as below :

$$\Delta V_{OUT\_ESR} = \Delta I_{OUT} \times R_{ESR}$$

The voltage amplitude (ΔV_{OUT_SAG}) of the capacitive sag is a function of the load step (ΔI_{OUT}), the output capacitor value (C_{OUT}), the inductor value (L), the input-to-output voltage differential, and the maximum duty cycle (D_{MAX}). And, the maximum duty cycle during a fast transient can be determined by the on-time (t_{ON}) and the minimum off-time (t_{OFF_MIN}) since the ACOT^{TM} control scheme will ramp the current during on-times, which are spaced apart by a minimum off-time, that is, as fast as allowed. The approximate on-time (neglecting parasitics) and maximum duty cycle for a given input and output voltage can be calculated according to the following equations :

$$t_{ON} = \frac{V_{OUT}}{V_{IN} \times f_{SW}} \text{ and } D_{MAX} = \frac{t_{ON}}{t_{ON} + t_{OFF\_MIN}}$$

Note the actual on-time will be slightly larger than the calculated one as the IC will automatically adapt to compensate the internal voltage drops, such as the voltage across high-side switch due to on-resistance. However, both of these can be neglected since the on-time increase

can compensate for the voltage drops. The output voltage sag (ΔV_{OUT_SAG}) can then be calculated as below :

$$\Delta V_{OUT\_SAG} = \frac{L \times (\Delta I_{OUT})^2}{2 \times C_{OUT} \times (V_{IN} \times D_{MAX} - V_{OUT})}$$

The voltage amplitude of the capacitive soar is a function of the load step (ΔI_{OUT}), the output capacitor value (C_{OUT}), the inductor value (L), and the output voltage (V_{OUT}). And the output voltage soar (ΔV_{OUT_SOAR}) can be calculated as below :

$$\Delta V_{OUT\_SOAR} = \frac{L \times (\Delta I_{OUT})^2}{2 \times C_{OUT} \times V_{OUT}}$$

Feedforward Capacitor (C_{FF})

The RT5758 is optimized for ceramic output capacitors and for low duty-cycle applications. This optimization makes circuit stability easy to achieve with reasonable output capacitors, but it also narrows the optimization of transient responses of the converter. For high output voltage (that is, high duty-cycle) applications, the FB voltage is highly attenuated from the output, the circuit's response becomes under-damped and transient response is slowed. A small feedforward capacitor (C_{FF}) can be introduced into the feedback network to speed up the transient response of high output voltage circuits. The feedforward capacitor is added across the upper FB divider resistor (as seen in Figure 2) to speed up the transient response without affecting the steady-state stability of the circuit.

To optimize transient response, a C_{FF} value is chosen so that the gain and phase boost of the feedback network increases the bandwidth of the converter, while still maintaining an acceptable phase margin. Generally, larger C_{FF} values provide higher bandwidth, but may result in an unacceptable phase margin or instability. Suitable feedforward capacitor values can be chosen from the table of Suggested Component Values.
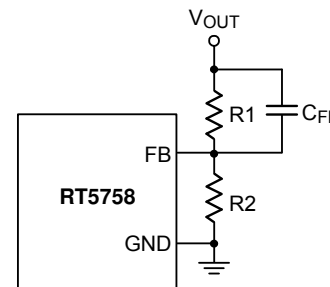

Figure 2. C_{FF} Capacitor Setting

EN Pin for Start-Up and Shutdown Operation

For automatic start-up, the EN pin, with normal voltage rating, can be connected to the input supply V_{IN}, through a 100kΩ resistor. The large built-in hysteresis band makes the EN pin useful for simple delay and timing circuits. The EN pin can be externally connected to V_{IN} by adding a resistor R_{EN} and a capacitor C_{EN}, as shown in Figure 3, to have an additional delay. The time delay can be calculated with the EN's internal threshold, at which switching operation begins.

An external MOSFET can be added for the EN pin to be logic-controlled, as shown in Figure 4. In this case, a 100kΩ pull-up resistor, R_{EN}, is connected between V_{IN} and the EN pin. The MOSFET Q1 will be under logic control to pull down the EN pin. To prevent the device being enabled when V_{IN} is smaller than the V_{OUT} target level or some other desired voltage level, a resistive divider (R_{EN1} and R_{EN2}) can be used to externally set the input under-voltage lockout threshold, as shown in Figure 5.
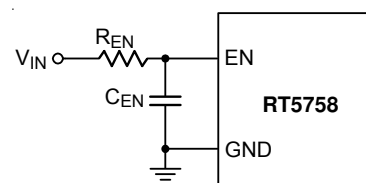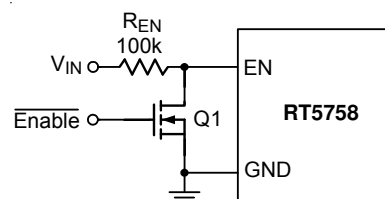

Figure 3. Enable Timing Control
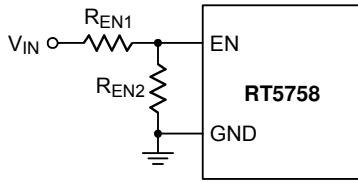

Figure 4. Logic Control for the EN Pin

RT5758

Figure 5. Resistive Divider for Under-Voltage Lockout Threshold Setting

Output Voltage Setting

The output voltage can be programmed by a resistive divider from the output to ground with the midpoint connected to the FB pin. The resistive divider allows the FB pin to sense a fraction of the output voltage as shown in Figure 6. The output voltage is set according to the following equation :

$$V_{OUT} = V_{REF} \times (1 + \frac{R1}{R2})$$

where the reference voltage V_{REF}, is around 0.6V (Typical).
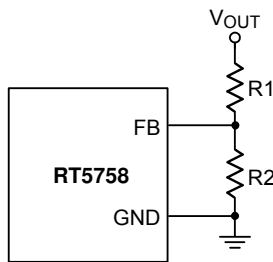
Figure 6. Output Voltage Setting

The placement of the resistive divider should be within 5mm of the FB pin. The resistance of R2 is suggested between 10kΩ and 100kΩ to minimize power consumption, and noise pick-up at the FB pin. The resistance of R1 can then be obtained as below :

$$R1 = \frac{R2 \times (V_{OUT} - V_{REF})}{V_{REF}}$$

For better output voltage accuracy, the divider resistors (R1 and R2) with ±1% tolerance or better should be used.

External Bootstrap Diode

A bootstrap capacitor of 0.1μF low-ESR ceramic capacitor is connected between the BOOT and SW pins to supply the high-side gate driver. It is recommended to add an external bootstrap diode between an external 5V voltage supply and the BOOT pin to improve enhancement of the internal MOSFET switch and improve efficiency when the input voltage is below 5.5V. The bootstrap diode can be a low-cost one, such as 1N4148 or BAT54.
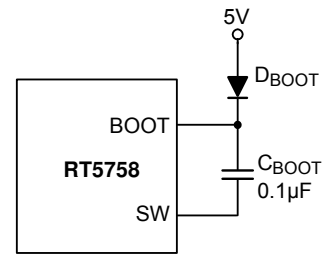

Figure 7. External Bootstrap Diode

Resistor at BOOT Pin

The gate driver of an internal power MOSFET, utilized as a high-side switch, is optimized for turning on the switch not only fast enough for reducing switching power loss, but also slow enough for minimizing EMI. The EMI issue is worse when the switch is turned on rapidly due to high di/dt noises induced. When the high-side switch is being turned off, the SW node will be discharged relatively slowly by the inductor current due to the presence of the dead time when both the high-side and low-side switches are turned off.

In some cases, it is desirable to reduce EMI further, even at the expense of some additional power dissipation. The turn-on rate of the high-side switch can be slowed by placing a small (< 47Ω) resistor between the BOOT pin and the external bootstrap capacitor. This will slow down the rates of the high-side switch turn-on and the rise of V_{SW}. The recommended application circuit is shown in Figure 8, which includes an external bootstrap diode for charging the bootstrap capacitor and a bootstrap resistor R_{BOOT} being placed between the BOOT pin and the capacitor/diode connection.
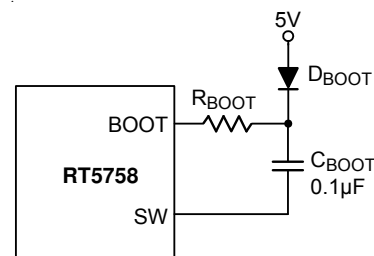

Figure 8. External Bootstrap Diode and Resistor at the BOOT Pin

Soft-Start Function

The RT5758 provides an adjustable soft-start function. The soft-start function is used to prevent large inrush current while the converter is being powered-up. The soft-start time is defined as the output voltage rising time from 10% to 90% of settled level and can be programmed by the external soft-start capacitor C_{SS} between the SS and GND pins. An internal current source I_{SS} (typically, 10μA) charges the capacitor to build a soft-start ramp voltage. The FB voltage will track the ramp voltage of SS pin during soft-start. The typical soft-start time can be calculated as follows :

Soft-Start Time

$$t_{SS} \ (ms) = \frac{C_{SS}(nF) \times V_{REF} \times 0.8}{I_{SS}(\mu A)} = \frac{C_{SS} \ (nF) \times 0.6 \times 0.8}{10(\mu A)}$$

If we leave SS pin unconnected, the soft-start time has its minimum value equal to 0.96ms. We only connect an external soft-start capacitor C_{SS} when we need longer soft-start time.

Power-Good Output

The PGOOD pin is an open-drain power-good indication output and is to be connected to an external voltage source through a pull-up resistor. The power-good function is activated after soft-start is finished and is controlled by the feedback signal V_{FB}. During soft-start, PGOOD is actively held low and only allowed to transition high after soft-start is over. If V_{FB} rises above a power-good threshold (V_{TH_PGLH}) (typically 95% of the target value), the PGOOD pin will be in high impedance and V_{PGOOD} will be held high after a certain delay elapsed. When V_{FB} drops by a power-good hysteresis (ΔV_{TH_PGLH}) (typically 5% of the target value) or exceeds V_{TH_PGHL} (typically 110% of the target value), the PGOOD pin will be pulled low. For V_{FB} above V_{TH_PGHL}, V_{PGOOD} will be pulled high again when V_{FB} drops back by a power-good hysteresis (ΔV_{TH_PGHL}) (typically 5% of the target value). Once being started-up, if any internal protection is triggered, PGOOD will be pulled low to GND.

Output Under-Voltage Protection (Hiccup Mode)

The RT5758 includes output under-voltage protection (UVP) against over-load or short-circuited condition by constantly monitoring the feedback voltage V_{FB}. If V_{FB} drops below the under-voltage protection trip threshold (typically 70% of the internal reference voltage), the UV comparator will go high to turn off both the internal high-side and low-side MOSFET switches.

If the output under-voltage condition continues for a period of time, the RT5758 will enter output under-voltage protection with hiccup mode. During hiccup mode, the device remains shut down. After a period of time, a soft-start sequence for auto-recovery will be initiated. Upon completion of the soft-start sequence, if the fault condition is removed, the converter will resume normal operation; otherwise, such cycle for auto-recovery will be repeated until the fault condition is cleared. Hiccup mode allows the circuit to operate safely with low input current and power dissipation, and then resume normal operation as soon as the over-load or short-circuit condition is removed.

Low-Side Current Limit Protection

The RT5758 features a cycle-by-cycle valley-type current limit protection, measuring the inductor current through the synchronous rectifier (low-side switch). The inductor current level is determined by measuring the low-side switch voltage between the SW pin and GND, which is proportional to the switch current, during the low-side on-time. For greater accuracy, temperature compensation is added to the voltage sensing. Once the current rises above the low-side switch valley current limit (I_{LIM}), the on-time one-shot will be inhibited until the inductor current ramps down to the current limit level (I_{LIM}), that is, another on-time can only be triggered when the inductor current goes below the low-side current limit. This function can prevent the average output current from greatly exceeding the guaranteed low-side current limit value.

If the output load current exceeds the available inductor current (clamped by the above-mentioned low-side current limit), the output capacitor needs to supply the extra current such that the output voltage will begin to drop. If it drops below the output under-voltage protection trip threshold, the IC will stop switching to avoid excessive heat.

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a UQFN-13L 3x3 (FC) package, the thermal resistance, θ_{JA}, is 38.1°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below :

$$P_{D(MAX)} = (125°C - 25°C) / (38.1°C/W) = 2.62W \text{ for a}$$
UQFN-13L 3x3 (FC) package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 9 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.
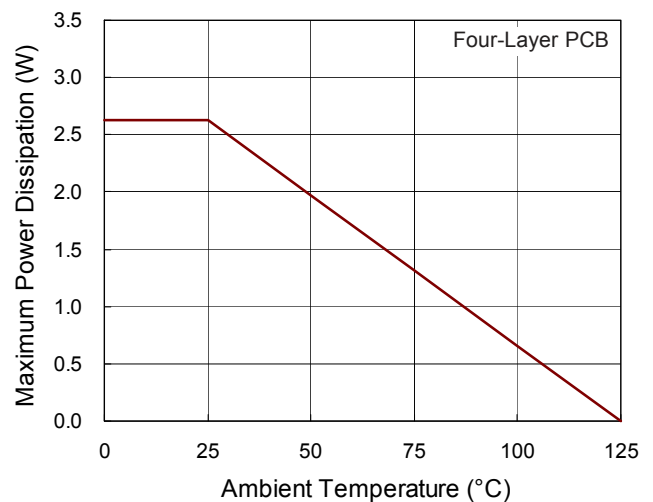

Figure 9. Derating Curve of Maximum Power Dissipation

Layout Consideration

Follow the PCB layout guidelines for optimal performance of the device.

‣ Keep the traces of the input and output current paths as short and wide as possible.

‣ Place input capacitor C_{IN1} and C_{IN2} as close as possible to VIN pins.

‣ Place BOOT capacitor C_{BOOT} as close to the BOOT pin as possible, the 0.1µF to 1µF BOOT capacitor is recommended.

‣ Place vias as many as possible on PGND, and the vias should be closed to the PGND pin to reduce parasitic impendence and minimize the thermal resistance.

‣ SW node is with high frequency voltage swing and should be kept at small area, and keep analog components away from the SW node to prevent stray capacitive noise pickup.

‣ Connect the feedback sense network behind via of output capacitor.

‣ Place the feedback components R1/R2 near the IC.

‣ The decoupling capacitor C_{AVCC} should be placed as close to VCC pin as possible.
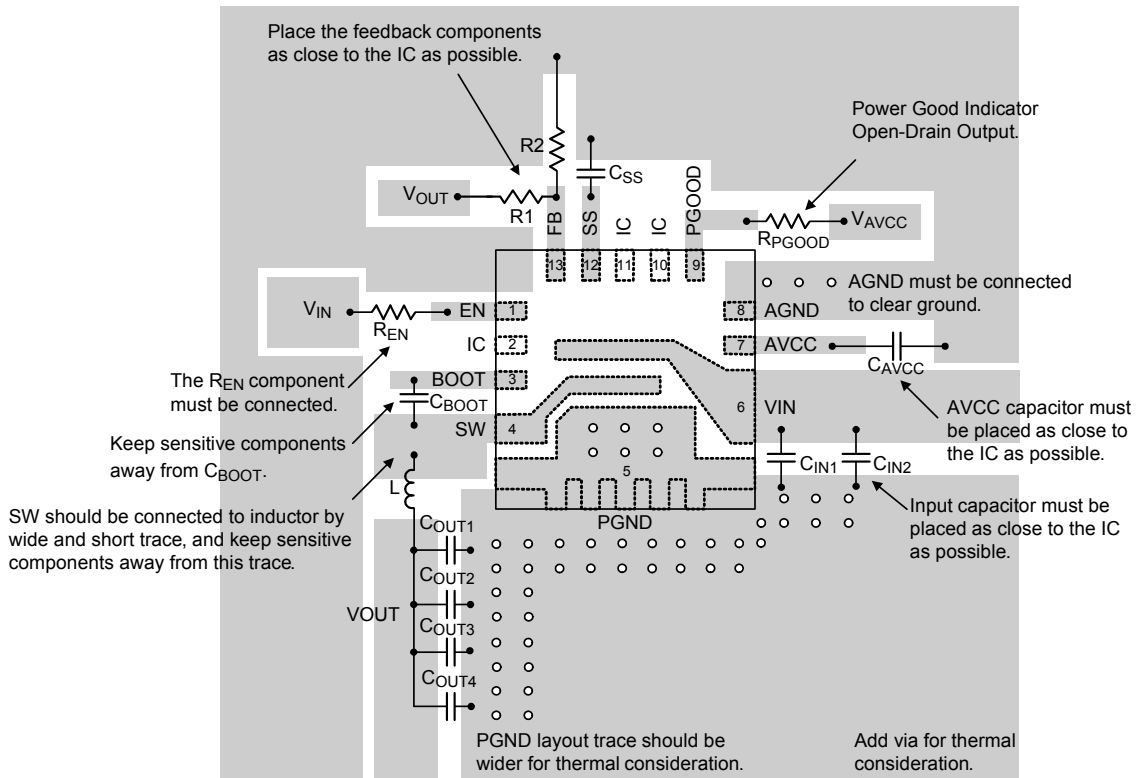
Layout Consideration
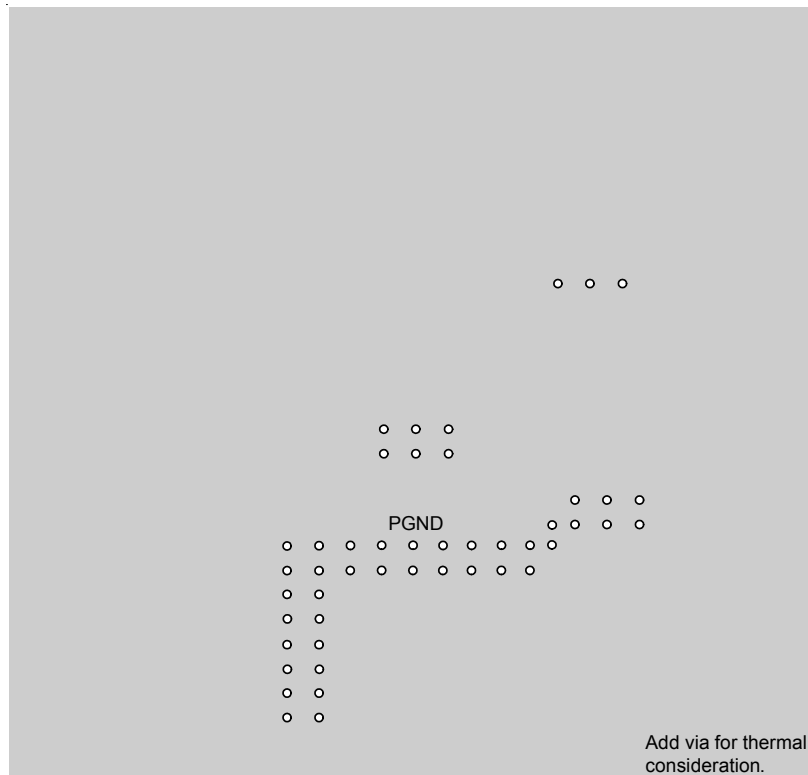

Figure 10. PCB Layout Guide (Top Layer)

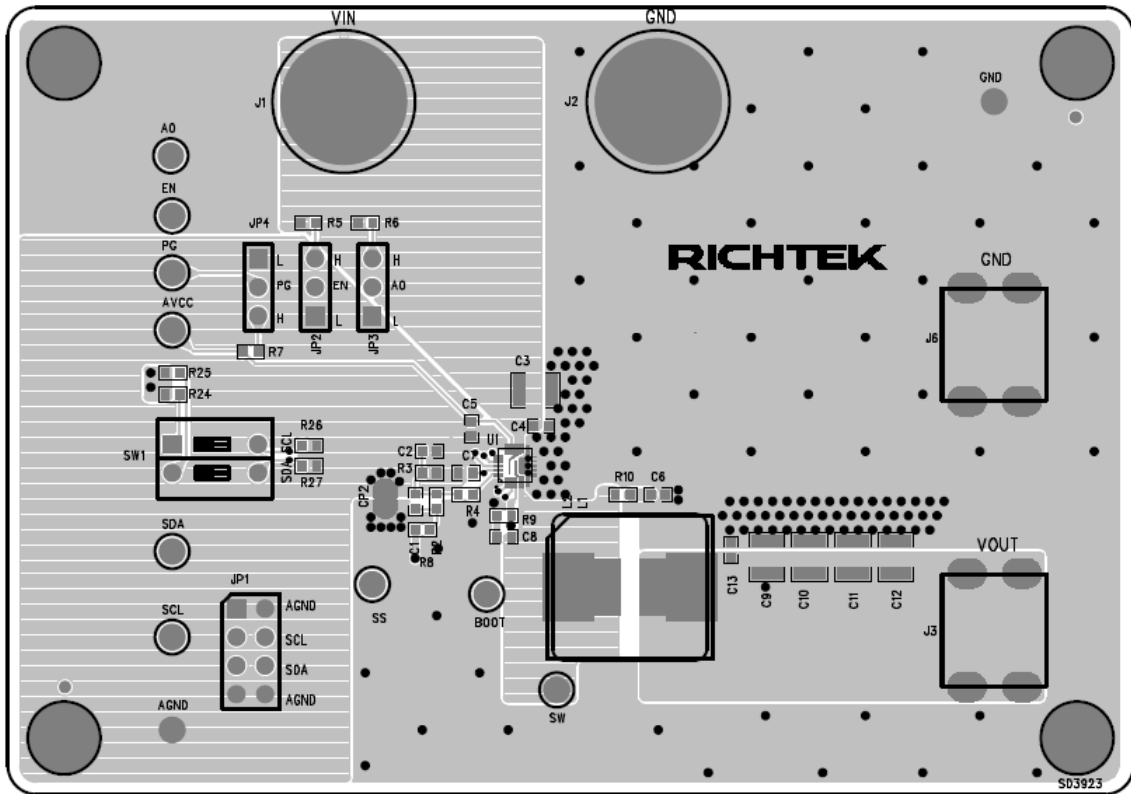Figure 11. PCB Layout Guide (Bottom Layer)
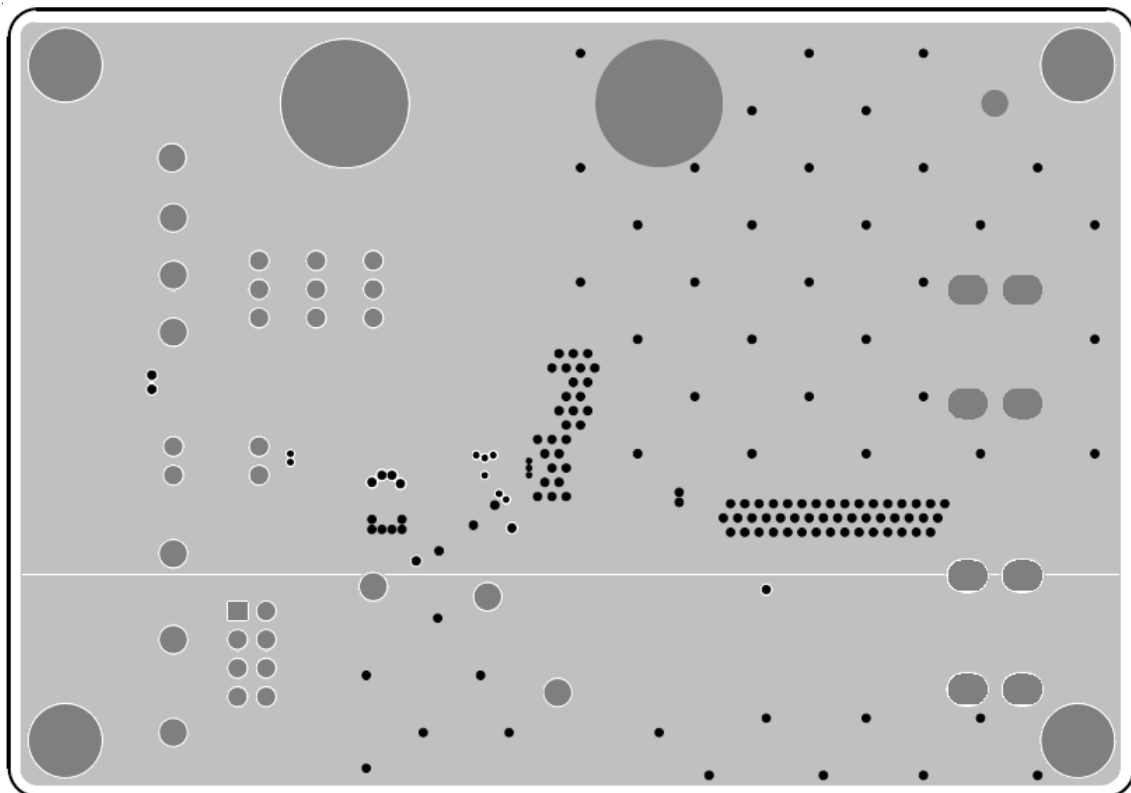
Figure 12. Top Layer PCB Layout
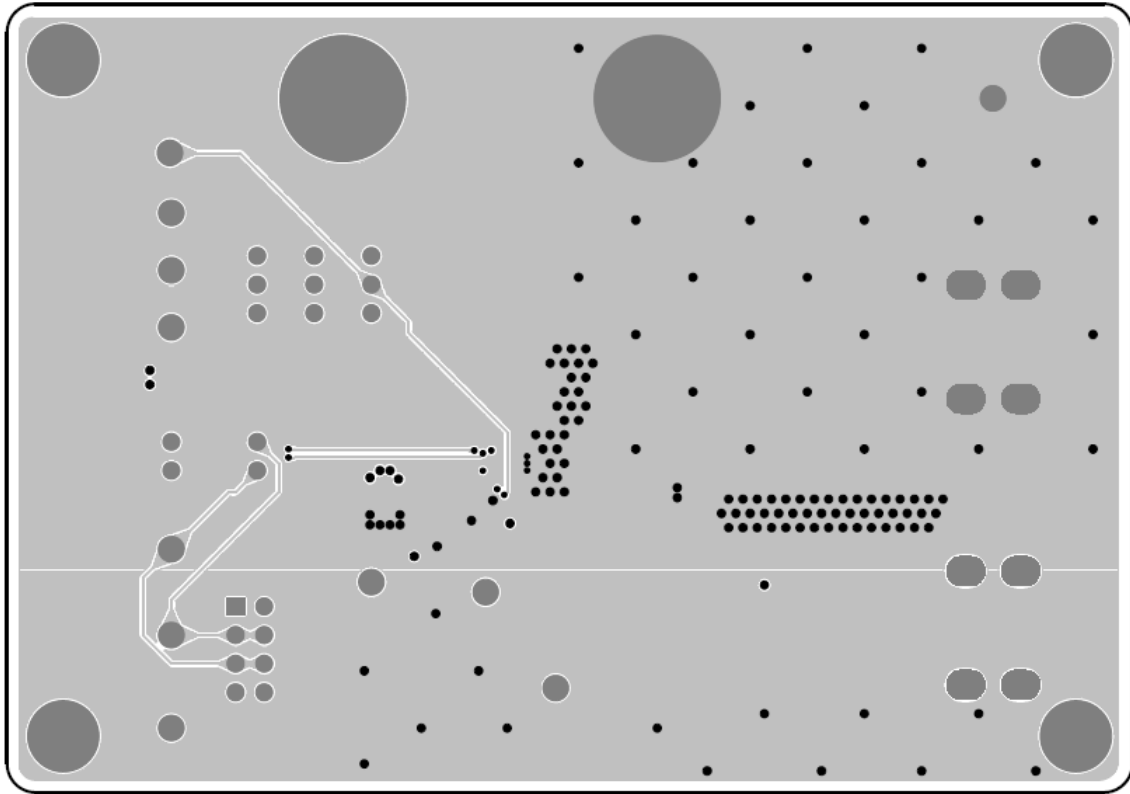

Figure 13. Inner Layer 1 PCB Layout

Figure 14. Inner Layer 2 PCB Layout

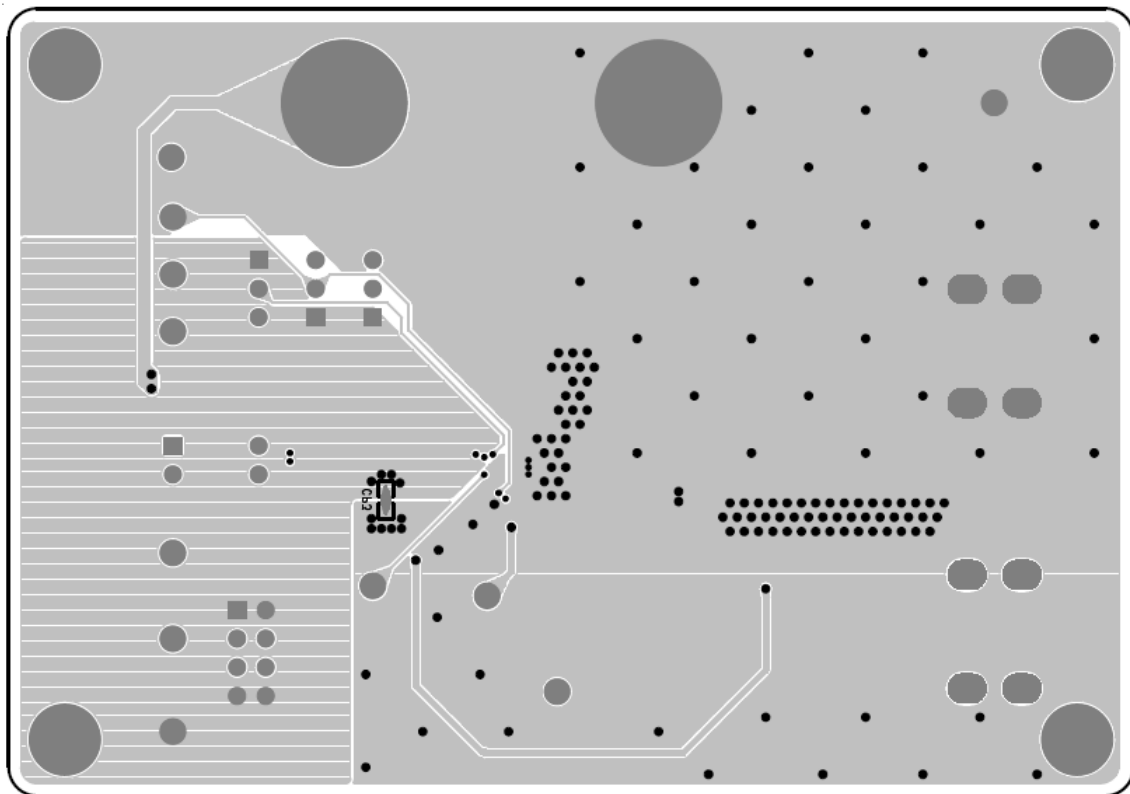Figure 15. Bottom Layer PCB Layout

Suggested Inductors for Typical Application Circuit

Component Supplier	Part No.	Inductance (μH)	DCR (mΩ)	Dimensions (mm)
WE	744314047	0.47	1.35	7.0 x 7.0 x 5.0

Recommended Component Selection for Typical Application Circuit

Component Supplier	Part No.	Capacitance (μF)	Case Size
MURATA	GRM32ER71H106KA12L	10	1210
TDK	C3225X5R1E226MT	22	1210
MURATA	GRM188R61C475KAAJ	4.7	0603

Outline Dimension
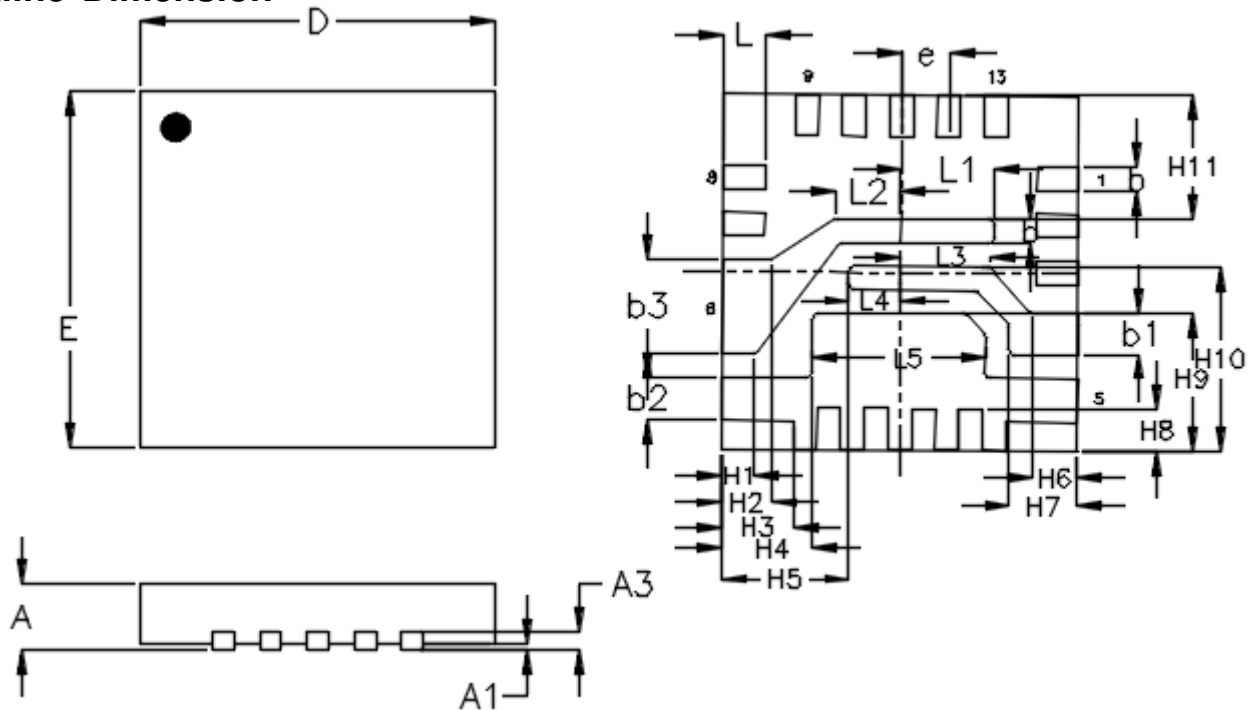
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.500	0.600	0.020	0.024
A1	0.000	0.050	0.000	0.002
A3	0.100	0.175	0.004	0.007
b	0.150	0.250	0.006	0.010
b1	0.310	0.410	0.012	0.016
b2	0.320	0.420	0.013	0.017
b3	0.740	0.840	0.029	0.033
D	2.900	3.100	0.114	0.122
E	2.900	3.100	0.114	0.122
e	0.400		0.016	
L	0.300	0.400	0.012	0.016
L1	0.740	0.840	0.029	0.033
L2	0.480	0.580	0.019	0.023
L3	0.740	0.840	0.029	0.033
L4	0.390	0.490	0.015	0.019
L5	1.410	1.510	0.056	0.059
H1	0.280		0.011	
H2	0.420		0.017	
H3	0.600		0.024	
H4	0.750		0.030	
H5	1.050		0.041	
H6	0.400		0.016	
H7	0.600		0.024	
H8	0.350		0.014	
H9	1.150		0.045	
H10	1.550		0.061	
H11	1.050		0.041	

U-Type 13L QFN 3x3 (FC) Package

Footprint Information
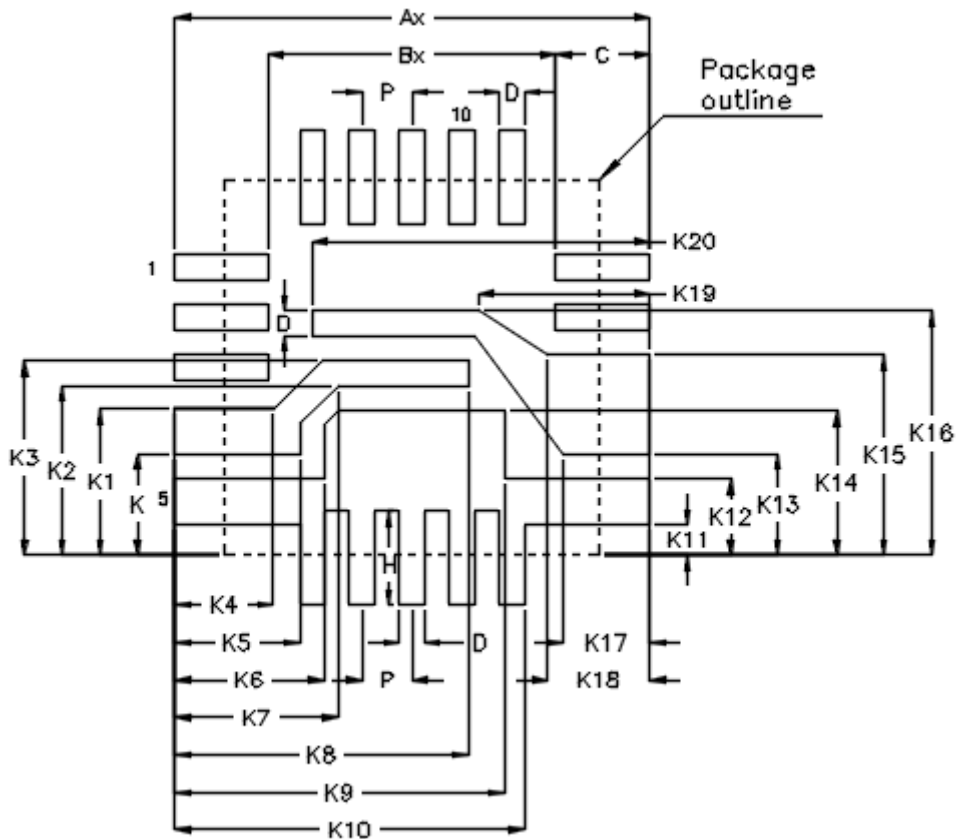
Package	Number of Pin	Footprint Dimension (mm)									Tolerance
		P	Ax	Bx	C	D	K	K1	K2	K3	
		0.40	3.80	2.30	0.75	0.20	0.80	1.17	1.35	1.55	
		K4	K5	K6	K7	K8	K9	K10	K11	K12	
UQFN3x3-13(FC)	13	0.80	1.00	1.20	1.30	2.35	2.65	2.80	0.24	0.61	±0.05
		K13	K14	K15	K16	K17	K18	K19	K20	H	
		0.80	1.15	1.60	1.95	0.68	0.82	1.37	2.70	0.75	

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