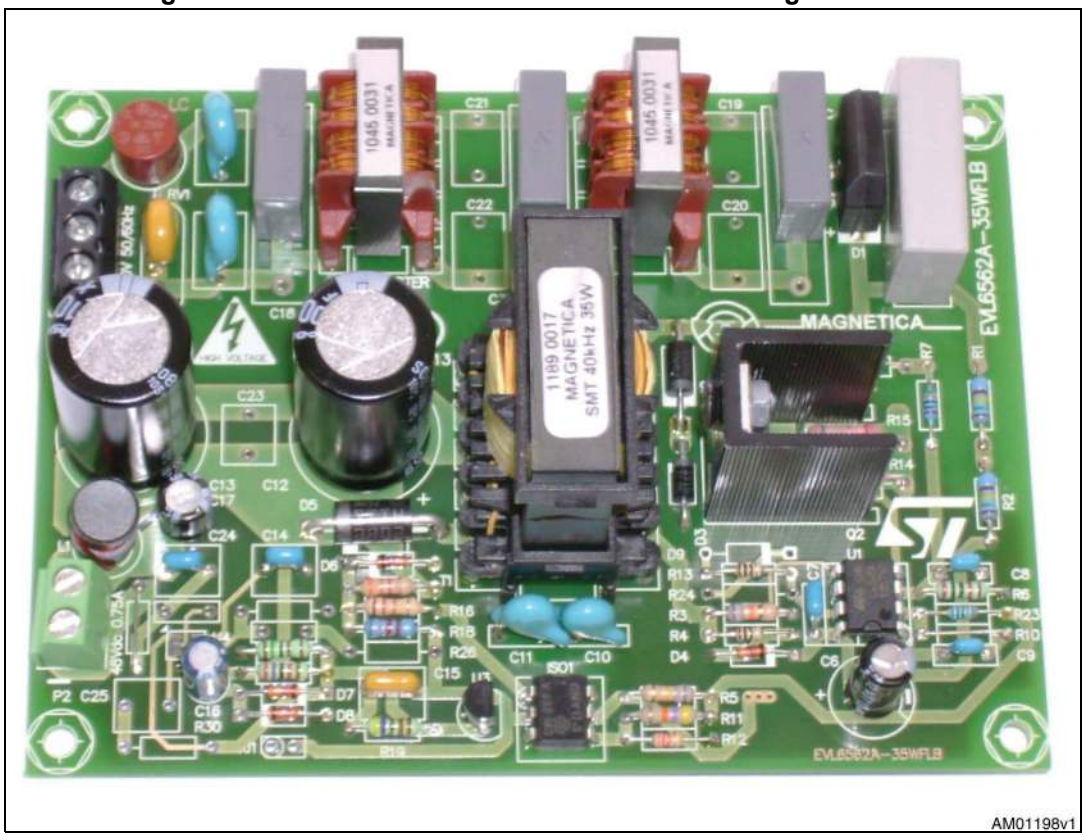
AN2838
Application note

35 W wide-range high power factor flyback converter evaluation board using the L6562A

Introduction

This application note describes a product evaluation board based on the transition-mode PFC controller L6562A, and presents the results of its bench demonstration. The board is a 35 W, wide-range mains input, power factor corrected SMPS (switched mode power supply) suitable for all low power applications requiring a high PF (power factor), such as lighting applications and power supplies for LEDs. The low-cost L6562A and the simple flyback topology combine to provide a very competitive PFC controller solution.

Figure 1. EVL6562A-35WFLB evaluation board using the L6562A



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1 Main characteristics and circuit description

The main characteristics of the SMPS evaluation board are:

- Line voltage range: 90 to 265 V_{AC}
- Minimum line frequency (f_L): 47-63 Hz
- Regulated output voltage: 48 V
- Rated output power: 35 W
- Power factor (load = 50 %): 0.9 minimum
- Minimum efficiency: 85 % at full load
- Maximum 2 f_L output voltage ripple: 1.5 V pk-pk / 0.39 V_{RMS} (@V_{IN} = 90 V_{AC}, P_{OUT} = 35 W)
- Maximum ambient temperature: 50 °C
- Conducted EMI: In acc. with EN55022 Class-B
- Surge rejection: surge test 2.5 kV
- Primary to secondary insulation: 4 kV
- PCB type and size: double-sided, 35 µm, FR-4, 120 x 82 mm

The main feature of this converter is that the input current is almost in phase with the mains voltage, therefore the power factor is close to unity. This is achieved by the L6562A controller, which shapes the input current as a sinewave in phase with the mains voltage.

The power supply utilizes a typical flyback converter topology, using a transformer to provide the required insulation between the primary and secondary side. The converter is connected after the mains rectifier and the capacitor filter, which in this case is quite small to avoid damage to the shape of the input current. The flyback switch is represented by the power MOSFET Q1, and driven by the L6562A.

At startup, the L6562A is powered by the V_{CC} capacitor (C6), which is charged via resistors R1 and R2. The TR1 auxiliary winding (pins 8-7) generates the V_{CC} voltage, rectified by D4 and R4, that powers the L6562A during normal operation. R3 is also connected to the auxiliary winding to provide the transformer demagnetization signal to the L6562A ZCD pin, turning on the MOSFET at any switching cycle. The MOSFET used is the STP5NK80ZFP, a standard, low-cost 800 V device housed in a TO-220FP package, and needing only a small heat sink. The transformer is layer type, using a standard ferrite size ETD-29 and is manufactured by Magnetica. The flyback reflected voltage is ~190 V, providing enough room for the leakage inductance voltage spike still within the reliability margin of the MOSFET. The rectifier D2 and the Transil D3 clamp the peak of the leakage inductance voltage spike at MOSFET turn-off.

The resistors R14 and R15 sense the current flowing into the transformer primary side. Once the signal at the current sense pin has reached the level programmed by the internal multiplier of the L6562A, the MOSFET turns off.

The divider R7, R8, R9 and R6 provides to the L6562A multiplier pin with instantaneous voltage information which is used to modulate the current flowing into the transformer primary side.

The divider R20 and R21 is dedicated to sensing the output voltage, and capacitor C16 and diodes D7 and D8 provide a soft-start at turn-on. Output regulation is done by means of an

isolated voltage loop by the optocoupler U2, and using an inexpensive TL431 (U3) to drive the optocoupler. The opto-transistor modulates the input voltage of the L6562A internal amplifier, thus closing the voltage loop.

The output rectifier is a fast recovery type, selected according to its maximum reverse voltage, forward voltage drop and power dissipation. A small LC filter is added on the output, filtering the high frequency ripple.

The board is equipped with an input EMI filter designed for a 3-wire input mains plug. It is composed of two, common mode Pi-filter stages connected after the input connector and the input fuse. A varistor is also connected at the input of the board, improving immunity against input voltage fast transients.

2 Electrical diagram and bill of material

Figure 2. EVL6562A-35WFLB evaluation board: electrical schematic

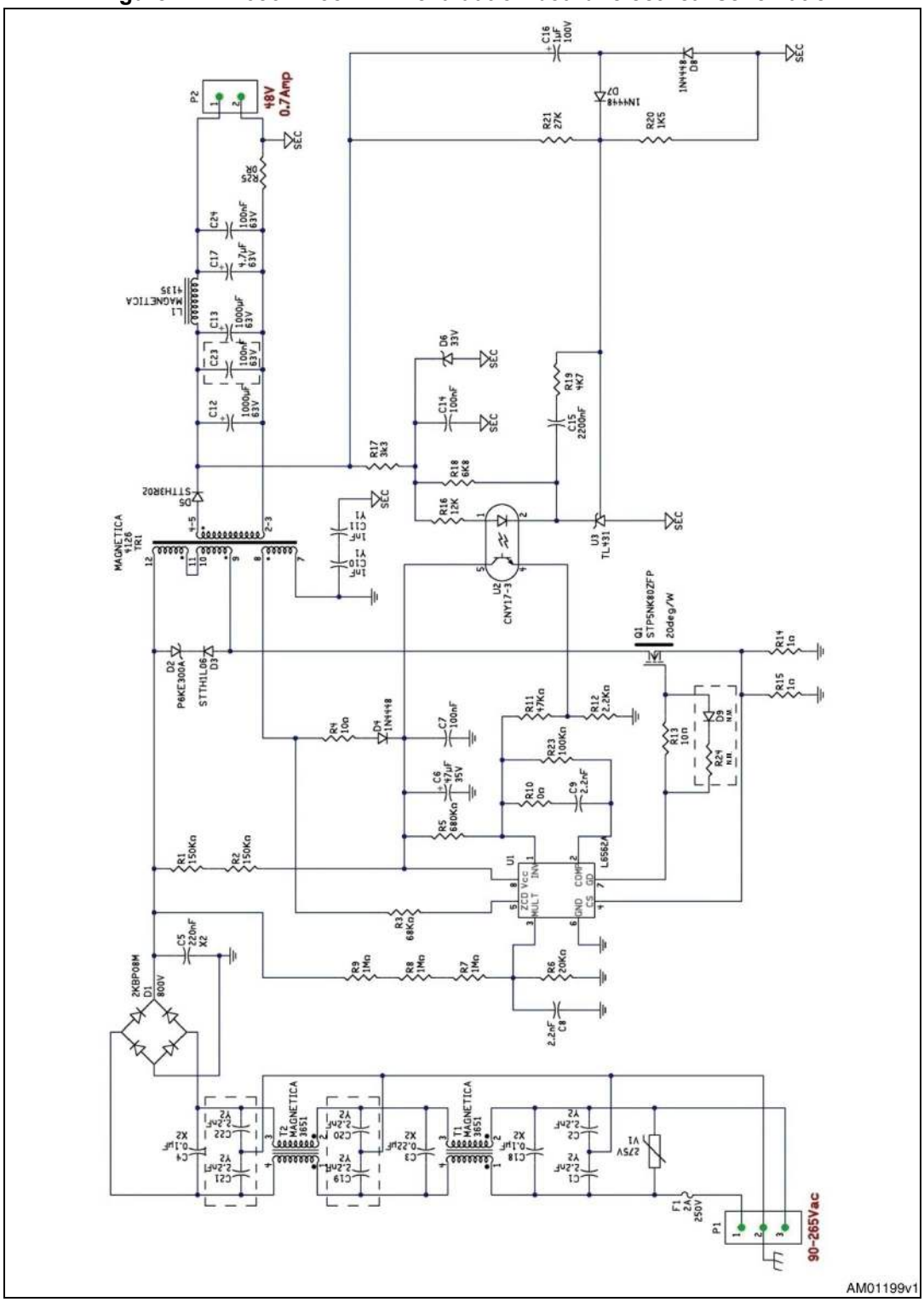


Table 1. Bill of material

Reference	Part value	Type/description	Supplier
C1	2.2 nF	Ceramic Y2	Murata
C2	2.2 nF	Ceramic Y2	Murata
C3	0.22 µF	R.46 275 V_{AC}	Arcotronics
C4	0.1 µF	R.41 MKP Y2/X1 300 V_{AC}	n.d.
C5	220 nF	MKT X2 275 V_{AC}	n.d.
C6	47 µF	35 V	n.d.
C7	100 nF	Ceramic	n.d.
C8	2.2 nF	Ceramic	n.d.
C9	2.2 nF	Ceramic	n.d.
C10	1 nF	Ceramic Y2	Murata
C11	1 nF	Ceramic Y2	Murata
C12	1000 µF	63 V 105 °C YXF	Rubycon
C13	1000 µF	63 V 105 °C YXF	Rubycon
C14	100 nF	Ceramic	n.d.
C15	2200 nF	Ceramic	n.d.
C16	1 µF	100 V	n.d.
C17	4.7 µF	63 V 105°C	Rubycon
C18	0.1 µF	R.41 MKP Y2/X1 300 V_{AC}	n.d.
C19	2.2 nF	Ceramic Y2	Murata
C20	2.2 nF	Ceramic Y2	Murata
C21	2.2 nF	Ceramic Y2	Murata
C22	2.2 nF	Ceramic Y2	Murata
C23	100 nF	Ceramic	n.d.
C24	100 nF	Ceramic	n.d.
D1	800 V, 2 A	2KBP08M diode bridge	n.d.
D2	P6KE300A	Transil	STMicroelectronics
D3	STTH1L06	Rectifier, ultra-fast 1 A, 600 V	STMicroelectronics
D4	1N4448		n.d.
D5	STTH3R02	Rectifier, ultra-fast 3 A, 200 V	STMicroelectronics
D6	33 V	Zener, 5%	n.d.
D7	1N4448		n.d.
D8	1N4448		n.d.
D9	N.M.	Not mounted	n.d.
F1	2 A, 250 V	Fuse PCB mounting	n.d.

Table 1. Bill of material (continued)

Reference	Part value	Type/description	Supplier
L1	4135	Filter inductor 15 µH/3 A	Magnetica
Q1	STP5NK80ZFP	Power MOSFET, TO-220FP w/heatsink	STMicroelectronics
R1	150 kΩ	Axial	n.d.
R2	150 kΩ	Axial	n.d.
R3	68 kΩ	Axial	n.d.
R4	10 R	Axial	n.d.
R5	680 kΩ	Axial	n.d.
R6	20 kΩ	Axial	n.d.
R7	1 MΩ	Axial	n.d.
R8	1 MΩ	Axial	n.d.
R9	1 MΩ	Axial	n.d.
R10	0 R	shorted	n.d.
R11	47 kΩ	Axial	n.d.
R12	2.2 kΩ	Axial	n.d.
R13	10 Ω	Axial	n.d.
R14	1R0	Axial, precision 5%, ¼ W	n.d.
R15	1R0	Axial, precision 5%, ¼ W	n.d.
R16	12K	Axial	n.d.
R17	3K3	Axial, ¼ W	n.d.
R18	6.8 kΩ	Axial	n.d.
R19	4.7 kΩ	Axial	n.d.
R20	1K5	Axial, precision 1%	n.d.
R21	27 kΩ	Axial, precision 1%	n.d.
R23	100 kΩ	Axial	n.d.
R24	N.M	Not mounted	n.d.
R25	0R	Shorted	
T1	3651	Common mode choke 2x18 mH	Magnetica
T2	3651	Common mode choke 2x18 mH	Magnetica
TR1	4126	Switch-mode transformer	Magnetica
U1	L6562A	TM PFC controller	STMicroelectronics
U2	CNY17-3	Optocoupler DIP-6	n.d.
U3	TL431	Voltage reference, TO-92	STMicroelectronics
V1	275 V	VDR 40J (10/1000 µs) 7 mm	n.d.

3 Test results and significant waveforms

3.1 Harmonic content measurement

One of the main purposes of this converter is the correction of input current distortion, decreasing the harmonic contents below the limits of the actual regulation. Therefore, the board has been tested according to the European standard EN61000-3-2 Class-C and Japanese standard JEIDA-MITI Class-C, at full load and both nominal input voltage mains.

As shown in figures that follow, the circuit is capable of reducing the harmonics well below the limits of both regulations.

Figure 3. EVL6562A-35WFLB compliance with EN61000-3-2 Class-C limits @ full load

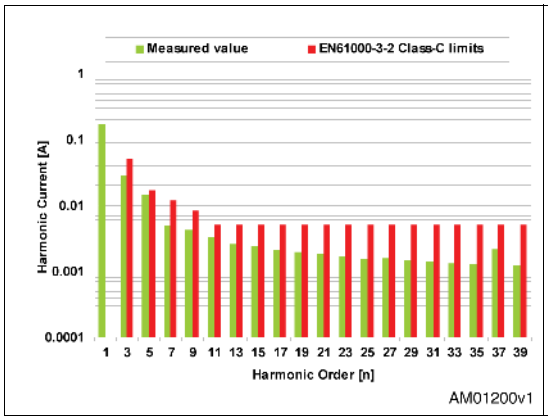
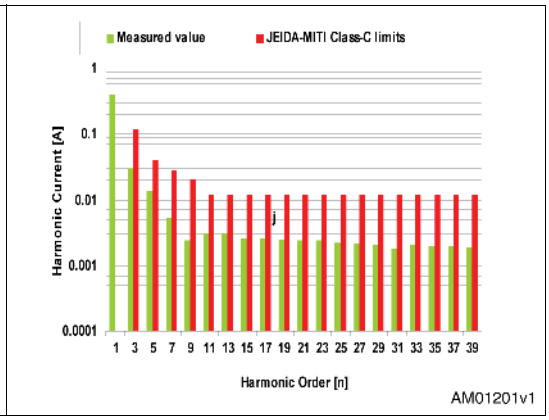
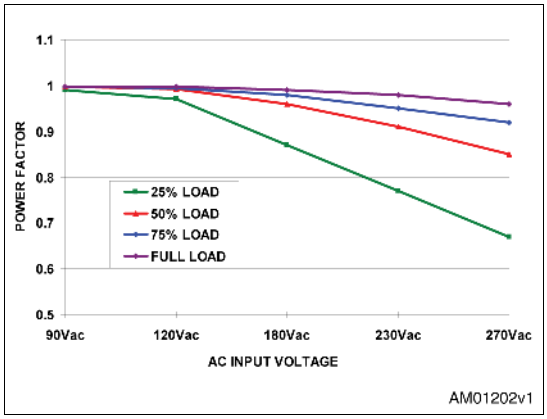


Figure 4. EVL6562A-35WFLB compliance with JEIDA-MITI Class-C limits @ full load



The power factor (PF) has been measured also and the results are reported in *Figure 5*. As shown, the PF remains very close to unity throughout the input voltage mains range.

Figure 5. Power factor vs. V_{IN} and load



The waveforms of the input current and voltage at the nominal input voltage mains and full load condition are illustrated in *Figure 6* and *Figure 7*.

Figure 6. EVL6562A-35WFLB input current waveform @100 V-50 Hz - 35 W load

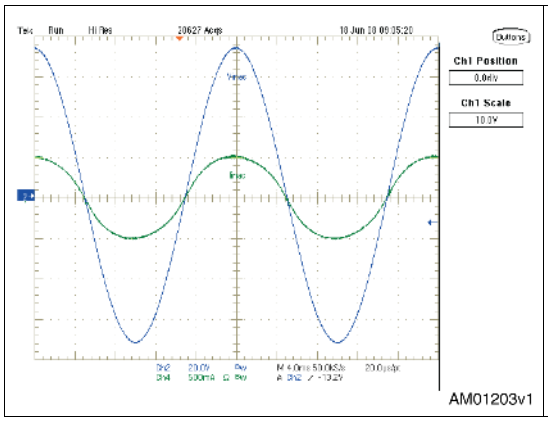
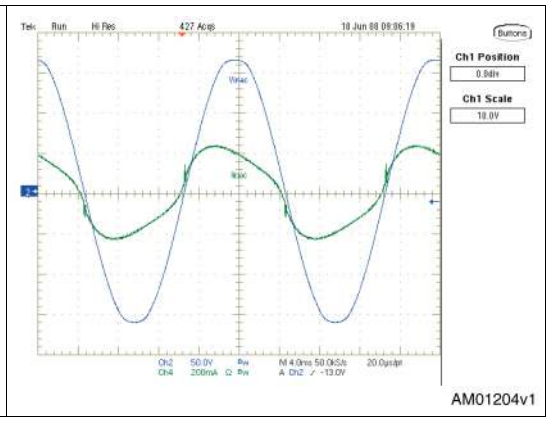


Figure 7. EVL6562A-35WFLB input current waveform @230 V-50 Hz - 35 W load



The converter's efficiency has been measured and it is significantly high in all load and line conditions (see *Figure 8*). At full load, the efficiency is higher than 85% at any input voltage, making this design suitable for high efficiency power supplies. Also, at lower output load the efficiency is better than 82%. At minimum load (40 mA output current) the efficiency is still good.

Figure 9 reports the output voltage measured under different line and load conditions. As shown, the voltage regulation over the entire input voltage range is excellent at any output current level.

Figure 8. Efficiency vs. V_{IN} and load

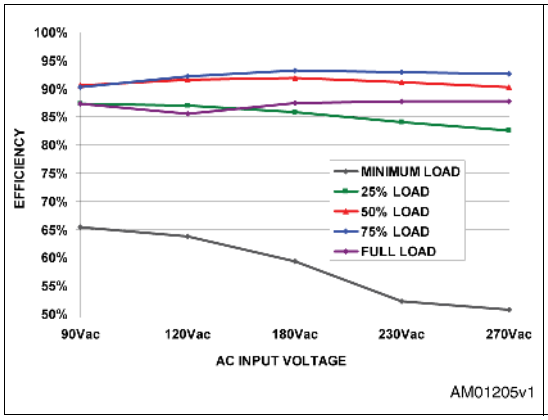


Figure 9. Static V_{OUT} regulation vs. V_{IN} and I_{OUT}

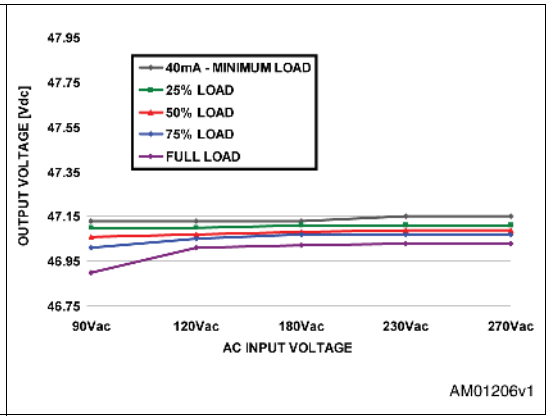


Figure 10. EVL6562A-35WFLB output voltage ripple @ 90 V_{AC} - full load

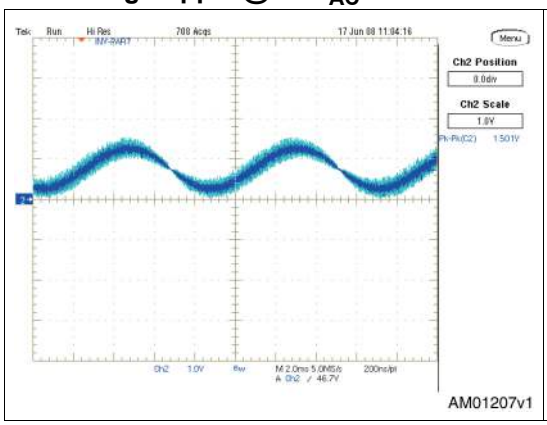
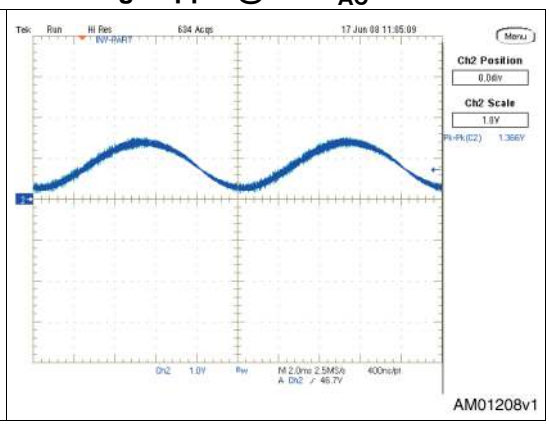


Figure 11. EVL6562A-35WFLB output voltage ripple @ 265 V_{AC} - full load



In *Figure 10* and *Figure 11* the output voltage ripple at twice the input mains frequency is measured. As shown it is less than 0.4 V peak-to-peak, which is ideal for LED or lighting applications. High frequency noise, including spikes, is significantly reduced as well.

In the following illustrations, the MOSFET drain voltage and current are measured at different line and maximum loads.

Figure 12. EVL6562A-35WFLB V_{DS} and I_D @ 90 V_{AC} - full load

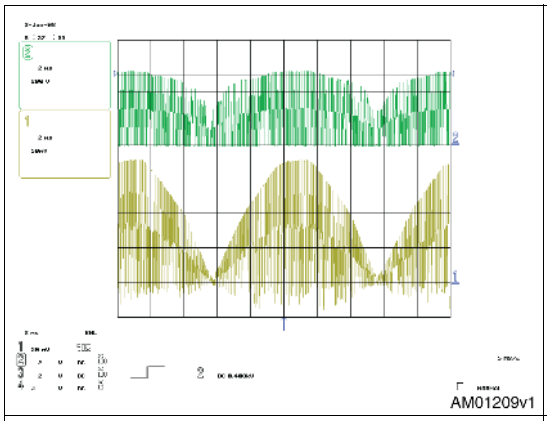
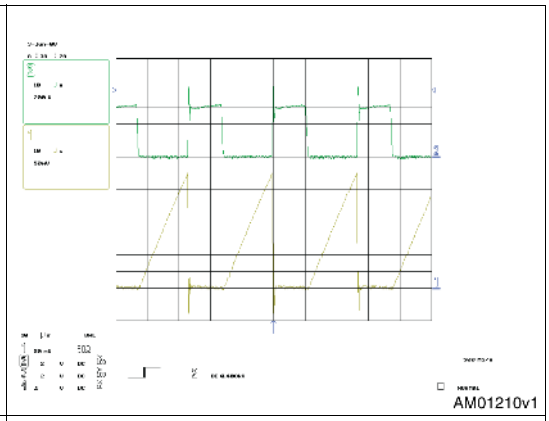
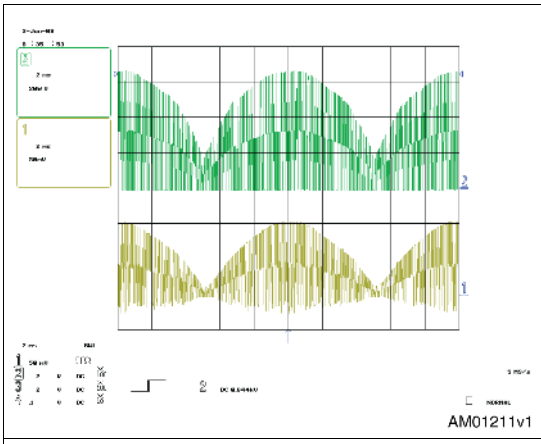


Figure 13. EVL6562A-35WFLB V_{DS} and I_D @ 90 V_{AC} - full load - detail



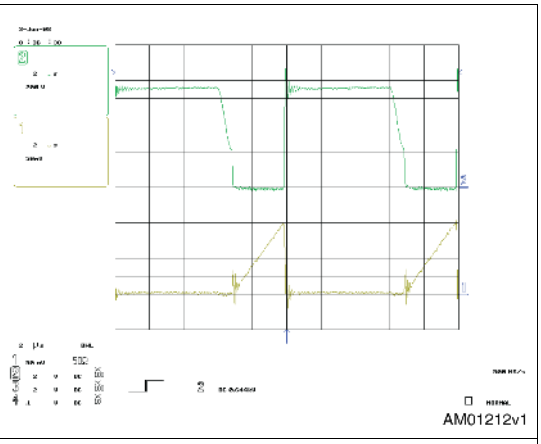
CH1: drain current - 0.5 A/div	CH1: drain current - 0.5 A/div
CH2: drain voltage - 200 V/div	CH2: drain voltage - 200 V/div

Figure 14. EVL6562A-35WFLB V_{DS} and I_D @ 265 V_{AC} - full load



CH1: drain current - 0.5 A/div
CH2: drain voltage - 200 V/div

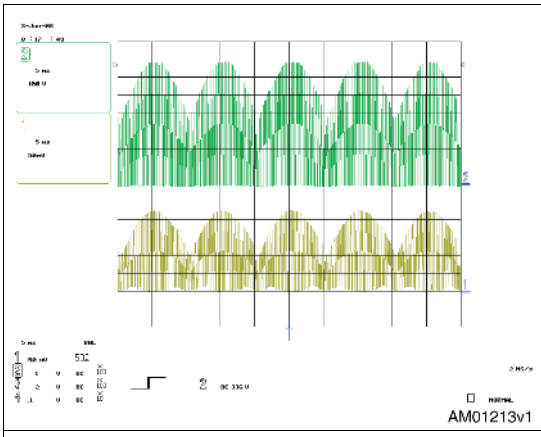
Figure 15. EVL6562A-35WFLB V_{DS} and I_D @ 265 V_{AC} - full load - detail



CH1: drain current - 0.5 A/div
CH2: drain voltage - 200 V/div

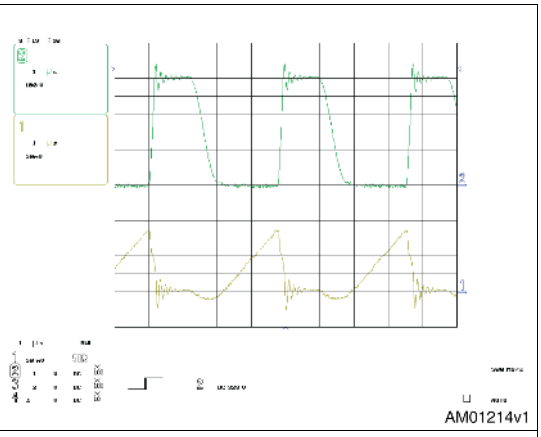
Figure 14 shows the measurement at the maximum drain voltage of 265 V_{AC} and max load. In this worst-case condition, the peak drain voltage is 640 V_{PK}, assuring a good margin with respect to the MOSFET BV_{DSS} and contributing strongly to the reliability and low failure rate of the design.

Figure 16. EVL6562A-35WFLB V_{DS} and I_D @ 90 V_{AC} - 40 mA



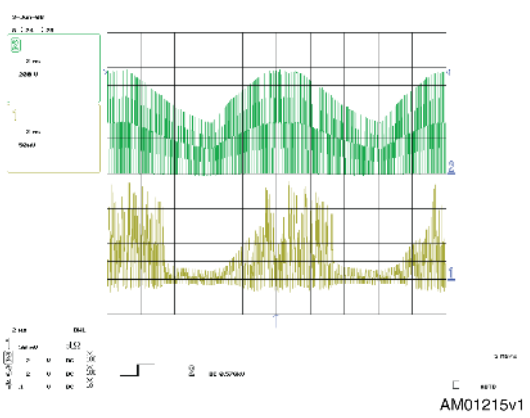
CH1: drain current - 0.1 A/div
CH2: drain voltage - 100 V/div

Figure 17. EVL6562A-35WFLB V_{DS} and I_D @ 90 V_{AC} - 40 mA - detail



CH1: drain current - 0.1 A/div
CH2: drain voltage - 100 V/div

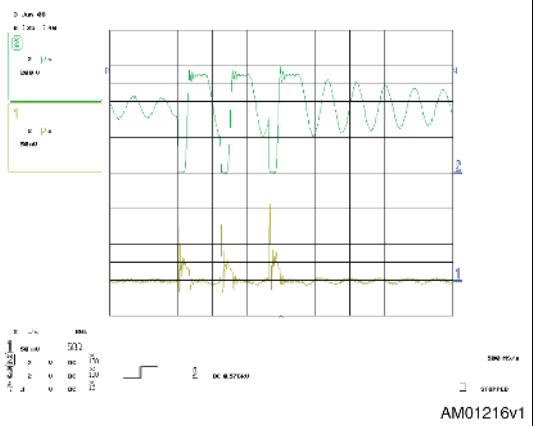
Figure 18. EVL6562A-35WFLB V_{DS} and I_D @ 265 V_{AC} - 40 mA



CH1: drain current - 0.2 A/div

CH2: drain voltage - 200 V/div

Figure 19. EVL6562A-35WFLB V_{DS} and I_D @ 265 V_{AC} - 40 mA - detail



CH1: drain current - 0.2 A/div

CH2: drain voltage - 200 V/div

The above figures show the MOSFET waveforms at light load. Even in this load condition the waveforms are correct. It can be noted that at high mains the converter works in burst mode (see *Figure 19*), keeping efficiency at a good level.

4 Thermal measurements

To check the reliability of the design, thermal mapping by means of an IR camera was carried out. *Figure 20* and *Figure 21* show thermal measurements on the component side of the board at nominal input voltages and full load. Some pointers visible on the pictures placed across key components show the relevant temperature. *Table 1* provides the correlation between the measured points and components, for both thermal maps. The ambient temperature during both measurements was 27 °C. According to these measurement results, all components on the board function within their temperature limits.

Figure 20. Thermal map at 90 V_{AC} - full load

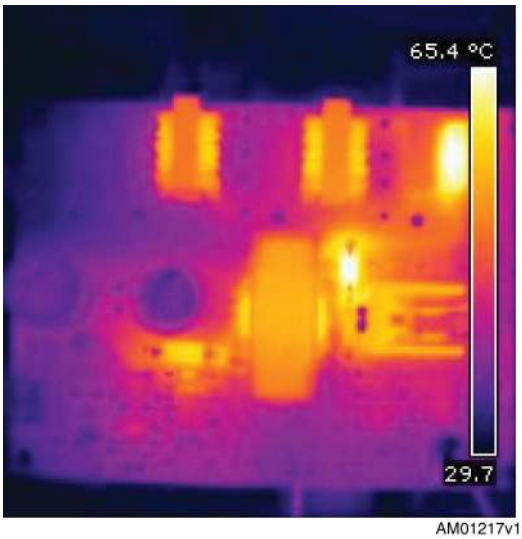


Figure 21. Thermal map at 265 V_{AC} - full load

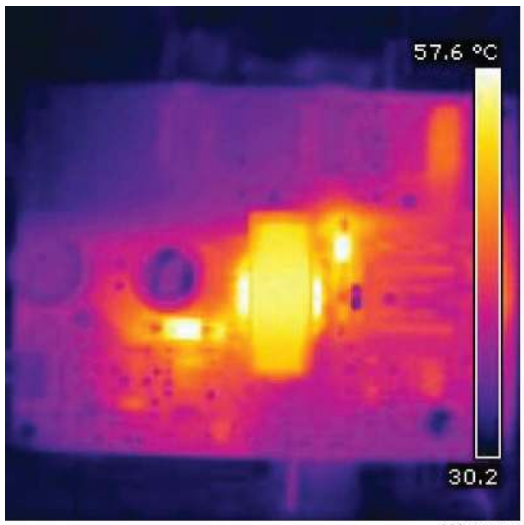


Table 2. Measured temperature @ 90 V_{AC} and 265 V_{AC} - full load

Component	Temperature @ 90 V_{AC}	Temperature @ 265 V_{AC}
MOSFET Q1	57.8 °C	43.8 °C
Secondary diode D5	58.9 °C	58.1 °C
Diode bridge D1	65.9 °C	45.6 °C
Transformer TR1 (bobbin)	64.3 °C	65.1 °C
Transformer TR1 (core)	54.5 °C	55 °C
Choke T1	55.7 °C	36. 2 °C
Choke T2	56 °C	38.2 °C
Transil D2	70 °C	59 °C

5 Conducted emission pre-compliance test

The following images are the peak measurements of the conducted noise at full load and nominal mains voltages. The limits shown on the diagrams are those of EN55022 Class-B, which is the most popular standard for domestic equipment. As visible in the diagrams, good margins with respect to the limits are present in all test conditions.

Figure 22. 115 V_{AC} and full load - phase

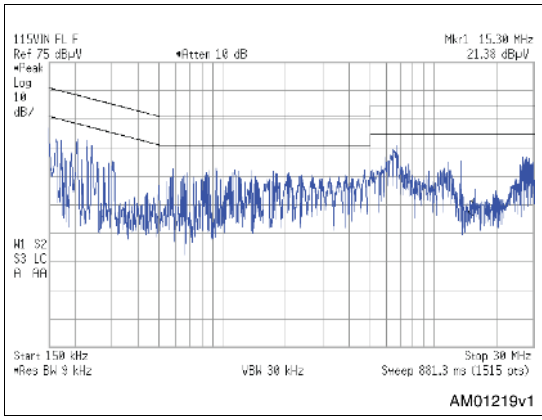


Figure 23. 115 V_{AC} and full load - neutral

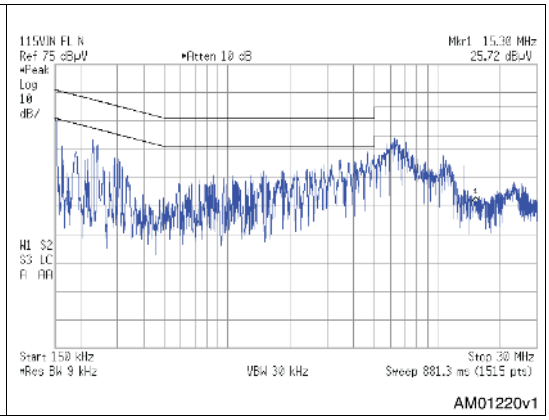


Figure 24. 230 V_{AC} and full load - phase

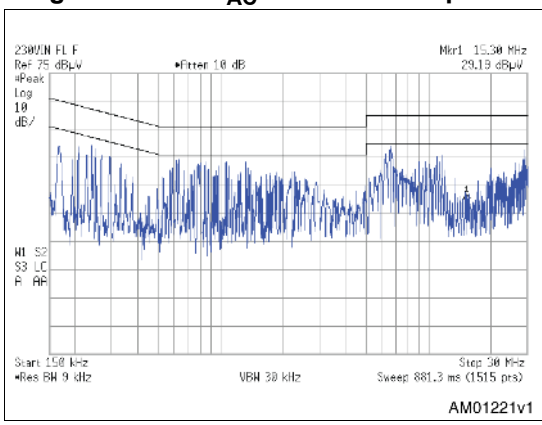
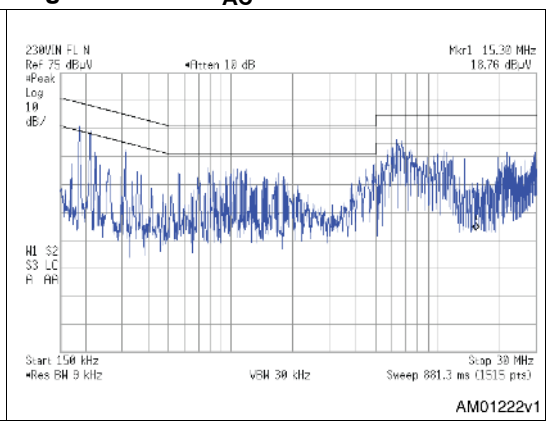


Figure 25. 230 V_{AC} and full load - neutral



6 Burst test

The board has been tested against burst pulses, with good results. The tests have been carried out using the following equipment and the procedures:

- Surge generator: Schaffner NSG 200 E 7 NSG 224 A
- Test types:
  - SYM = symmetric with respect to earth pole (pulse applied between line and neutral)
  - ASYM = asymmetric (pulse applied between line and earth and between neutral and earth)
- Output load 700 mA.

Figure 26. Burst pulse and characteristics

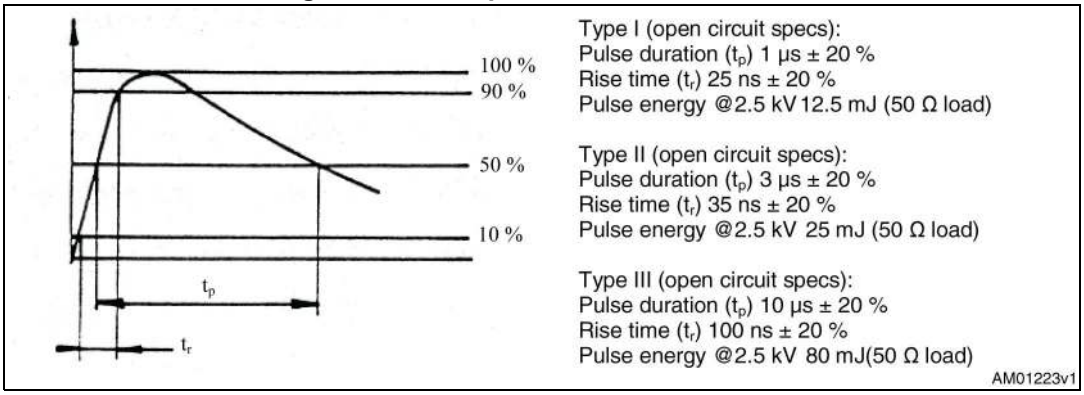


Table 3. Burst test report table

Configuration	Amplitude	Polarity and phase	Pulse type	Pulse frequency	Pulse number (burst)	Pause	Pulse number (burst)	Pause	Pulse number (burst)	Pause	Pulse number (burst)	Pause
SYM	2.5 kV	+ 90°	III	1 Hz	10	15”	10	15”	10	15”	10	15”
					10	15”						
SYM	2.5 kV	- 270°	III	1 Hz	10	15”	10	15”	10	15”	10	15”
					10	15”						
ASYM	2.5 kV	+ 90°	III	1 Hz	10	15”	10	15”	10	15”	10	15”
					10	15”						
ASYM	2.5 kV	- 270°	III	1 Hz	10	15”	10	15”	10	15”	10	15”
					10	15”						

- Test passed with a total of 200 pulses applied and a medium energy of 80 mJ (when connected to a 50 Ω load).

7 Schematic with output voltage and current loop

All tests described in this document have been done using the schematic in *Figure 1* and using a TL431 for the output voltage feedback. If a secondary current loop is also needed, the schematic below can be implemented on the PCB by making the modifications listed in *Table 4*.

The proposed schematic has been designed to drive LEDs with a current rating of 700 mA. For correct board functionality the minimum output voltage when the current loop is working is around 30 V. Therefore, the minimum number of LEDs in series that can be connected to the output must be calculated according to this minimum output voltage value.

Figure 27. Electrical schematic with secondary current feedback

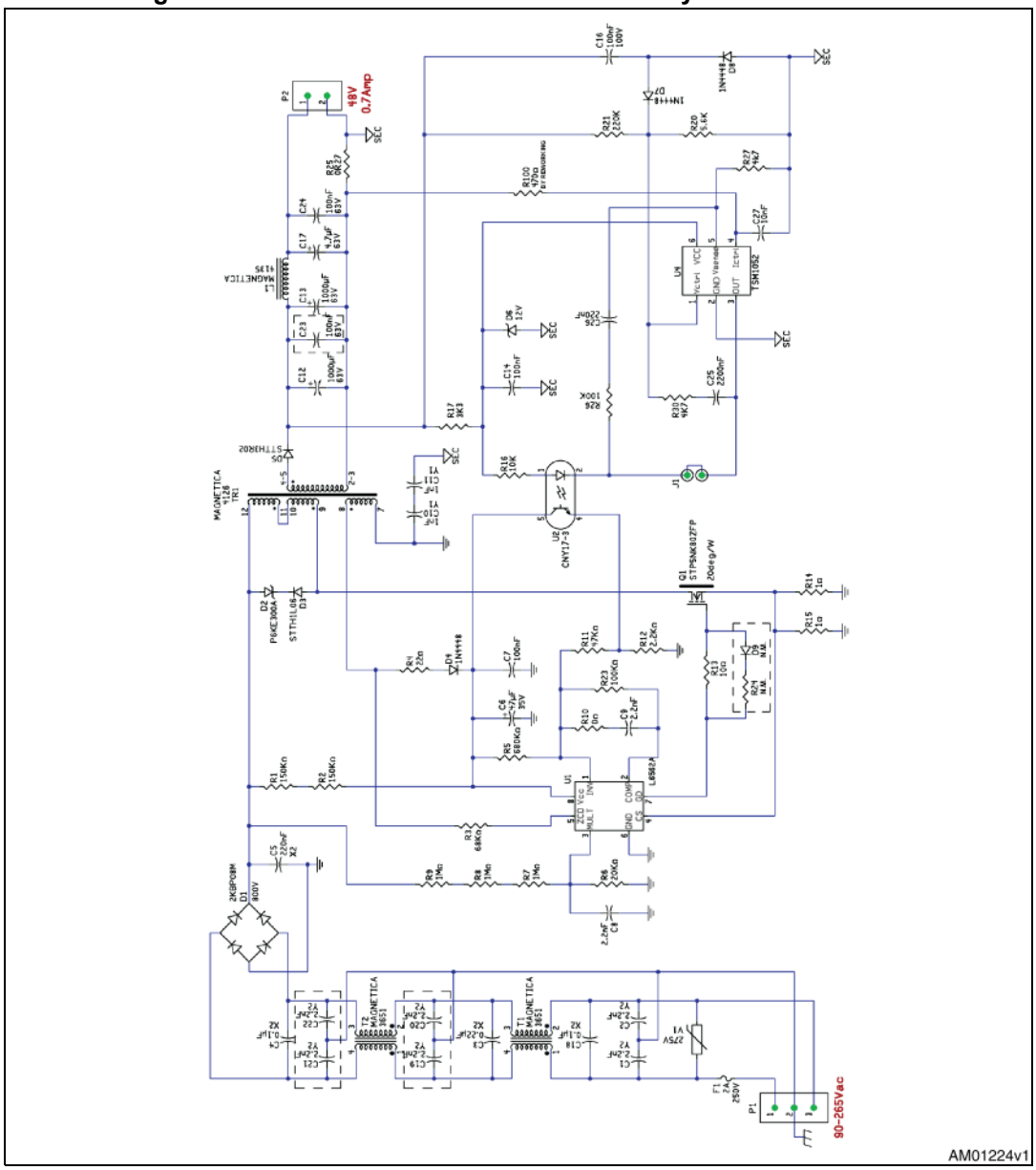


Table 4. Modification list for TSM1052 implementation

Reference	Part value	Modification	Type/ Description
C15		Removed	
C16	100 nF	Changed value	Ceramic
C25	2.2 nF	Added	Ceramic
C26	220 nF	Added	Ceramic
C27	10 nF	Added	Ceramic
D6	12 V	Changed value	Zener, 5%
R4	22 R	Changed value	Axial
R16	10 kΩ	Changed value	Axial
R18		Removed	
R19		Removed	
R20	5K6	Changed value	Axial, precision 1%
R21	220 kΩ	Changed value	Axial, precision 1%
R25	0R27	Added	Axial 2 W
R26	100 kΩ	Added	Axial
R27	4K7	Added	Axial
R30	4K7	Added	Axial
R100	470R	Mounted by reworking of PCB	Axial
J1	JUMPER	Added	Wire jumper
U3		Removed	
U4	TSM1052 STMicroelectronics	Added	Current/voltage controller

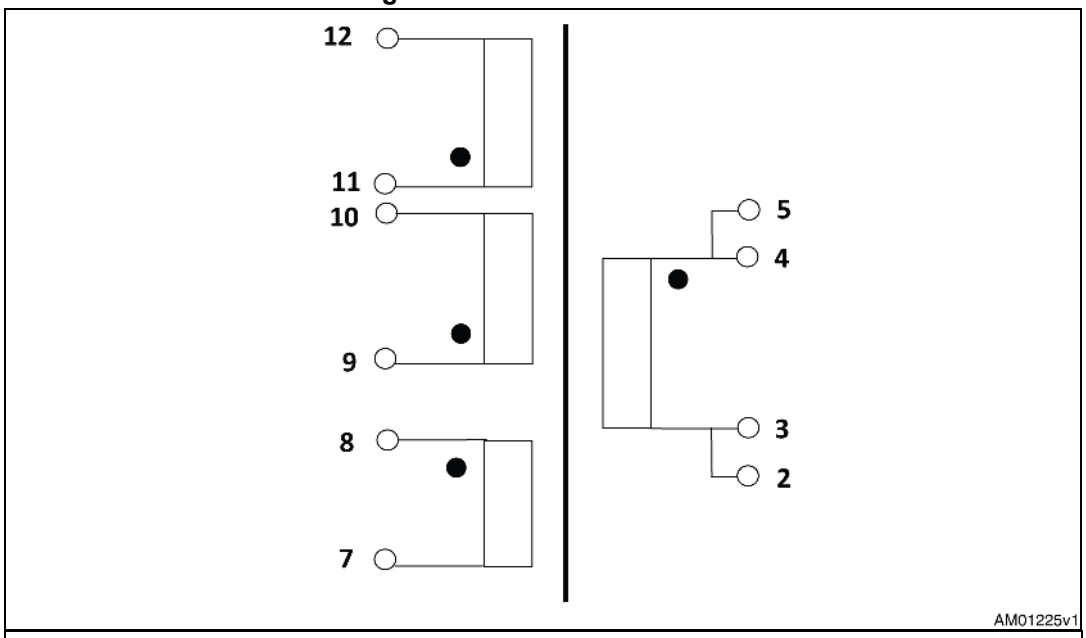
8 Power transformer specification

- Transformer type: open
  - Winding type: layer
  - Coil former: vertical type, 6 + 6 pins
  - Mains insulation: 4 kV
  - Unit finishing: varnished

Electrical characteristics (all measurements taken with pins 10 and 11 shorted)

- Converter topology: flyback, TM mode
- Core type: ETD29
- Min. operating frequency: 36 kHz
- Primary inductance: 550 mH 10% @ 1 kHz - 0.25 V [(a)]
- Leakage inductance: 4.5 mH@ 50 kHz - 0.25 V [(b)]
- Parasitic capacitance: 7 pF max.
- Max. peak primary current: 1.9 A_{PK}
- Turn ratio:
  - Pin 9-12 / 8-7: 10.55 ± 5%
  - Pin 9-12 / 5/4-3/2: 3.8 ± 5%

Figure 28. Power transformer



Manufacturer: Magnetica
P/N: 4126

a. Measured between pins (9-12)

b. Measured between pins (9-12) with all secondary windings shorted

9 References

- L6562A transition-mode PFC controller datasheet
- Application note AN1059: Design equations of high-power-factor flyback converters based on the L6561
- Application note AN1060: Flyback converters with the L6561 PFC controller

10 Revision history

Table 5. Document revision history

Date	Revision	Changes
12-Nov-2008	1	Initial release
20-Jan-2014	2	– Updated *Figure 2*, *Table 1*, *Figure 27* and *Chapter 8* – Modified board nomenclature