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## **WB2072-00**

**Bluetooth® Low Energy**

**Wireless MCU Module**

**ST BlueNRG-355AC Solution**

**Datasheet**

**Revision 0.3**

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## 1. OVERVIEW

The certified WB2072-00 module from JORJIN is a wireless MCU module targeting Bluetooth 5.2 low energy applications. This module is based on ST BlueNRG-355AC wireless MCU QFN-32 package chip.

The module is a cost-effective, ultralow power, 2.4-GHz RF devices. Very low active RF and MCU current and low-power mode current consumption provide excellent battery lifetime and allow for operation on small coin cell batteries and in energy-harvesting applications.

### 1.1. General Features

- STMicroelectronics BlueNRG-LP, 32MHz & 32.768KHz crystals, DC2DC, and chip antenna on a single module.
- Built-in STMicroelectronics BlueNRG-LP, 5x5mm QFN32 (20 GPIOs)
- 2.4-GHz RF Transceiver and Integrated Antenna.
- Bluetooth Low Energy system-on-chip supporting Bluetooth 5.2 specifications:
  - 2 Mbps data rate
  - Long Range (Coded PHY)
  - Advertising Extensions
  - Channel Selection Algorithm #2
  - GATT caching
- Data rate supported: 2 Mbps, 1 Mbps, 500 kbps and 125 kbps
- Operating supply voltage: from 1.7 to 3.6 V
- High performance and ultra-low power Cortex-M0+ 32-bit, 64 MHz
- 256KB Flash, 64KB SRAM, 1KB OTP, 7KB ROM, MPU
- Dynamic current consumption: 18  $\mu$ A/MHz
- Extensive peripheral set: 2 x SPI / I2S, 1x SPI, 2 x I<sup>2</sup>C, 1 x USART, 1 x UART, 6 x PWM, 1 x PDM, 1 x 12-bit ADC
- Supply and reset management
  - High efficiency embedded SMPS step-down converter
  - Ultra-low-power Power-On-Reset (POR) and Power-Down-Reset (PDR)
  - Programmable Voltage Detector (PVD)
- Embedded UART bootloader
- Enhanced security mechanisms such as:
  - Flash read/write protection
  - SWD access can be disabled
  - Secure bootloader
- LGA-42pins package.

- Dimension 15mm(L) x 11mm(W) x 2.6mm(H)
- Temperature range: -40 °C to +85 °C temperature range
- RoHS Compliance
- Suitable for Systems Targeting Compliance With Worldwide Radio Frequency Regulations
  - ETSI EN 300 328 (Europe)
  - FCC CFR47 Part 15 (US)
  - IC RSS-247 (Canada)
  - ARIB STD-T66 (Japan)
  - NCC LP0002 (Taiwan)
  - AS/NZS 4268 (Australia/New Zealand)
  - KN 301 489 (South Korea)
- Development support
  - Serial wire debug (SWD)
  - 4 breakpoints and 2 watchpoints
- All packages are ECOPACK®2 compliant.

## 1.2. Applications

- Industrial
- Home and Industrial automation
- Smart Lighting
- Fitness, wellness and sports
- Healthcare, consumer medical
- Security/proximity
- Remote Control
- Assisted Living
- Mobile Phone peripherals
- PC peripherals

## 2. FUNCTIONAL FEATURES

### 2.1. Module Block Diagram

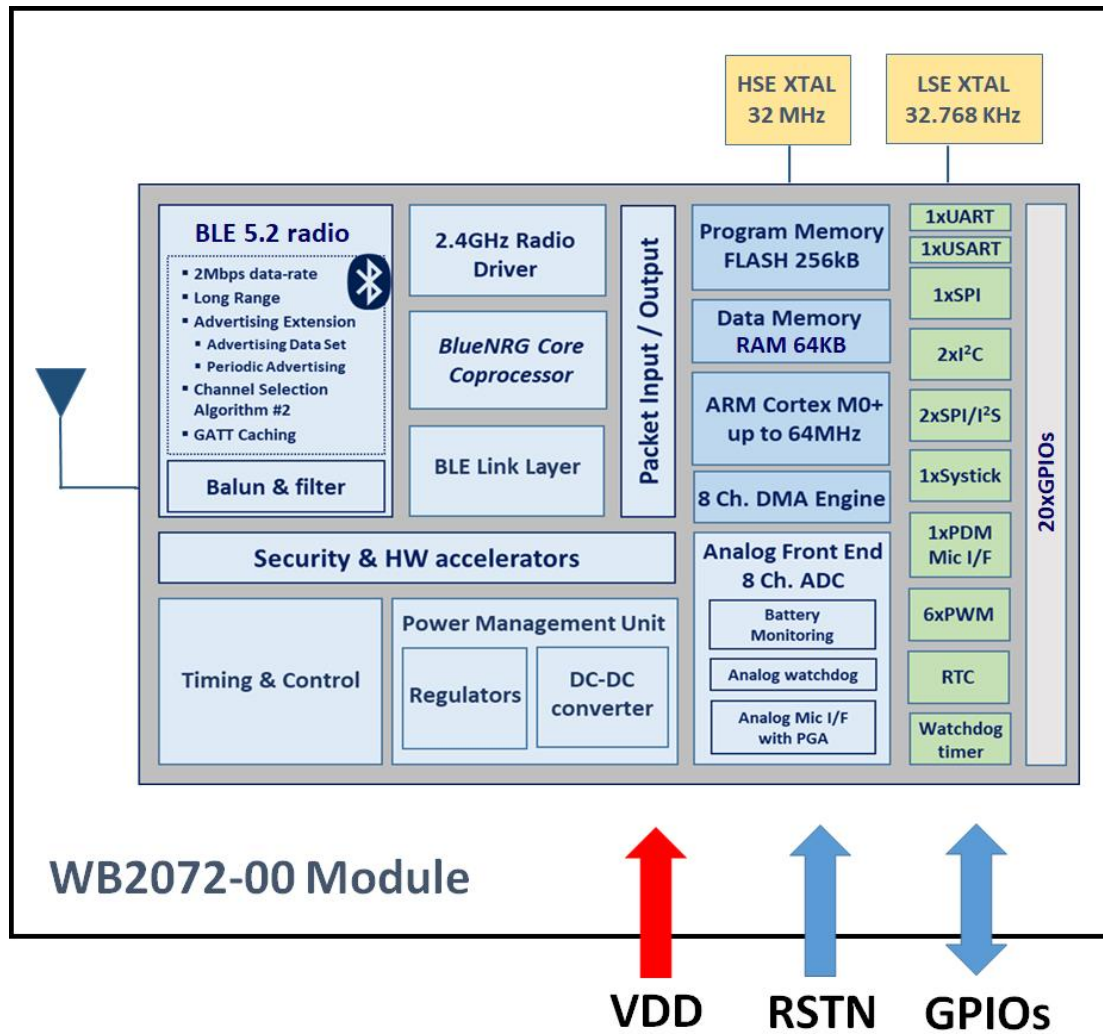


Figure 1 – Module block diagram

### 3. MODULE OUTLINE

#### 3.1. Signal Layout (Top View)

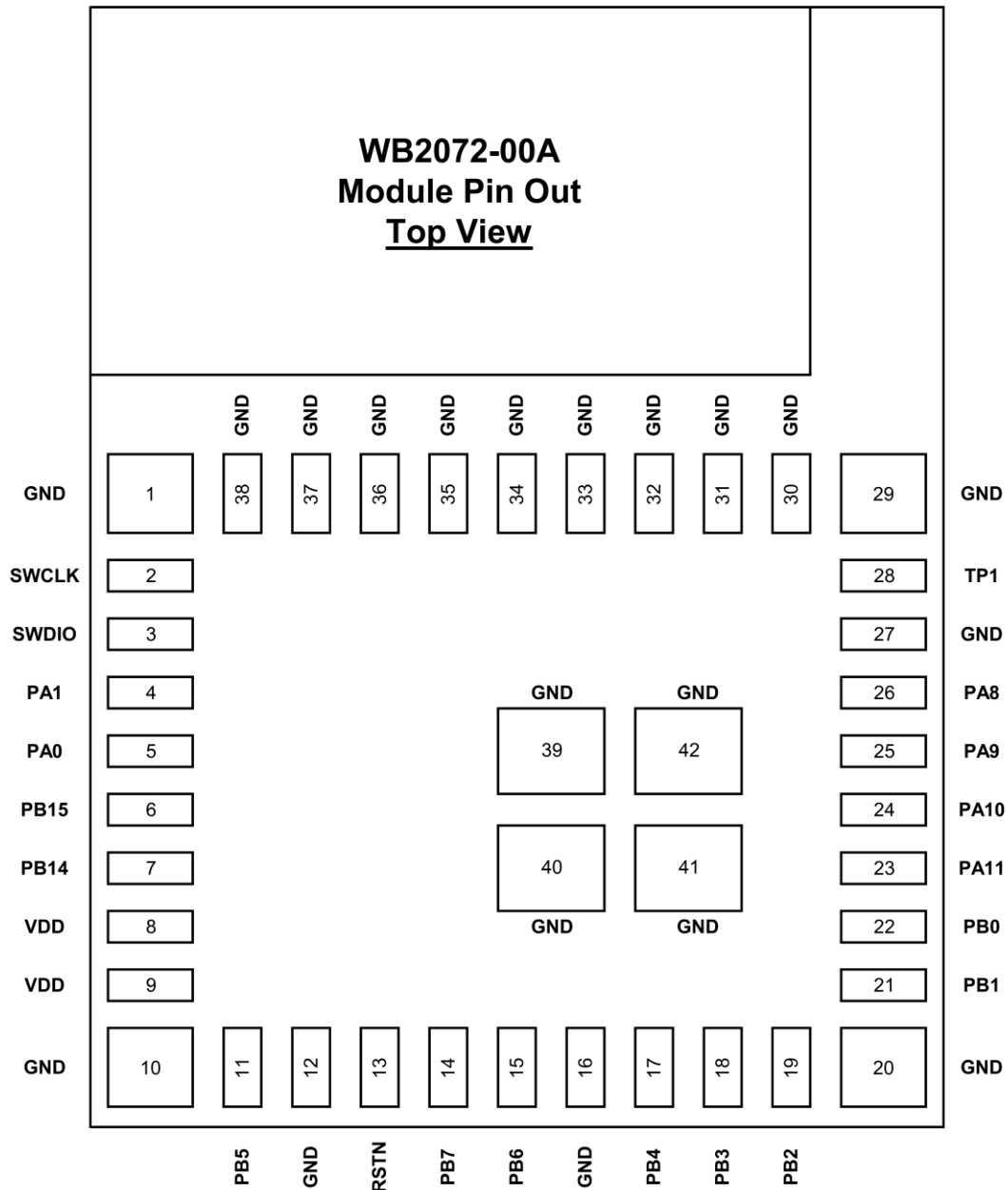


Figure 2 –Pinout top view

### 3.2. Pin Description

**Table1 –Pin Description**

| Pin No. | Pin Name  | Type | Description  |
|---------|-----------|------|--|
| 1       | GND       | S    | Ground   |
| 2       | BLE_SWCLK | I/O  | BLE_SWCLK to CMSIS-DAP for programming                                   |
| 3       | BLE_SWDIO | I/O  | BLE_SWDIO to CMSIS-DAP for programming                                   |
| 4       | PA1       | I/O  | I2C1_SDA, SPI2_MISO, USART_TX, TIM1_CH4                                  |
| 5       | PA0       | I/O  | I2C1_SCL, USART_CTS, SPI2_MCK, TIM1_CH3                                  |
| 6       | PB15      | I/O  | I2C1_SMBA, TX_SEQUENCE, MCO, TIM1_CH4N, TIM1_CH6, USART_TX               |
| 7       | PB14      | I/O  | SPI1_MOSI, I2C2_SDA, TIM1_ETR, TIM1_CH3N, TIM1_CH5, USART_RX             |
| 8       | VDD_MOD   | S    | 1.7-3.6 battery voltage input  |
| 9       | VDD_MOD   | S    | 1.7-3.6 battery voltage input  |
| 10      | GND       | S    | Ground   |
| 11      | PB5       | I/O  | LPUART_RX, SPI2_MOSI, PDM_CLK  |
| 12      | GND       | S    | Ground   |
| 13      | BLE_RSTN  | I/O  | Reset, active-low. No internal pull-up. Built-in 0.1uF capacitor to GND. |
| 14      | PB7       | I/O  | I2C2_SDA, SPI2_SCK, LPUART_RX, TIM1_CH2                                  |
| 15      | PB6       | I/O  | I2C2_SCL, SPI2_NSS, LPUART_TX, TIM1_CH1                                  |
| 16      | GND       | S    | Ground   |
| 17      | PB4       | I/O  | LPUART_TX, SPI2_MISO, PDM_DATA   |
| 18      | PB3       | I/O  | USART_CTS, LPUART_TX, TIM1_CH4   |
| 19      | PB2       | I/O  | USART_RTS_DE, PDM_DATA, TIM1_CH3   |
| 20      | GND       | S    | Ground   |
| 21      | PB1       | I/O  | SPI1_NSS, PDM_CLK, TIM1_ETR  |
| 22      | PB0       | I/O  | USART_RX, LPUART_RTS_DE, TIM1_CH2N                                       |
| 23      | PA11      | I/O  | MCO, SPI1_NSS, SPI3_MOSI, TIM1_CH6                                       |
| 24      | PA10      | I/O  | LCO, SPI1_MISO, SPI3_MCK, TIM1_CH5                                       |
| 25      | PA9       | I/O  | USART_TX, SPI1_SCK, RTC_OUT, SPI3_NSS, TIM1_CH4                          |
| 26      | PA8       | I/O  | USART_RX, SPI1_MOSI, SPI3_MISO, TIM1_CH3                                 |
| 27      | GND       | S    | Ground   |
| 28      | TP1       | I/O  | NC   |
| 29~38   | GND       | S    | Ground   |
| 39~42   | GND       | S    | Ground   |



## 4. MODULE SPECIFICATIONS

### 4.1. Parameter conditions

Unless otherwise specified, all voltages are referenced to ground (GND).

#### 4.1.1 Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the following standard conditions:

- Ambient temperature is  $T_A = 25\text{ }^\circ\text{C}$
- Supply voltage is VDD: 3.3 V
- System clock frequency is 32 MHz (clock source HSI)
- SMPS clock frequency is 4 MHz

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean  $\pm 3\sigma$ ).

#### 4.1.2 Typical values

Unless otherwise specified, typical data are based on  $T_A = 25\text{ }^\circ\text{C}$ , VDD = 3.3 V. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean  $\pm 2\sigma$ ).

### 4.2. Absolute maximum ratings and thermal data

Stresses above the absolute maximum ratings listed in the tables below, may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

*Table 2 - Voltage characteristics*

| Symbol | Ratings | MIN | MAX | Unit |
|--------|---------|-----|-----|------|
|--------|---------|-----|-----|------|

|                          |   |      |      |   |
|--------------------------|---|------|------|---|
| VDD_MOD                  | DC-DC converter supply voltage input    | -0.3 | +3.9 | V |
| PA0 to PA15, PB0 to PB15 | DC voltage on digital input/output pins | -0.3 | +3.9 | V |

Note: All the main power and ground pins must always be connected to the external power supply, in the permitted range.

**Table 3 - Current characteristics**

| Symbol               | Ratings  | MAX | Unit |
|----------------------|--|-----|------|
| $\Sigma IV_{DD}$     | Total current into sum of all VDD power lines (source)           | 130 | mA   |
| $\Sigma IV_{GND}$    | Total current out of sum of all ground lines (sink)              | 130 |      |
| $IV_{DD(PIN)}$       | Maximum current into each VDD power pin (source)                 | 100 |      |
| $IV_{GND(PIN)}$      | Maximum current out of each ground pin (sink)                    | 100 |      |
| $I_{IO(PIN)}$        | Output current sunk by any I/O and control pin                   | 20  |      |
|                      | Output current sourced by any I/O and control pin                | 20  |      |
| $\Sigma I_{IO(PIN)}$ | Total output current sunk by sum of all I/Os and control pins    | 100 |      |
|                      | Total output current sourced by sum of all I/Os and control pins | 100 |      |

**Table 4 - Thermal characteristics**

| Symbol    | Ratings                      | Value       | Unit |
|-----------|------------------------------|-------------|------|
| $T_{STG}$ | Storage temperature range    | -40 to +125 | °C   |
| $T_J$     | Maximum junction temperature | 125         | °C   |

### 4.3. Operating conditions

#### 4.3.1 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

The MCU is put under the following conditions:

- All I/O pins are in analog input mode
- All peripherals are disabled except when explicitly mentioned
- The Flash memory access time is adjusted with the minimum wait states number
- When the peripherals are enabled  $f_{PCLK} = f_{HCLK}$

**Table 5- Current consumption**

| Symbol                     | Parameter                                 | Conditions                                 | Typ. | Unit |
|----------------------------|---|--|------|------|
| I <sub>DD</sub> (RUN)      | Supply current in RUN mode                | fHCLK = 64 MHz<br>All peripherals disabled | 2.40 | mA   |
|                            |   | fHCLK = 32 MHz<br>All peripherals disabled | 1.98 |      |
|                            |   | fHCLK = 16 MHz<br>All peripherals disabled | 1.62 |      |
| I <sub>DD</sub> (DEEPSTOP) | Supply current in DEEPSTOP <sup>(1)</sup> | Timer OFF                                  | 0.65 | μA   |
|                            |   | Timer source LSI                           | 1.25 |      |
|                            |   | Timer source LSI<br>RTC ON                 | 1.30 |      |
|                            |   | Timer source LSI<br>IWDG ON                | 1.27 |      |
|                            |   | Timer source LSI<br>RTC and IWDG ON        | 1.33 |      |
|                            |   | Timer source LSE                           | 1.00 |      |
|                            |   | Timer source LSE<br>RTC ON                 | 1.06 |      |
|                            |   | Timer source LSE<br>IWDG ON                | 1.02 |      |
|                            |   | Timer source LSE<br>RTC and IWDG ON        | 1.07 |      |
| I <sub>DD</sub> (SHUTDOWN) | Supply current in SHUTDOWN                |  | 0.12 | μA   |
| I <sub>DD</sub> (RST)      | Current under reset condition             |  | 1.34 | mA   |

(1) The current consumption in DEEPSTOP is measured considering the entire SRAM retained.

**Table 6- Peripheral current consumption at VDD = 3.3 V, sysclk at 32 MHz, SMPS on**

| Parameter | Test conditions | Typ. | Unit |
|-----------|-----------------|------|------|
| ADC       |                 | 80   | μA   |
| DMA       |                 | 39   |      |
| GPIOA     |                 | 2    |      |
| GPIOB     |                 | 2    |      |
| I2C1      |                 | 40   |      |
| I2C2      |                 | 39   |      |

|         |                            |     |               |
|---------|----------------------------|-----|---------------|
| I2S2    | Peripheral clock at 32 MHz | 46  | $\mu\text{A}$ |
| I2S3    | Peripheral clock at 32 MHz | 47  |               |
| IWDG    |                            | 11  |               |
| LPUART  |                            | 52  |               |
| PKA     |                            | 50  |               |
| RNG     |                            | 64  |               |
| RTC     |                            | 14  |               |
| SPI1    |                            | 35  |               |
| SPI2    | Peripheral clock at 16 MHz | 40  |               |
| SPI3    | Peripheral clock at 16 MHz | 42  |               |
| Systick |                            | 8   |               |
| TIM1    |                            | 248 |               |
| USART   |                            | 81  |               |
| SYSCFG  |                            | 33  |               |
| THSENS  |                            | 301 |               |
| CRC     |                            | 9   |               |

#### 4.3.2 General operating conditions

*Table 7- General operating conditions*

| Symbol              | Parameter  | Conditions                | MIN  | MAX                 | Unit               |
|---------------------|--|---------------------------|------|---------------------|--------------------|
| $f_{\text{HCLK}}$   | Internal AHB clock frequency   |                           | 1    | 64                  | MHz                |
| $f_{\text{PCLK0}}$  | Internal APB0 clock  |                           | 1    | 64                  |                    |
| $f_{\text{PCLK1}}$  | Internal APB1 clock  |                           | 1    | 64                  |                    |
| $f_{\text{PCLK2}}$  | Internal APB2 clock frequency  |                           | 16   | 32                  |                    |
| $V_{\text{DD}}$     | Standard operating voltage   |                           | 1.7  | 3.6                 | V                  |
| $V_{\text{FBSMPS}}$ | SMPS feedback voltage  |                           | 1.4  | 3.6                 |                    |
| $V_{\text{DDRF}}$   | Minimum RF voltage   |                           | 1.7  | 3.6                 |                    |
| $V_{\text{IN}}$     | I/O input voltage  |                           | -0.3 | $V_{\text{DD}}+0.3$ |                    |
| $P_{\text{D}}$      | Power dissipation at $T_{\text{A}}=85\text{ }^{\circ}\text{C}^{(1)}$ |                           |      | 30                  | mW                 |
| $T_{\text{A}}$      | Ambient temperature  | Maximum power dissipation | -40  | 85                  | $^{\circ}\text{C}$ |
| $T_{\text{J}}$      | Junction temperature range   |                           | -40  | 85                  |                    |

(1)  $T_{\text{A}}$  cannot exceed the  $T_{\text{J}}$  max.

### 4.3.3 RF general characteristics

All performance data are referred to a 50  $\Omega$  antenna connector, via reference design.

**Table 8- Bluetooth Low energy RF general characteristics**

| Symbol             | Parameter  | Test conditions   | Min. | Typ.      | Max.      | Unit |
|--------------------|--|---|------|-----------|-----------|------|
| F <sub>RANGE</sub> | Frequency range <sup>(1)</sup>   |   | 2400 |           | 2483.5    | MHz  |
| RF <sub>CH</sub>   | RF channel center frequency <sup>(1)</sup>                                       |   | 2402 |           | 2480      | MHz  |
| PLL <sub>RES</sub> | RF channel spacing <sup>(1)</sup>  |   |      | 2         |           | KHz  |
| $\Delta F$         | Frequency deviation <sup>(1)</sup>   |   |      | 250       |           | KHz  |
| $\Delta f1$        | Frequency deviation average <sup>(1)</sup>                                       |   | 450  |           | 550       | KHz  |
| C <sub>Fdev</sub>  | Center frequency deviation <sup>(1)</sup>  | During the packet and including both initial frequency offset and drift |      |           | $\pm 150$ | KHz  |
| $\Delta fa$        | Frequency deviation $\Delta f2$ (average) / $\Delta f1$ (average) <sup>(1)</sup> |   | 0.80 |           |           |      |
| R <sub>gfsk</sub>  | On air data rate <sup>(1)</sup>  |   | 1    |           | 2         | Mbps |
| STacc              | Symbol time accuracy <sup>(1)</sup>  |   |      |           | $\pm 50$  | ppm  |
| MOD                | Modulation scheme  |   | GFSK |           |           |      |
| BT                 | Bandwidth-bit period product   |   |      | 0.5       |           |      |
| Mindex             | Modulation index <sup>(1)</sup>  |   | 0.45 | 0.5       | 0.55      |      |
| PMAX               | Maximum Output   | At antenna connector, VSMP5 = 1.9 V, LDO code                           | 6.3  | 7         | 7.7       | dBm  |
| PMIN               | Minimum Output   | At antenna connector  |      | -20       |           | dBm  |
| PRFC               | RF power accuracy  | @ 27°C  |      | $\pm 1.5$ |           | dB   |
|                    |  | All temperatures  |      | $\pm 2.5$ |           |      |

(1) Tested according to Bluetooth SIG radio frequency physical layer (RF PHY) test suite.

### 4.3.4 RF transmitter characteristics

All performance data are referred to a 50  $\Omega$  antenna connector, via reference design.

**Table 9- Bluetooth Low Energy RF Transmitter characteristics at 1 Mbps not coded**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|--------|-----------|-----------------|------|------|------|------|
|--------|-----------|-----------------|------|------|------|------|

|                   |  |  |     |    |     |                |
|-------------------|--|--|-----|----|-----|----------------|
| $P_{BW1M}$        | 6 dB Bandwidth for modulated carrier                               | Using resolution bandwidth of 100kHz   | 550 |    |     | KHz            |
| $P_{RF1, 1 Ms/s}$ | In-band emission at $\pm 2\text{MHz}^{(1)}$                        | Using resolution bandwidth of 100 kHz and average detector                   |     |    | -20 | dBm            |
| $P_{RF2, 1 Ms/s}$ | In-band emission at $\pm[3+n]\text{MHz}$ , where $n=0,1,2..^{(1)}$ | Using resolution bandwidth of 100 kHz and average detector                   |     |    | -30 | dBm            |
| $P_{SPUR}$        | Spurious emission  | Harmonics included. Using resolution bandwidth of 1 MHz and average detector |     |    | -41 | dBm            |
| $Freq_{drift}$    | Frequency drift  | Integration interval #n – integration interval #0, where $n=2,3,4..k$        | -50 |    | +50 | KHz            |
| $IFreq_{drift}$   | Initial carrier frequency drift <sup>(1)</sup>                     | Integration interval #1 – integration interval #0                            | -23 |    | +23 | KHz            |
| $IntFreq_{drift}$ | Intermediate carrier frequency drift <sup>(1)</sup>                | Integration interval #n – integration interval #(n-5), where $n=6,7,8..k$    | -20 |    | +20 | KHz            |
| $DriftRate_{max}$ | Maximum drift rate <sup>(1)</sup>                                  | Between any two 10-bit groups separated by 50 $\mu$ s                        | -20 |    | +20 | KHz/50 $\mu$ s |
| $Z_{RF1}$         | Optimum RF load (Impedance at RF1 pin)                             | @ 2440 MHz   |     | 40 |     | $\Omega$       |

(1) Tested according to Bluetooth SIG radio frequency physical layer (RF PHY) test suite.

**Table 10- Bluetooth Low Energy RF Transmitter characteristics at 2 Mbps not coded**

| Symbol           | Parameter  | Test conditions  | Min. | Typ. | Max. | Unit |
|------------------|--|--|------|------|------|------|
| $P_{BW1M}$       | 6 dB Bandwidth for modulated carrier                               | Using resolution bandwidth of 100kHz   | 670  |      |      | KHz  |
| $P_{RF1, 2Ms/s}$ | In-band emission at $\pm 4\text{MHz}^{(1)}$                        | Using resolution bandwidth of 100kHz and average detector                    |      |      | -20  | dBm  |
| $P_{RF2, 2Ms/s}$ | In-band emission at $\pm 5\text{MHz}^{(1)}$                        | Using resolution bandwidth of 100kHz and average detector                    |      |      | -20  | dBm  |
| $P_{RF3, 2Ms/s}$ | In-band emission at $\pm[6+n]\text{MHz}$ , where $n=0,1,2..^{(1)}$ | Using resolution bandwidth of 100kHz and average detector                    |      |      | -30  | dBm  |
| $P_{SPUR}$       | Spurious emission  | Harmonics included. Using resolution bandwidth of 1 MHz and average detector |      |      | -41  | dBm  |

|                          |   |   |     |    |     |          |
|--------------------------|---|---|-----|----|-----|----------|
| Freq <sub>drift</sub>    | Frequency drift <sup>(1)</sup>                      | Integration interval #n – integration interval #0, where n=2,3,4..k     | -50 |    | +50 | KHz      |
| IFreq <sub>drift</sub>   | Initial carrier frequency drift <sup>(1)</sup>      | Integration interval #1 – integration interval #0                       | -23 |    | +23 | KHz      |
| IntFreq <sub>drift</sub> | Intermediate carrier frequency drift <sup>(1)</sup> | Integration interval #n – integration interval #(n-5), where n=6,7,8..k | -20 |    | +20 | KHz      |
| DriftRate <sub>max</sub> | Maximum drift rate <sup>(1)</sup>                   | Between any two 10-bit groups separated by 50µs                         | -20 |    | +20 | KHz/50µs |
| Z <sub>RF1</sub>         | Optimum RF load (Impedance at RF1 pin)              | @ 2440 MHz  |     | 40 |     | Ω        |

(1) Tested according to Bluetooth SIG radio frequency physical layer (RF PHY) test suite.

**Table 11- Bluetooth Low Energy RF Transmitter characteristics at 1 Mbps LE coded (S=8)**

| Symbol                     | Parameter   | Test conditions  | Min.  | Typ. | Max.  | Unit     |
|----------------------------|---|--|-------|------|-------|----------|
| P <sub>BW</sub>            | 6 dB Bandwidth for modulated carrier                          | Using resolution bandwidth of 100kHz   | 500   |      |       | KHz      |
| P <sub>RF1, LE coded</sub> | In-band emission at ±2MHz <sup>(1)</sup>                      | Using resolution bandwidth of 100kHz and average detector                    |       |      | -20   | dBm      |
| P <sub>RF2, LE coded</sub> | In-band emission at ±[3+n]MHz, where n=0,1,2.. <sup>(1)</sup> | Using resolution bandwidth of 100kHz and average detector                    |       |      | -30   | dBm      |
| P <sub>SPUR</sub>          | Spurious emission   | Harmonics included. Using resolution bandwidth of 1 MHz and average detector |       |      | -41   | dBm      |
| Freq <sub>drift</sub>      | Frequency drift <sup>(1)</sup>                                | Integration interval #n – integration interval #0, where n=1,2,3..k          | -50   |      | +50   | KHz      |
| IFreq <sub>drift</sub>     | Initial carrier frequency drift <sup>(1)</sup>                | Integration interval #3 – integration interval #0                            | -19.2 |      | +19.2 | KHz      |
| IntFreq <sub>drift</sub>   | Intermediate carrier frequency drift <sup>(1)</sup>           | Integration interval #n – integration interval #(n-3), where n=7,8,9..k      | -19.2 |      | +19.2 | KHz      |
| DriftRate <sub>max</sub>   | Maximum drift rate <sup>(1)</sup>                             | Between any two 16-bit groups separated by 48µs                              | -19.2 |      | +19.2 | KHz/48µs |
| Z <sub>RF1</sub>           | Optimum RF load (Impedance at RF1 pin)                        | @ 2440 MHz   |       | 40   |       | Ω        |

(1) Tested according to Bluetooth SIG radio frequency physical layer (RF PHY) test suite.

### 4.3.5 RF receiver characteristics

All performance data are referred to a 50  $\Omega$  antenna connector, via reference design.

**Table 12- Bluetooth Low Energy RF receiver characteristics at 1 Msym/s uncoded**

| Symbol   | Parameter   | Test conditions   | Min. | Typ. | Max. | Unit     |
|--|---|---|------|------|------|----------|
| RX <sub>SENS</sub>   | Sensitivity   | PER < 30.8%   | -    | -94  |      | dBm      |
| P <sub>SAT</sub>   | Saturation  | PER < 30.8%   |      | 8    |      | dBm      |
| Z <sub>RF1</sub>   | Optimum RF source<br>(Impedance at RF1 pin)   | @ 2440 MHz  |      | 40   |      | $\Omega$ |
| RF selectivity with BLE equal modulation on interfering signal |   |   |      |      |      |          |
| C/I <sub>CO-channel</sub>                                      | Co-channel interference $f_{RX} = f_{interference}$                                     | Wanted signal=-67dBm, PER < 30.8%                                   |      | 8    |      | dBc      |
| C/I <sub>1 MHz</sub>   | Adjacent Interference<br>$f_{interference} = f_{RX} \pm 1\text{MHz}$                    | Wanted signal=-67dBm, PER < 30.8%                                   |      | -1   |      | dBc      |
| C/I <sub>2 MHz</sub>   | Adjacent Interference<br>$f_{interference} = f_{RX} \pm 2\text{MHz}$                    | Wanted signal=-67dBm, PER < 30.8%                                   |      | -35  |      | dBc      |
| C/I <sub>3 MHz</sub>   | Adjacent Interference<br>$f_{interference} = f_{RX} \pm (3+n)\text{MHz}$ [n = 0,1,2...] | Wanted signal=-67dBm, PER < 30.8%                                   |      | -47  |      | dBc      |
| C/I <sub>Image</sub>   | Image frequency Interference<br>$f_{interference} = f_{image}$                          | Wanted signal=-67dBm, PER < 30.8%                                   |      | -25  |      | dBc      |
| C/I <sub>Image<math>\pm</math>1 MHz</sub>                      | Adjacent channel to image frequency<br>$f_{interference} = f_{image} \pm 1\text{MHz}$   | Wanted signal=-67dBm, PER < 30.8%                                   |      | -25  |      | dBc      |
| Out of Band Blocking (Interfering signal CW)                   |   |   |      |      |      |          |
| C/I <sub>Block</sub>   | Interfering signal frequency<br>30MHz – 2000 MHz  | Wanted signal=-67dBm, PER < 30.8%,<br>Measurement resolution 10 MHz |      | 5    |      | dBm      |
| C/I <sub>Block</sub>   | Interfering signal frequency<br>2003 MHz – 2399 MHz                                     | Wanted signal=-67dBm, PER < 30.8%,<br>Measurement resolution 3MHz   |      | -5   |      | dBm      |
| C/I <sub>Block</sub>   | Interfering signal frequency<br>2484 MHz – 2997 MHz                                     | Wanted signal=-67dBm, PER < 30.8%,<br>measurement resolution 3MHz   |      | -5   |      | dBm      |
| C/I <sub>Block</sub>   | Interfering signal frequency  | Wanted signal=-67dBm, PER < 30.8%,                                  |      | 10   |      | dBm      |



|   |  |                                   |  |     |  |     |
|---|--|-----------------------------------|--|-----|--|-----|
|   | 3000 MHz – 12.75 GHz   | measurement resolution 25MHz      |  |     |  |     |
| Intermodulation characteristics (CW signal at f1, BLE interfering signal at f2) |  |                                   |  |     |  |     |
| P_IM(3)   | Input power of IM interferer at 3 and 6 MHz distance from wanted signal    | Wanted signal=-64dBm, PER < 30.8% |  | -27 |  | dBm |
| P_IM(-3)  | Input power of IM interferer at -3 and -6 MHz distance from wanted signal  | Wanted signal=-64dBm, PER < 30.8% |  | -40 |  | dBm |
| P_IM(4)   | Input power of IM interferer at ±4 and ±8 MHz distance from wanted signal  | Wanted signal=-64dBm, PER < 30.8% |  | -32 |  | dBm |
| P_IM(5)   | Input power of IM interferer at ±5 and ±10 MHz distance from wanted signal | Wanted signal=-64dBm, PER < 30.8% |  | -32 |  | dBm |

**Table 13- Bluetooth Low Energy RF receiver characteristics at 2 Msym/s uncoded**

| Symbol   | Parameter  | Test conditions                   | Min. | Typ. | Max. | Unit |
|--|--|-----------------------------------|------|------|------|------|
| RX <sub>SENS</sub>   | Sensitivity  | PER < 30.8%                       | -    | -91  |      | dBm  |
| P <sub>SAT</sub>   | Saturation   | PER < 30.8%                       |      | 8    |      | dBm  |
| Z <sub>RF1</sub>   | Optimum RF source<br>(Impedance at RF1 pin)  | @ 2440 MHz                        |      | 40   |      | Ω    |
| RF selectivity with BLE equal modulation on interfering signal |  |                                   |      |      |      |      |
| C/I <sub>CO-channel</sub>                                      | Co-channel interference<br>$f_{RX} = f_{interference}$                                   | Wanted signal=-67dBm, PER < 30.8% |      | 8    |      | dBc  |
| C/I <sub>2 MHz</sub>   | Adjacent Interference<br>$f_{interference} = f_{RX} \pm 2\text{MHz}$                     | Wanted signal=-67dBm, PER < 30.8% |      | -14  |      | dBc  |
| C/I <sub>4MHz</sub>  | Adjacent Interference<br>$f_{interference} = f_{RX} \pm 4\text{MHz}$                     | Wanted signal=-67dBm, PER < 30.8% |      | -41  |      | dBc  |
| C/I <sub>6 MHz</sub>   | Adjacent Interference<br>$f_{interference} = f_{RX} \pm (6+2n)\text{MHz}$ [n = 0,1,2...] | Wanted signal=-67dBm, PER < 30.8% |      | -45  |      | dBc  |
| C/I <sub>Image</sub>   | Image frequency Interference<br>$f_{interference} = f_{image-2M}$                        | Wanted signal=-67dBm, PER < 30.8% |      | -25  |      | dBc  |
| C/I <sub>Image±1 MHz</sub>                                     | Adjacent channel to image  | Wanted signal=-67dBm, PER < 30.8% |      | -14  |      | dBc  |

|   |   |   |  |     |  |     |
|---|---|---|--|-----|--|-----|
|   | frequency<br>$f_{\text{interference}} = f_{\text{image}-2M} \pm 2\text{MHz}$                | 30.8%   |  |     |  |     |
| Out of Band Blocking (Interfering signal CW)  |   |   |  |     |  |     |
| $C/I_{\text{Block}}$  | Interfering signal frequency<br>30MHz – 2000 MHz  | Wanted signal=-67dBm, PER < 30.8%,<br>Measurement resolution 10 MHz |  | 5   |  | dBm |
| $C/I_{\text{Block}}$  | Interfering signal frequency<br>2003 MHz – 2399 MHz   | Wanted signal=-67dBm, PER < 30.8%,<br>Measurement resolution 3MHz   |  | -5  |  | dBm |
| $C/I_{\text{Block}}$  | Interfering signal frequency<br>2484 MHz – 2997 MHz   | Wanted signal=-67dBm, PER < 30.8%,<br>measurement resolution 3MHz   |  | -5  |  | dBm |
| $C/I_{\text{Block}}$  | Interfering signal frequency<br>3000 MHz – 12.75 GHz  | Wanted signal=-67dBm, PER < 30.8%,<br>measurement resolution 25MHz  |  | 10  |  | dBm |
| Intermodulation characteristics (CW signal at $f_1$ , BLE interfering signal at $f_2$ ) |   |   |  |     |  |     |
| $P_{\text{IM}}(6)$  | Input power of IM interferer at<br>6 and 12 MHz distance from<br>wanted signal              | Wanted signal=-64dBm, PER < 30.8%                                   |  | -27 |  | dBm |
| $P_{\text{IM}}(-6)$   | Input power of IM interferer at<br>-6 and -12 MHz distance from<br>wanted signal            | Wanted signal=-64dBm, PER < 30.8%                                   |  | -30 |  | dBm |
| $P_{\text{IM}}(8)$  | Input power of IM interferer at<br>$\pm 8$ and $\pm 16$ MHz distance from<br>wanted signal  | Wanted signal=-64dBm, PER < 30.8%                                   |  | -30 |  | dBm |
| $P_{\text{IM}}(10)$   | Input power of IM interferer at<br>$\pm 10$ and $\pm 20$ MHz distance from<br>wanted signal | Wanted signal=-64dBm, PER < 30.8%                                   |  | -28 |  | dBm |

**Table 14- Bluetooth Low Energy RF receiver characteristics at 1 Msym/s LE coded ( $S=2$ )**

| Symbol   | Parameter  | Test conditions                   | Min. | Typ. | Max. | Unit     |
|--|--|-----------------------------------|------|------|------|----------|
| $RX_{\text{SENS}}$   | Sensitivity  | PER < 30.8%                       | -    | -97  |      | dBm      |
| $P_{\text{SAT}}$   | Saturation   | PER < 30.8%                       |      | 8    |      | dBm      |
| $Z_{\text{RF1}}$   | Optimum RF source<br>(Impedance at RF1 pin)                          | @ 2440 MHz                        |      | 40   |      | $\Omega$ |
| RF selectivity with BLE equal modulation on interfering signal |  |                                   |      |      |      |          |
| $C/I_{\text{CO-channel}}$                                      | Co-channel interference<br>$f_{\text{RX}} = f_{\text{interference}}$ | Wanted signal=-79dBm, PER < 30.8% |      | 2    |      | dBc      |

|                            |   |                                   |  |     |  |     |
|----------------------------|---|-----------------------------------|--|-----|--|-----|
| C/I <sub>1</sub> MHz       | Adjacent Interference<br>$f_{\text{interference}} = f_{\text{RX}} \pm 1\text{MHz}$                    | Wanted signal=-79dBm, PER < 30.8% |  | -5  |  | dBc |
| C/I <sub>2</sub> MHz       | Adjacent Interference<br>$f_{\text{interference}} = f_{\text{RX}} \pm 2\text{MHz}$                    | Wanted signal=-79dBm, PER < 30.8% |  | -38 |  | dBc |
| C/I <sub>3</sub> MHz       | Adjacent Interference<br>$f_{\text{interference}} = f_{\text{RX}} \pm (3+n)\text{MHz}$ [n = 0,1,2...] | Wanted signal=-79dBm, PER < 30.8% |  | -50 |  | dBc |
| C/I <sub>Image</sub>       | Image frequency Interference<br>$f_{\text{interference}} = f_{\text{Image}}$                          | Wanted signal=-79dBm, PER < 30.8% |  | -30 |  | dBc |
| C/I <sub>Image±1</sub> MHz | Adjacent channel to image frequency<br>$f_{\text{interference}} = f_{\text{Image}} \pm 1\text{MHz}$   | Wanted signal=-79dBm, PER < 30.8% |  | -34 |  | dBc |

**Table 15- Bluetooth Low Energy RF receiver characteristics at 1 Msym/s LE coded (S=8)**

| Symbol   | Parameter   | Test conditions                   | Min. | Typ. | Max. | Unit |
|--|---|-----------------------------------|------|------|------|------|
| RX <sub>SENS</sub>   | Sensitivity   | PER < 30.8%                       |      | -100 |      | dBm  |
| P <sub>SAT</sub>   | Saturation  | PER < 30.8%                       |      | 8    |      | dBm  |
| Z <sub>RF1</sub>   | Optimum RF source<br>(Impedance at RF1 pin)   | @ 2440 MHz                        |      | 40   |      | Ω    |
| RF selectivity with BLE equal modulation on interfering signal |   |                                   |      |      |      |      |
| C/I <sub>CO-channel</sub>                                      | Co-channel interference<br>$f_{\text{RX}} = f_{\text{interference}}$                                  | Wanted signal=-79dBm, PER < 30.8% |      | 1    |      | dBc  |
| C/I <sub>1</sub> MHz   | Adjacent Interference<br>$f_{\text{interference}} = f_{\text{RX}} \pm 1\text{MHz}$                    | Wanted signal=-79dBm, PER < 30.8% |      | -4   |      | dBc  |
| C/I <sub>2</sub> MHz   | Adjacent Interference<br>$f_{\text{interference}} = f_{\text{RX}} \pm 2\text{MHz}$                    | Wanted signal=-79dBm, PER < 30.8% |      | -39  |      | dBc  |
| C/I <sub>3</sub> MHz   | Adjacent Interference<br>$f_{\text{interference}} = f_{\text{RX}} \pm (3+n)\text{MHz}$ [n = 0,1,2...] | Wanted signal=-79dBm, PER < 30.8% |      | -53  |      | dBc  |
| C/I <sub>Image</sub>   | Image frequency Interference<br>$f_{\text{interference}} = f_{\text{Image}}$                          | Wanted signal=-79dBm, PER < 30.8% |      | -33  |      | dBc  |
| C/I <sub>Image±1</sub> MHz                                     | Adjacent channel to image frequency<br>$f_{\text{interference}} = f_{\text{Image}} \pm 1\text{MHz}$   | Wanted signal=-79dBm, PER < 30.8% |      | -32  |      | dBc  |

#### 4.3.6 Embedded reset and power control block characteristics

*Table 16- Embedded reset and power control block characteristics*

| Symbol                | Parameter                                 | Test conditions | Min. | Typ. | Max. | Unit |
|-----------------------|---|-----------------|------|------|------|------|
| T <sub>RSTTEMPO</sub> | Reset temporization after PDR is detected | VDD rising      |      |      | 500  | us   |
| VPDR                  | Power-down reset threshold                |                 |      | 1.63 |      | V    |
| VPVD0                 | PVD threshold 0                           | Falling edge    |      | 2.02 |      | V    |
| VPVD1                 | PVD threshold 1                           | Falling edge    |      | 2.17 |      |      |
| VPVD2                 | PVD threshold 2                           | Falling edge    |      | 2.33 |      |      |
| VPVD3                 | PVD threshold 3                           | Falling edge    |      | 2.49 |      |      |
| VPVD4                 | PVD threshold 4                           | Falling edge    |      | 2.61 |      |      |
| VPVD5                 | PVD threshold 5                           | Falling edge    |      | 2.78 |      |      |
| VPVD6                 | PVD threshold 6                           | Falling edge    |      | 2.87 |      |      |

#### 4.3.7 Wakeup time from low power modes

The wakeup times reported are the latency between the event and the execution of the instruction.

The device goes in Low-power mode after the WFI (Wait For Interrupt) instruction.

*Table 17- Low power mode wakeup timing*

| Symbol                  | Parameter                                  | Conditions                             | Typ. | Unit |
|-------------------------|--|--|------|------|
| T <sub>WUDEEPSTOP</sub> | Wakeup time from DEEPSTOP mode to RUN mode | Wakeup from GPIO. Boot in Flash memory | 110  | μs   |

#### 4.3.8 High speed crystal requirements

High speed external oscillator must be supplied with an external 32 MHz crystals that are specified for a 6 to 8pF loading capacitor. The BlueNRG-LP include internal programmable capacitances that can be used to tune the crystal frequency in order to compensate the PCB parasitic one.

These internal load capacitors, are made by a fixed one, in parallel with a 6-bit binary weighted capacitor bank. Thanks to low CL step size (LSB is typically 0.07pF), very fine Crystal tuning is possible. With typical XTAL sensitivity of -14ppm/pF, it is possible to trim a 32MHz crystal, with a resolution of 1ppm

The requirements for the external 32 MHz crystal are reported in the table below.

**Table 18- HSE crystal requirements**

| Symbol           | Parameter                                 | Conditions  | Min.             | Typ.             | Max.               | Unit |
|------------------|---|---|------------------|------------------|--------------------|------|
| f <sub>NOM</sub> | Oscillator frequency                      |   |                  | 32               |                    | MHz  |
| f <sub>TOL</sub> | Frequency tolerance                       | Includes initial accuracy, stability over temperature, aging and frequency pulling due to incorrect load capacitance. |                  |                  | ±50                | ppm  |
| ESR              | Equivalent series resistance              |   |                  |                  | 100                | Ω    |
| P <sub>D</sub>   | Drive level                               |   |                  |                  | 100                | μW   |
| CL               | HSE Crystal load capacitance              | 27 °C, typical corner<br>GMCONF = 3   | 5 <sup>(1)</sup> | 7 <sup>(2)</sup> | 9.2 <sup>(3)</sup> | pF   |
| CLstep           | HSE crystal load capacitance<br>LSB value | 27 °C,<br>GMCONF = 3<br>XOTUNE code between 32 and 33   |                  | 0.07             |                    | pF   |

- (1) XOTUNE programed at minimum code = 0
- (2) XOTUNE programed at center code = 32
- (3) XOTUNE programed at maximum code = 63

#### 4.3.9 Low speed crystal requirements

The low speed clock can be supplied with an external 32.768 kHz crystal oscillator. The requirements for the external 32.768 kHz crystal are reported in the table below.

**Table 19- LSE crystal requirements**

| Symbol           | Parameter                    | Conditions | Min. | Typ.   | Max. | Unit |
|------------------|------------------------------|------------|------|--------|------|------|
| f <sub>NOM</sub> | Nominal Frequency            |            |      | 32.768 |      | KHz  |
| ESR              | Equivalent series resistance |            |      |        | 90   | KΩ   |
| P <sub>D</sub>   | Drive level                  |            |      |        | 0.1  | μW   |

#### 4.3.10 High speed ring oscillator characteristics

**Table 20- HSI oscillator characteristics**

| Symbol           | Parameter         | Conditions | Min. | Typ. | Max. | Unit |
|------------------|-------------------|------------|------|------|------|------|
| f <sub>NOM</sub> | Nominal Frequency |            |      | 64   |      | MHz  |

#### 4.3.11 Low speed ring oscillator characteristics

**Table 21- LSI oscillator characteristics**

| Symbol                     | Parameter                        | Test conditions     | Min. | Typ. | Max. | Unit   |
|----------------------------|----------------------------------|---------------------|------|------|------|--------|
| $f_{NOM}$                  | Nominal Frequency                | Trimmed by software |      | 33   |      | KHz    |
| $\Delta F_{RO\_AT}/F_{RO}$ | Frequency spread vs. temperature | Standard deviation  |      | 140  |      | ppm/°C |

#### 4.3.12 PLL characteristics

Characteristics measured over recommended operating conditions unless otherwise specified.

**Table 22- PLL characteristics**

| Symbol                   | Parameter              | Conditions  | Min. | Typ. | Max. | Unit   |
|--------------------------|------------------------|---|------|------|------|--------|
| PN <sub>SYNTH</sub>      | RF carrier phase noise | At ±1MHz offset from carrier<br>(measured at 2.4GHz)        |      | -110 |      | dBc/Hz |
|                          |                        | At 2.4GHz ±3MHz offset from carrier<br>(measured at 2.4GHz) |      | -114 |      | dBc/Hz |
|                          |                        | At 2.4GHz ±6MHz offset from carrier<br>(measured at 2.4GHz) |      | -128 |      | dBc/Hz |
|                          |                        | At ±25MHz offset from carrier                               |      | -135 |      | dBc/Hz |
| LOCK <sub>TIMETX</sub>   | PLL lock time to TX    | With calibration @2.5 ppm                                   |      | 150  |      | μs     |
| LOCK <sub>TIMERX</sub>   | PLL lock time to RX    | With calibration @2.5 ppm                                   |      | 110  |      | μs     |
| LOCK <sub>TIMERXTX</sub> | PLL lock time RX to TX | Without calibration @2.5 ppm                                |      | 47   |      | μs     |
| LOCK <sub>TIMETXRX</sub> | PLL lock time TX to RX | Without calibration @2.5 ppm                                |      | 32   |      | μs     |

#### 4.3.13 Flash memory characteristics

The characteristics below are guaranteed by design.

**Table 23- Flash memory characteristics**

| Symbol            | Parameter                       | Test conditions | Typ. | Max. | Unit |
|-------------------|---------------------------------|-----------------|------|------|------|
| $t_{prog}$        | 32-bit programming time         |                 | 20   | 40   | μs   |
| $t_{prog\_burst}$ | 4x32-bit burst programming time |                 | 20   | 40   |      |

|             |                              |            |    |    |    |
|-------------|------------------------------|------------|----|----|----|
| $t_{ERASE}$ | Page (2 Kbyte) erase time    |            | 20 | 40 | ms |
| $t_{ME}$    | Mass erase time              |            | 20 | 40 |    |
| $I_{DD}$    | Average consumption from VDD | Write mode | 3  |    | mA |
|             |                              | Erase mode | 3  |    |    |
|             |                              | Mass erase | 5  |    |    |

**Table 24- Flash memory endurance and data retention**

| Symbol    | Parameter      | Test conditions         | Min. | Unit    |
|-----------|----------------|-------------------------|------|---------|
| $N_{END}$ | Endurance      | $T_A = -40$ to $+85$ °C | 10   | kcycles |
| $t_{RET}$ | Data retention | $T_A = 85$ °C           | 10   | Years   |

#### 4.3.14 Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts x (n + 1) supply pins). This test conforms to the ANSI/JEDEC standard.

**Table 25- ESD absolute maximum ratings**

| Symbol         | Parameter   | Conditions                              | Class | Max. <sup>(1)</sup> | Unit |
|----------------|---|---|-------|---------------------|------|
| $V_{ESD(HBM)}$ | Electrostatic discharge voltage (human body model)    | Conforming to ANSI/ESDA/JEDEC JS-001    | 2     | 2000                | V    |
| $V_{ESD(CBM)}$ | Electrostatic discharge voltage (charge device model) | Conforming to ANSI/ESDA/STM5.3.1 JS-002 | C2a   | 500                 |      |

(1) Guaranteed by characterization results.

#### 4.3.15 I/O port characteristics

Unless otherwise specified, the parameters given in the tables below are derived from tests performed under the conditions summarized in General operating conditions. All I/Os are designed as CMOS-compliant.

**Table 26- I/O static characteristics**

| Symbol   | Parameter                   | Conditions                                | Min.                | Typ | Max.                | Unit |
|----------|-----------------------------|---|---------------------|-----|---------------------|------|
| $V_{IL}$ | I/O input low level voltage | $1.62 \text{ V} < V_{DD} < 3.6 \text{ V}$ |                     |     | $0.3 \times V_{DD}$ | V    |
| $V_{IH}$ | I/O input low level voltage |   | $0.7 \times V_{DD}$ |     |                     |      |

|           |                       |   |    |    |           |            |
|-----------|-----------------------|---|----|----|-----------|------------|
| $I_{lkg}$ | Input leakage current | $0 \leq V_{IN} \leq \text{Max}(V_{DDx})^{(1)}$                              |    |    | $\pm 100$ | nA         |
|           |                       | $\text{Max}(V_{DDx})^{(1)} \leq V_{IN} \leq \text{Max}(V_{DDx})^{(1)} + 1V$ |    |    | 650       |            |
|           |                       | $\text{Max}(V_{DDx})^{(1)} + 1V < V_{IN} \leq 5.5 V$                        |    |    | 200       |            |
| $R_{PU}$  | Pull up resistor      | $V_{IN} = GND$  | 25 | 40 | 55        | K $\Omega$ |
| $R_{PD}$  | Pull down resistor    | $V_{IN} = GND$  | 25 | 40 | 55        |            |
| $C_{IO}$  | I/O pin capacitance   |   |    | 5  |           | pF         |

(1)  $\text{Max}(V_{DDx})$  is the maximum value among all the I/O supplies.

All I/Os are CMOS-compliant (no software configuration required).

The GPIOs (general purpose input/outputs) can sink or source up to  $\pm 8$  mA, and sink or source up to  $\pm 20$  mA (with a relaxed  $V_{OL} / V_{OH}$ ).

In the user application, the number of I/O pins that can drive current must be limited to respect the absolute maximum rating specified.

- The sum of the currents sourced by all the I/Os on VDD, plus the maximum consumption of the MCU sourced on VDD, cannot exceed the absolute maximum rating  $\Sigma I_{VDD}$ .
- The sum of the currents sunk by all the I/Os on VSS, plus the maximum consumption of the MCU sunk on GND, cannot exceed the absolute maximum rating  $\Sigma I_{V_{GND}}$ .

The characteristics below are guaranteed by characterization.

**Table 27- Output voltage characteristics**

| Symbol   | Parameter                                | Conditions  | Min. | Max.            | Unit |
|----------|--|---|------|-----------------|------|
| $V_{OL}$ | Output low level voltage for an I/O pin  | CMOS port <sup>(1)</sup>  IIO  = 8 mA $V_{DD} \geq 2.7 V$ |      | 0.4             | V    |
| $V_{OH}$ | Output high level voltage for an I/O pin |   |      | $V_{DD} - 0.4$  |      |
| $V_{OL}$ | Output low level voltage for an I/O pin  | IIO  = 20 mA $V_{DD} \geq 2.7 V$                          |      | 1.3             |      |
| $V_{OH}$ | Output high level voltage for an I/O pin |   |      | $V_{DD} - 1.3$  |      |
| $V_{OL}$ | Output low level voltage for an I/O pin  | IIO  = 4 mA $V_{DD} \geq 1.62 V$                          |      | 0.4             |      |
| $V_{OH}$ | Output high level voltage for an I/O pin |   |      | $V_{DD} - 0.45$ |      |

(1) CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.

#### 4.3.16 RSTN pin characteristics

The RSTN pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, RPU.

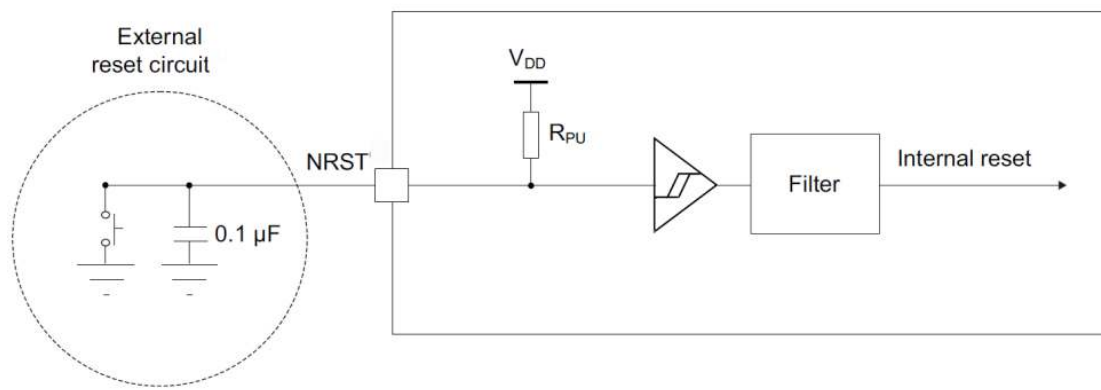
Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature and supply voltage conditions summarized in [Section 4.3.2 General operating conditions](#). The characteristics



below are guaranteed by design.

**Table 28- RSTN pin characteristics**

| Symbol          | Parameter                               | Conditions   | Min.                | Typ. | Max.                | Unit       |
|-----------------|---|--------------|---------------------|------|---------------------|------------|
| $V_{IL(RSTN)}$  | RSTN input low level voltage            |              |                     |      | $0.3 \times V_{DD}$ | V          |
| $V_{IH(RSTN)}$  | RSTN input high level voltage           |              | $0.7 \times V_{DD}$ |      |                     |            |
| $V_{hys(RSTN)}$ | RSTN Schmitt trigger voltage hysteresis |              |                     | 200  |                     | mV         |
| RPU             | Weak pull up equivalent resistor        | $V_{IN}=GND$ | 25                  | 40   | 55                  | K $\Omega$ |



**Figure 3 - Recommended RSTN pin protection**

Note:

The external reset circuit protects the device against parasitic resets.

The user must ensure that the level on the RSTN pin can go below the  $V_{IL(RSTN)}$  max. level specified in the table, otherwise the reset is not taken into account by the device. The external capacitor on RSTN must be placed as close as possible to the device.

#### 4.3.17 ADC characteristics

**Table 29- ADC characteristics (HSI must be set to PLL mode)**

| Symbol           | Parameter                                | Conditions               | Min. | Typ. | Max. | Unit |
|------------------|--|--------------------------|------|------|------|------|
| Ch_diff_num      | Number of channels for differential mode |                          |      |      | 4    |      |
| Ch_se_num        | Number of channels for single ended mode |                          |      |      | 8    |      |
| $IBAT_{ADCBIAS}$ | ADC biasing consumption at battery       | Biasing blocks turned on |      | 145  |      | mA   |

|                           |                                    |   |     |      |      |             |
|---------------------------|------------------------------------|---|-----|------|------|-------------|
| IBAT <sub>ADCACTIVE</sub> | ADC active consumption at battery  | ADC activated in differential mode  |     | 185  |      | mA          |
| VDDA                      | Analog supply voltage              |   | 1.2 |      | 1.32 | V           |
| R <sub>AIN</sub>          | Input impedance                    | In DC   |     | 250  |      | KΩ          |
| R <sub>in</sub>           | Internal access resistance         | VBOOST is enabled for VDD < 2.7 V   |     |      | 550  | Ω           |
| C <sub>in</sub>           | Input sampling capacitor           |   |     | 4    |      | pF          |
| T <sub>s</sub>            | Sampling period                    |   |     | 1    |      | μs          |
| T <sub>sw</sub>           | Sampling time                      |   |     | 125  |      | ns          |
| DR                        | Output data rate                   |   |     | 200  |      | k samples/s |
| FRMT <sub>output</sub>    | Output data format                 |   |     | 16   |      | bits        |
| T <sub>L</sub>            | Latency time                       | 200 kSps  |     | 5    |      | μs          |
| T <sub>STARTUP</sub>      | Start-up time                      | From ADC enable to conversion start                                       |     |      | 1    | μs          |
| DNL                       | Differential non-linearity         |   |     | ±0.7 |      | LSB         |
| INL                       | Integral non-linearity             |   |     | ±1   |      | LSB         |
| SNR Diff                  | Signal to noise ratio              | Differential input @1 kHz, -1 dBFS  |     | 72   |      | dB          |
| STHD Diff                 | Signal to THD ratio (10 harmonics) | Differential input @1 kHz, -1 dBFS  |     | 80   |      | dB          |
| ENOB Diff                 | Effective number of bits           | Differential input @1 kHz, -1 dBFS  |     | 11.5 |      | bits        |
| SNR SE                    | Signal to noise ratio              | Single ended @1 kHz, -1 dBFS  |     | 70   |      | dB          |
| STHD SE                   | Signal to THD ratio (10 harmonics) | Single ended @1 kHz, -1 dBFS  |     | 75   |      | dB          |
| ENOB SE                   | Effective number of bits           | Single ended @1 kHz, -1 dBFS  |     | 11   |      | bits        |
|                           | ADC_ERR_1V7                        | Absolute error when used for battery measurement at 1.7V, 2.4V, 3.0V,3.6V |     | 13   |      | mV          |
|                           | ADC_ERR_2V4                        |   |     | 0    |      |             |
|                           | ADC_ERR_3V0                        |   |     | -9   |      |             |
|                           | ADC_ERR_3V6                        |   |     | -22  |      |             |

#### 4.3.18 Temperature sensor characteristics

**Table 30- Temperature sensor characteristics**

| Symbol             | Parameter                       | Min. | Typ. | Max. | Unit   |
|--------------------|---------------------------------|------|------|------|--------|
| T <sub>FERR</sub>  | Error in temperature            |      | ±4   |      | °C     |
| T <sub>SLOPE</sub> | Average temperature coefficient |      | 8    |      | LSB/°C |

|              |                                      |  |      |  |         |
|--------------|--------------------------------------|--|------|--|---------|
| $T_{ICC}$    | Current consumption                  |  | 415  |  | $\mu A$ |
| $T_{TS-OUT}$ | Output voltage level at 30°C (+-5°C) |  | 2533 |  | V       |

#### 4.3.19 Timer characteristics

The characteristics below are guaranteed by design.

**Table 31- TIM1 characteristics**

| Symbol           | Parameter                   | Test conditions                | Min.     | Typ.   | Max.  | Unit    |
|------------------|-----------------------------|--------------------------------|----------|--------|-------|---------|
| $t_{res(TIM)}$   | Timer resolution time       | $f_{TIMxCLK} = 64 \text{ MHz}$ |          | 15.625 |       | ns      |
| $R_{esTIM}$      | Timer resolution            |                                |          | 16     |       | bit     |
| $t_{COUNTER}$    | 16-bit counter clock period | $f_{TIMxCLK} = 64 \text{ MHz}$ | 0.015625 |        | 1024  | $\mu s$ |
| $t_{MAX\_COUNT}$ | Maximum possible count time | $f_{TIMxCLK} = 64$             |          |        | 67.10 | s       |

**Table 32- IWDG min./max. timeout period at 32 kHz (LSE)**

| Prescaler divider | PR[2:0] bits | Min timeout RL[11:0] = 0x000 | Max timeout RL[11:0] = 0xFFF | Unit |
|-------------------|--------------|------------------------------|------------------------------|------|
| /4                | 0            | 0.125                        | 512                          | ms   |
| /8                | 1            | 0.250                        | 1024                         |      |
| /16               | 2            | 0.500                        | 2048                         |      |
| /32               | 3            | 1.0                          | 4096                         |      |
| /64               | 4            | 2.0                          | 8192                         |      |
| /128              | 5            | 4.0                          | 16384                        |      |
| /256              | 6 or 7       | 8.0                          | 32768                        |      |

#### 4.3.20 I<sup>2</sup>C interface characteristics

The I<sup>2</sup>C interface meets the timings requirements of the I<sup>2</sup>C-bus specification and user manual rev.03 for:

- Standard-mode (Sm): bit rate up to 100 kbit/s
- Fast-mode (Fm): bit rate up to 400 kbit/s
- Fast-mode Plus (Fm+): bit rate up to 1 Mbit/s.

The SDA and SCL I/O requirements are met with the following restriction: the SDA and SCL I/O pins are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and VDD is disabled, but is still present. The 20 mA output drive requirement in Fast-mode Plus is supported partially.

This limits the maximum load  $C_{load}$  supported in Fast-mode Plus, given by these formulas:

- $t_r(\text{SDA/SCL}) = 0.8473 \times R_p \times C_{\text{load}}$
- $R_p(\text{min}) = [V_{\text{DD}} - V_{\text{OL}}(\text{max})] / I_{\text{OL}}(\text{max})$

where  $R_p$  is the I<sup>2</sup>C lines pull-up.

All I<sup>2</sup>C SDA and SCL I/Os embed an analog filter.

The characteristics below are guaranteed by design.

**Table 33- I<sup>2</sup>C analog filter characteristics**

| Symbol | Parameter  | Min. | Max. | Unit |
|--------|--|------|------|------|
| tAF    | Maximum pulse width of spikes that are suppressed by the analog filter | 50   | 110  | ns   |

#### 4.3.21 SPI characteristics

The parameters for SPI are derived from tests performed according to fPCLKx frequency and supply voltage conditions.

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: 0.5 x VDD

The characteristics below are guaranteed by design.

**Table 34- SPI characteristics**

| Symbol                | Parameter                | Conditions  | Min.                        | Typ.                  | Max.                     | Unit |
|-----------------------|--------------------------|-------------|-----------------------------|-----------------------|--------------------------|------|
| f <sub>SCK</sub>      | SPI clock frequency      | Master mode |                             | -                     | 32                       | MHz  |
|                       |                          | Slave mode  |                             | -                     | 32 <sup>(1)</sup>        |      |
| t <sub>su</sub> (NSS) | NSS setup time           |             | 4 / f <sub>PCLK</sub>       | -                     | -                        | -    |
| t <sub>h</sub> (NSS)  | NSS hold time            |             | 2 / f <sub>PCLK</sub>       | -                     | -                        | -    |
| tw(SCKH)              | SCK high and low time    | Master mode | 1 / f <sub>PCLK</sub> - 1.5 | 1 / f <sub>PCLK</sub> | 1 / f <sub>PCLK</sub> +1 | ns   |
| tw(SCKL)              |                          |             | 1 / f <sub>PCLK</sub> - 1.5 | 1 / f <sub>PCLK</sub> | 1 / f <sub>PCLK</sub> +1 |      |
| t <sub>su</sub> (MI)  | Data input setup time    | Master mode | 1                           | -                     | -                        |      |
| t <sub>su</sub> (SI)  | Data input setup time    | Slave mode  | 1                           | -                     | -                        |      |
| t <sub>h</sub> (MI)   | Data input hold time     | Master mode | 3                           | -                     | -                        |      |
| t <sub>h</sub> (SI)   | Data input hold time     | Slave mode  | 1                           | -                     | -                        |      |
| t <sub>a</sub> (SO)   | Data output access time  | Slave mode  | 5                           | -                     | 40                       |      |
| t <sub>dis</sub> (SO) | Data output disable time | Slave mode  | 5                           | -                     | 38                       |      |
| t <sub>v</sub> (SO)   | Data output valid time   | Master mode | -                           | 2                     | 8                        |      |

|           |                        |             |   |    |    |    |
|-----------|------------------------|-------------|---|----|----|----|
|           |                        | Slave mode  | - | 12 | 39 |    |
| $t_h(SO)$ | Data output valid time | Master mode | 2 |    | -  | ns |
|           |                        | Slave mode  | 4 |    | -  |    |

- (1) The maximum frequency in slave transmitter mode is determined by the sum of  $t_v(SO)$  and  $t_{su}(MI)$ , which has to fit SCK low or high phase preceding the SCK sampling edge. This value can be achieved when the SPI communicates with a master having  $t_{su}(MI) = 0$  while  $duty(SCK) = 50\%$ .

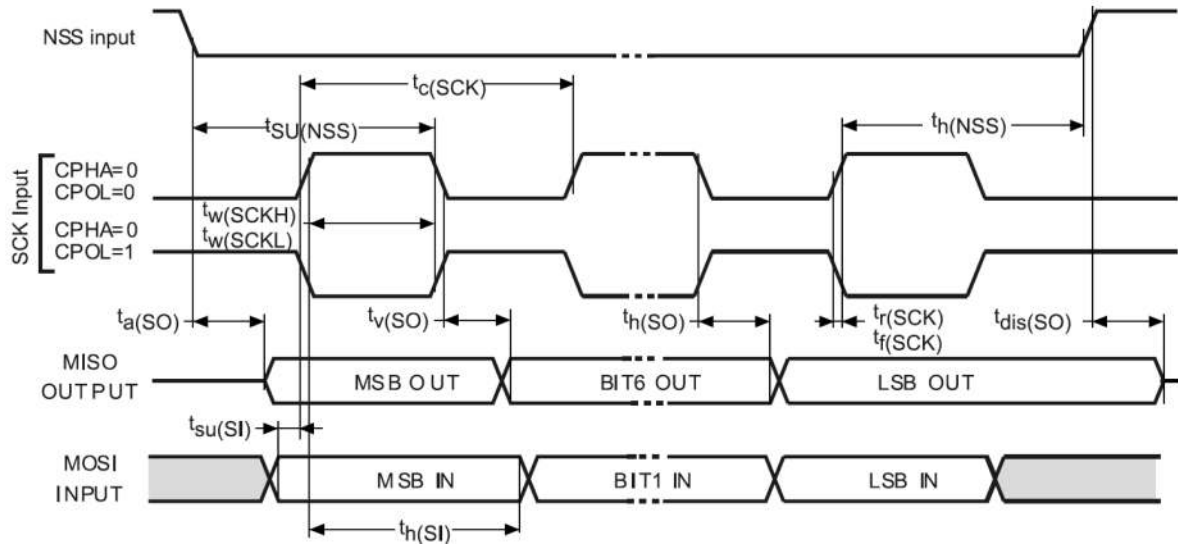


Figure 4 - SPI timing diagram - slave mode and CPHA = 0

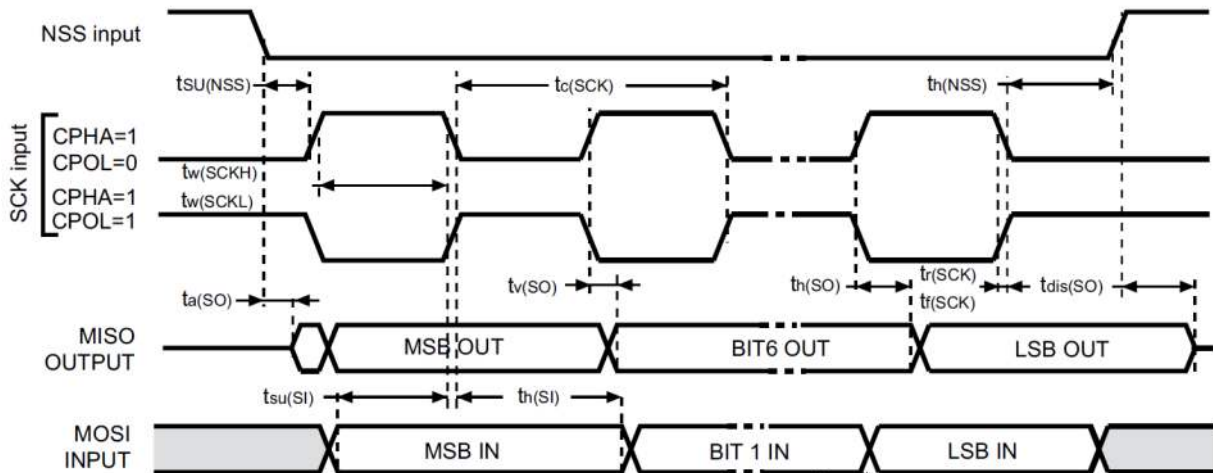


Figure 5 - SPI timing diagram - slave mode and CPHA = 1

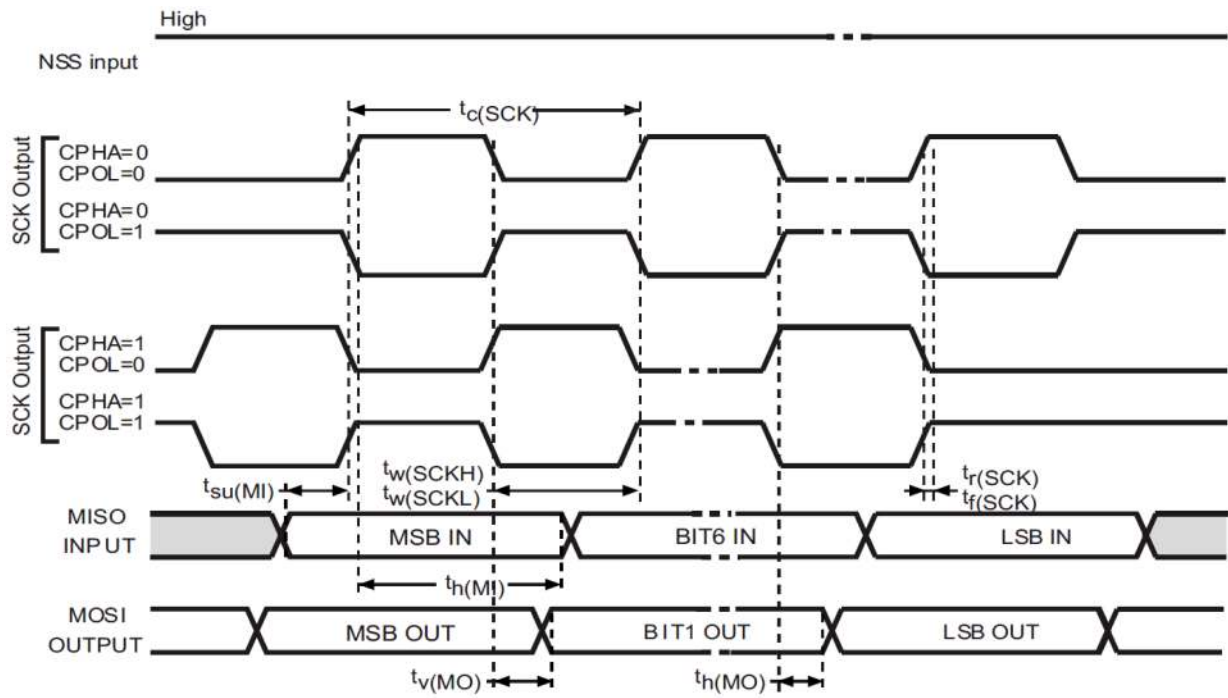


Figure 6 - SPI timing diagram - master mode

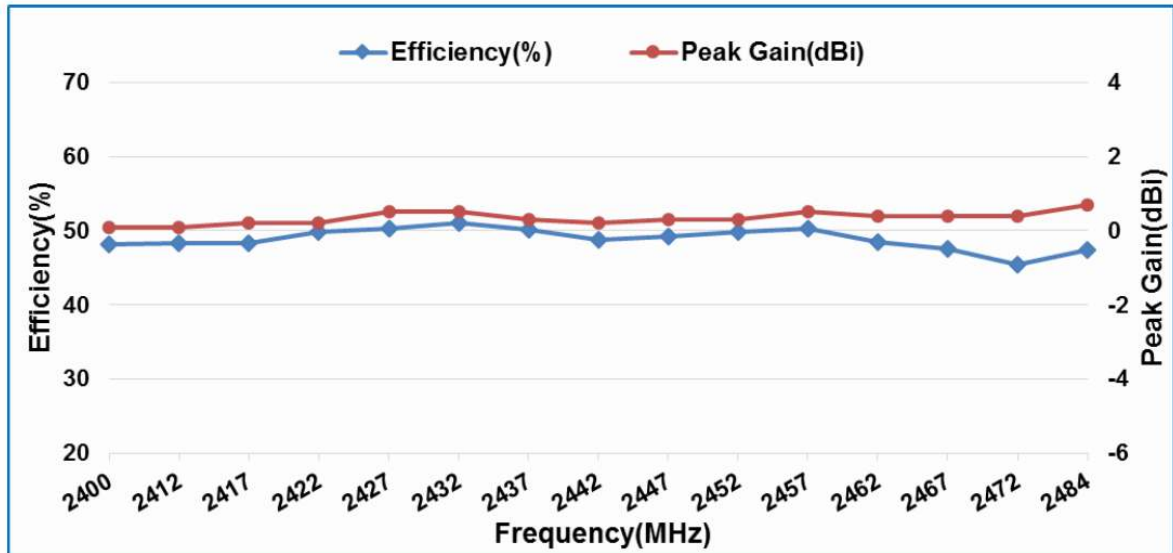
#### 4.3.22 Typical characteristics

There are some typical performance plots measured on the BlueNRG-355AC device in the BlueNRG-LP data sheet, and the plots relevant for the WB2072-00 module. Please visit STMicroelectronics web site

<https://www.st.com/resource/en/datasheet/bluenrg-lp.pdf>

### 4.4. Chip Antenna Characteristics

Measured on the Jorjin WB2072E00A EM board with  $T_A = 25^\circ\text{C}$



| Frequency (MHz) | 2400 | 2412 | 2417 | 2422 | 2427 | 2432 | 2437 | 2442 | 2447 | 2452 | 2457 | 2462 | 2467 | 2472 | 2484 |
|-----------------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|
| Efficiency (dB) | -3.2 | -3.2 | -3.2 | -3.0 | -3.0 | -2.9 | -3.0 | -3.1 | -3.1 | -3.0 | -3.0 | -3.2 | -3.2 | -3.4 | -3.2 |
| Efficiency (%)  | 48.2 | 48.3 | 48.3 | 49.9 | 50.3 | 51.0 | 50.1 | 48.8 | 49.3 | 49.9 | 50.3 | 48.4 | 47.5 | 45.5 | 47.4 |
| Peak Gain (dBi) | 0.1  | 0.1  | 0.2  | 0.2  | 0.5  | 0.5  | 0.3  | 0.2  | 0.3  | 0.3  | 0.5  | 0.4  | 0.4  | 0.4  | 0.7  |

Figure 7 – Efficiency vs. Frequency

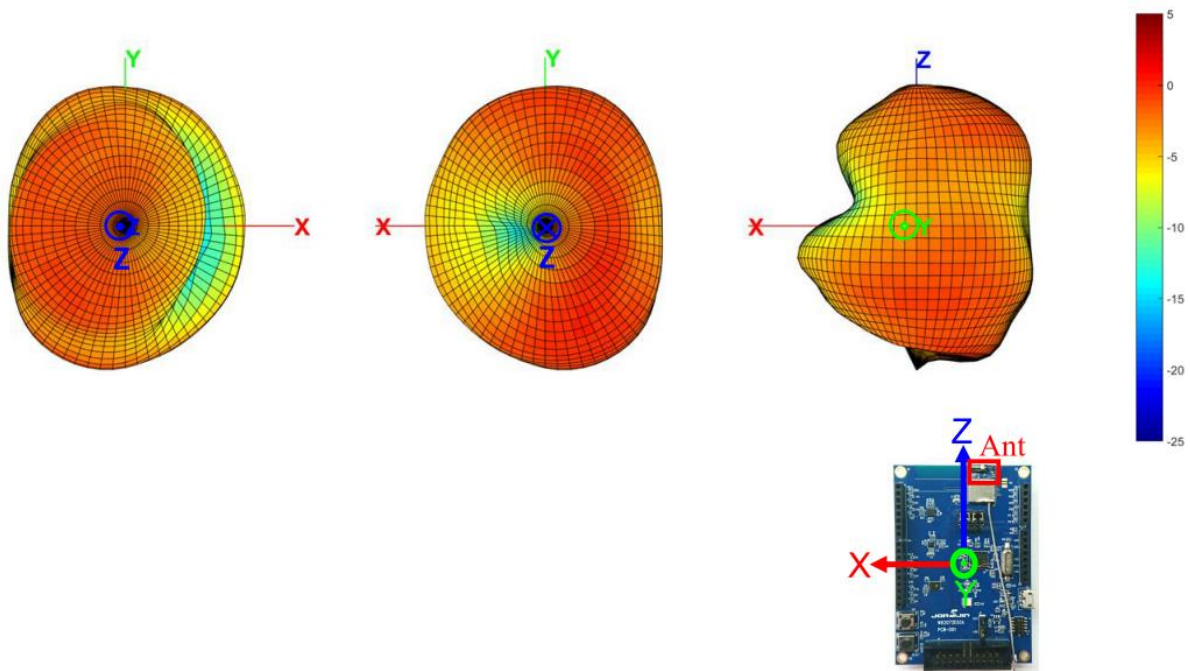


Figure 8 – 3D Pattern

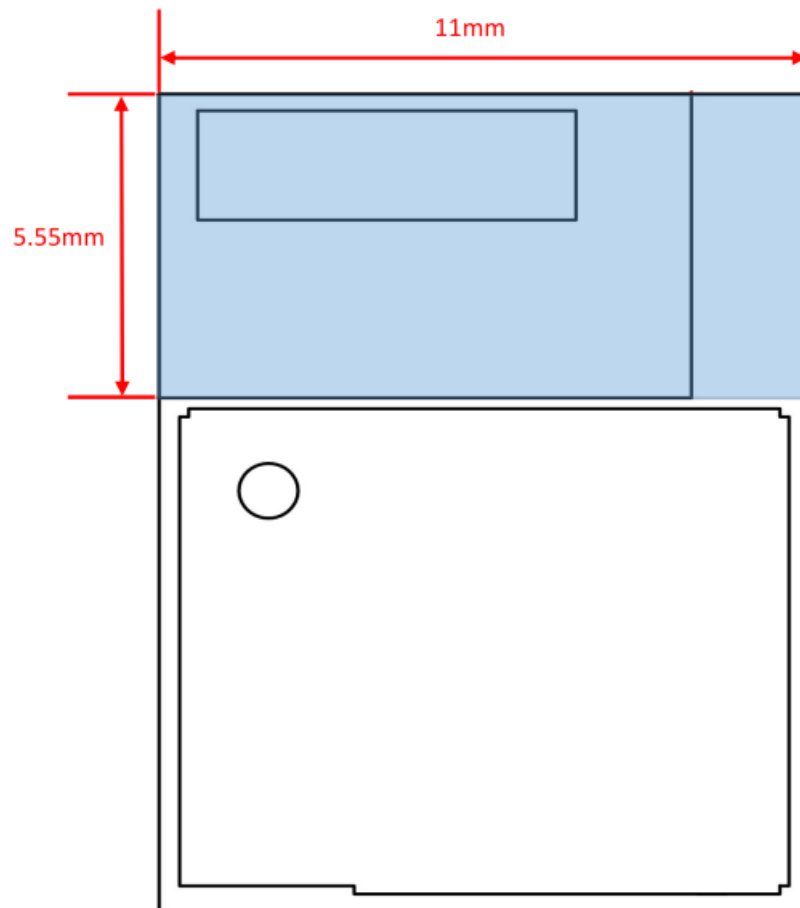
## 5. DESIGN RECOMMENDATIONS

### 5.1. Module Layout Recommendations

Follow these module layout recommendations:

- Antenna

For a module with on board chip antenna, to eliminate the influence from other components or ground, recommended that the module is placed in the corner of main PCB, and define a clearance area around the antenna, where no grounding or signal trace are contained. The clearance area applies to all layers of the main PCB. The recommended dimensions of the main PCB keep out area are shown in bellow.

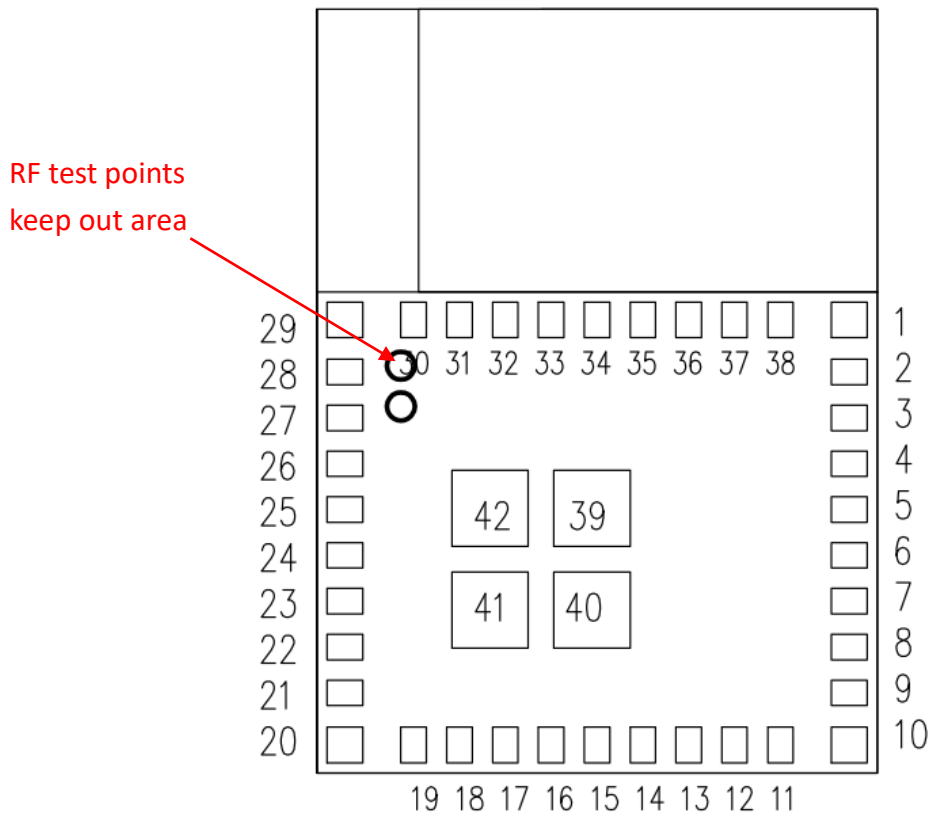


*Figure 9 –PCB keep out area*



- RF test point

There are RF test points in the bottom side of this module. It is only for module production used. Do not connect any signal to these test points (leave no connection) in the module. And do not design test point in the main board. Please reserve a clearance in the top-side copper plane underneath the RF test pads. Do not route any signal or place via in this keep out area.



**Figure 10** –RF Point

## 5.2. Reference Schematic

### BLE 5.1 Module

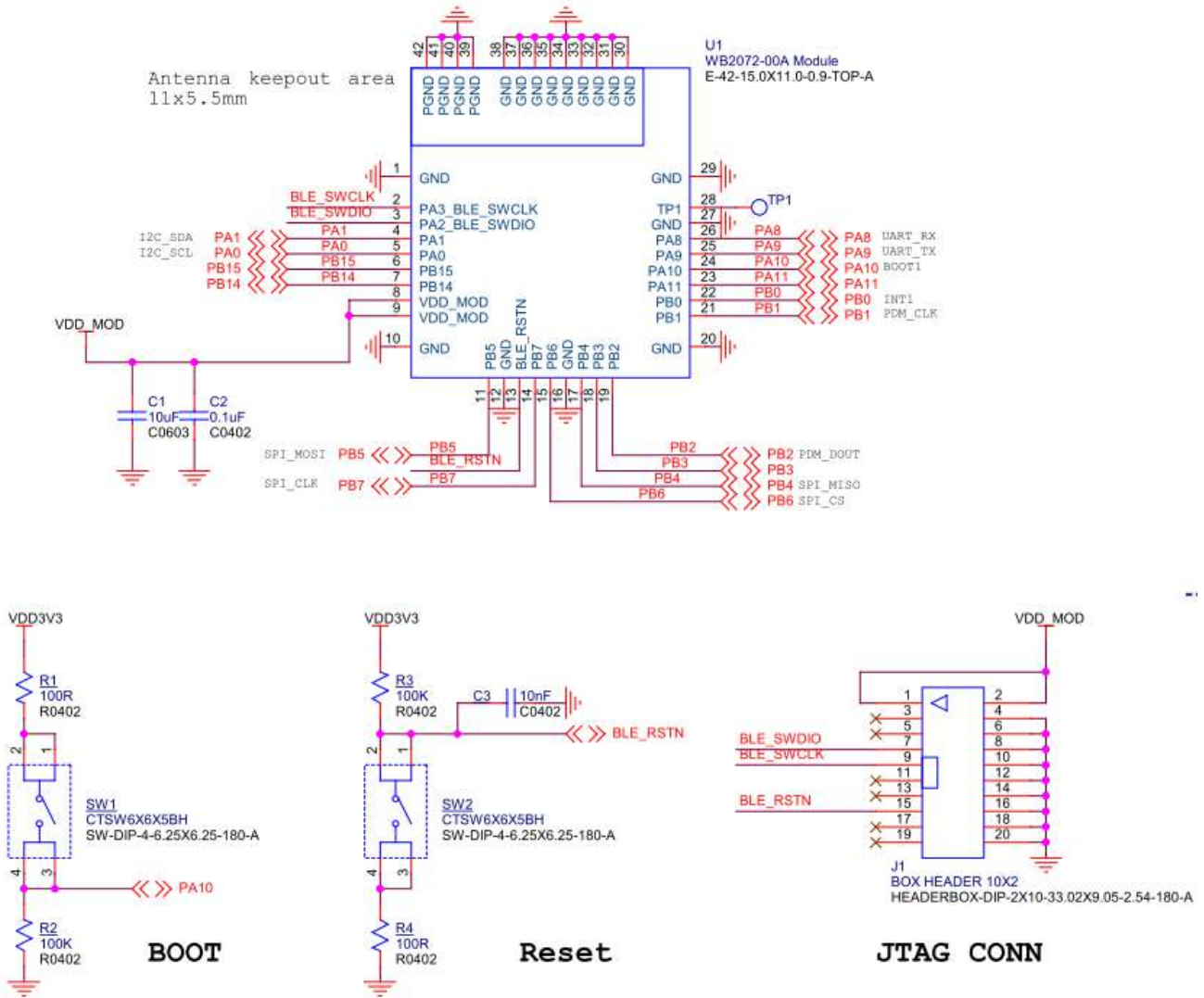
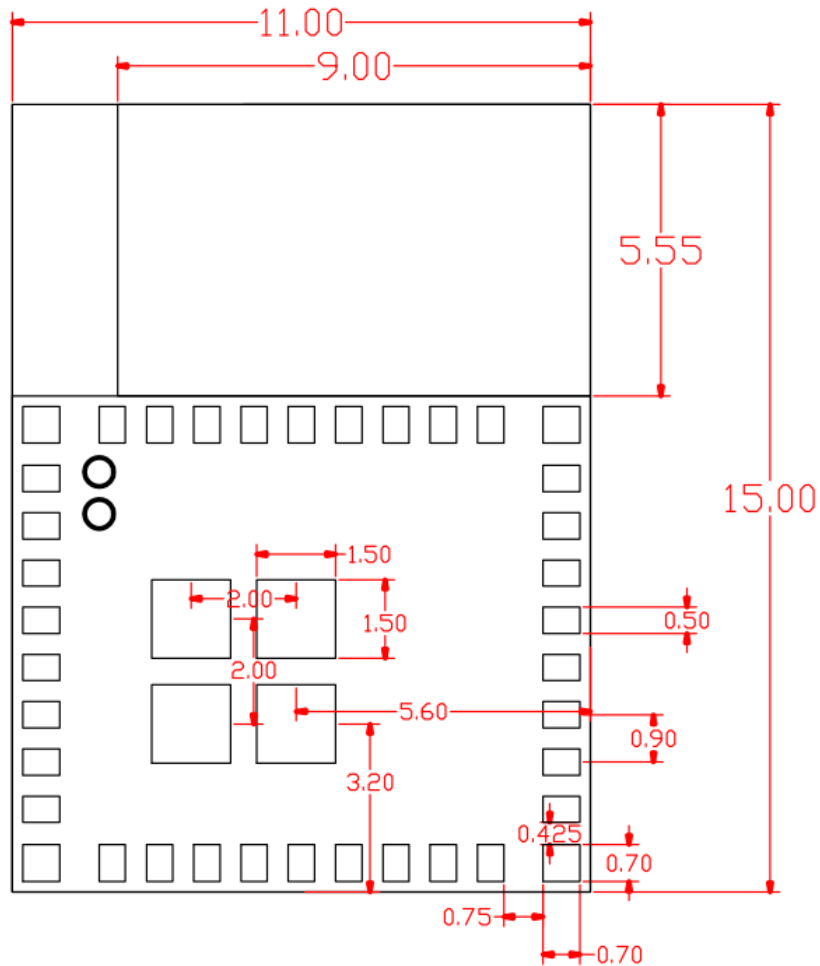


Figure 11 – Reference Schematic

## 6. PACKAGE INFORMATION

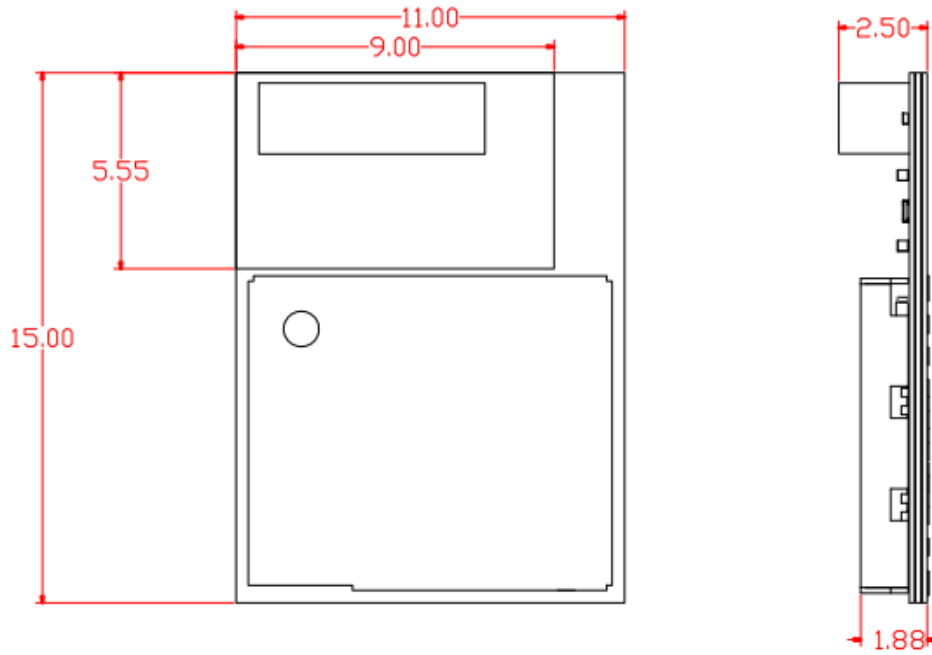
### 6.1. Module Mechanical Outline



**Figure 12** – Module Mechanical Outline (BOTTOM View)

Note:

- 1> Pad tolerance as  $\pm 30\mu\text{m}$
- 2> Unit: mm



**Figure 13 – Module Mechanical Outline (TOP and Side View)**

Note:

Unit: mm

## 6.2. Ordering Information

| Order Number | Package |
|--------------|---------|
| WB2072-00    | LGA-42  |

### 6.3. Package Marking

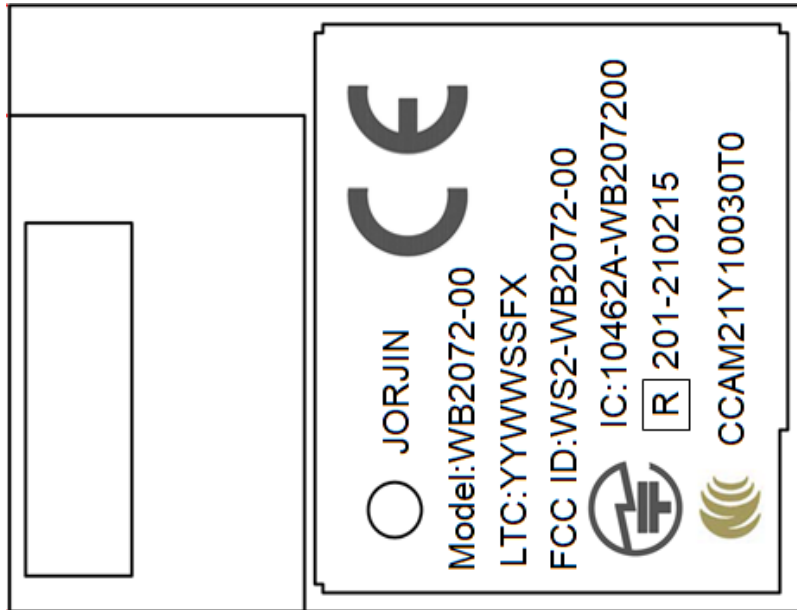





Figure 14 –shielding case information

| Marking   | Description  |
|---|--|
| JORJIN  | Brand name   |
| WB2072-00   | Model name   |
| YYWWSSFX  | Lot Trace Code: YYWWSSFX<br>YY= Digit of the year, ex: 2017=17<br>WW= Week (01~52)<br>SS= Serial number from 01~98 match to MFG’s lot number, or 99 to repair control code<br>F= Reverse for internal use<br>X = Module version from A to Z. This is A version |
| WS2-WB2072-00   | FCC ID   |
| 10462A-WB207200   | Canada IC ID   |
|  | TELEC compliance mark, and ID  |
|  | CE compliance mark   |
|  | NCC compliance mark, and ID  |

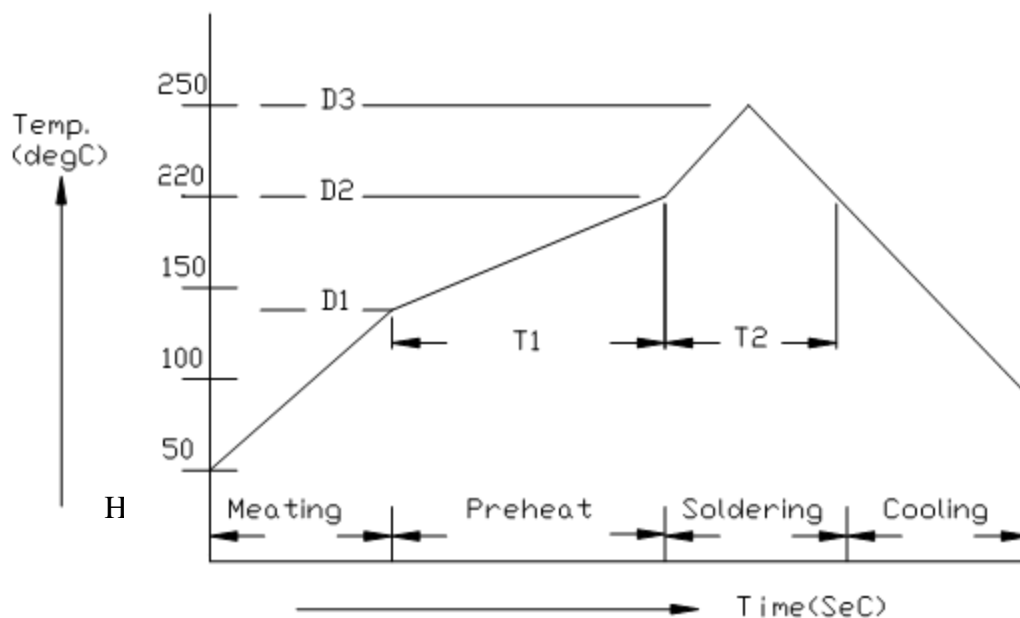
## 7. SMT AND BAKING RECOMMENDATION

### 7.1. Baking Recommendation

- Baking condition :
  - Follow MSL Level 4 to do baking process.
  - After bag is opened, devices that will be subjected to reflow solder or other high temperature process must be
    - a) Mounted within 72 hours of factory conditions <30°C/60% RH, or
    - b) Stored at <10% RH.
  - Devices require bake, before mounting, if Humidity Indicator Card reads >10%
  - If baking is required, Devices may be baked for 8 hrs. at 125 °C.

### 7.2. SMT Recommendation

- Recommended Reflow profile :



**Figure 15 – Reflow profile**

| No. | Item       | Temperature (°C)  | Time (sec)    |
|-----|------------|-------------------|---------------|
| 1   | Pre-heat   | D1: 140 ~ D2: 200 | T1: 80 ~ 120  |
| 2   | Soldering  | D2: = 220         | T2: 60 +/- 10 |
| 3   | Peak-Temp. | D3: 250 °C max    |               |

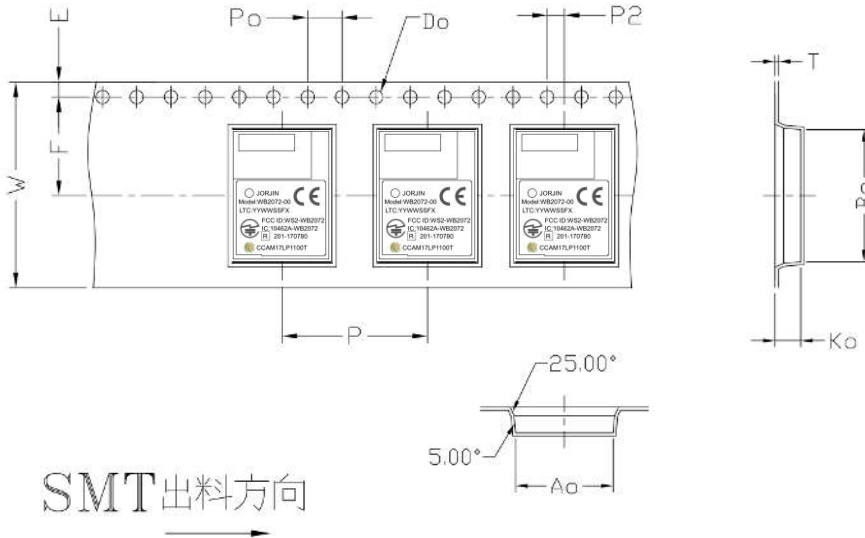
Note: (1) Reflow soldering is recommended two times maximum.

(2) Add Nitrogen while Reflow process : SMT solder ability will be better.

- **Stencil thickness** : 0.1~ 0.13 mm (Recommended)
- **Soldering paste (without Pb)** : Recommended SENJU N705-GRN3360-K2-V can get better soldering effects.

## 8. TAPE REEL INFORMATION

### 8.1. Cover / Carrier Tape Dimension



| ITEM           | DIM                                     | ALTERNATE |
|----------------|---|-----------|
| W              | 24.00 <sup>+0.30</sup> <sub>-0.30</sub> |           |
| E              | 1.75 <sup>+0.10</sup> <sub>-0.10</sub>  |           |
| F              | 11.50 <sup>+0.10</sup> <sub>-0.10</sub> |           |
| P              | 16.00 <sup>+0.10</sup> <sub>-0.10</sub> |           |
| P <sub>0</sub> | 4.00 <sup>+0.10</sup> <sub>-0.10</sub>  |           |
| P <sub>2</sub> | 2.00 <sup>+0.10</sup> <sub>-0.10</sub>  |           |
| Do             | ∅1.50 <sup>+0.10</sup> <sub>-0.00</sub> |           |
| T              | 0.35 <sup>+0.05</sup> <sub>-0.05</sub>  |           |
| A <sub>0</sub> | 11.40 <sup>+0.10</sup> <sub>-0.10</sub> |           |
| B <sub>0</sub> | 15.40 <sup>+0.10</sup> <sub>-0.10</sub> |           |
| K <sub>0</sub> | 3.00 <sup>+0.10</sup> <sub>-0.10</sub>  |           |

| Packing Qty    | Dry Bag             | Inner Box              | Outer Box                |
|----------------|---------------------|------------------------|--------------------------|
| 1200 EA / Reel | 1 Reel<br>(1200 EA) | 1 Dry Bag<br>(1200 EA) | 4 Inner Box<br>(4800 EA) |

Inner Box Size : 352mm x 352mm x 56mm

Outer Box Size : 354mm x 362mm x 250mm



## 9. REGULATORY INFORMATION

This section outlines the regulatory information for the following countries:

- United States
- Canada
- Japan
- Europe
- Taiwan

### 9.1. United States

#### Federal Communications Commission Statement

15.21. You are cautioned that changes or modifications not expressly approved by the part responsible for compliance could void the user's authority to operate the equipment.

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

- (1) This device may not cause harmful interference and
- (2) This device must accept any interference received, including interference that may cause undesired operation of the device.

#### FCC RF Radiation Exposure Statement:

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. End users must follow the specific operating instructions for satisfying RF exposure limits. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

#### End Product Labeling:

This module is designed to comply with the FCC statement, FCC ID: **WS2-WB2072-00**. The host system using this module must display a visible label indicating the following text:

"Contains FCC ID: **WS2-WB2072-00**"

#### Manual Information to the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module.

The end user manual shall include all required regulatory information/warning as shown in this manual.

## 9.2. Canada

### **This device complies with Industry Canada's licence-exempt RSS standard(s).**

Operation is subject to the following two conditions:

- (1) this device may not cause interference, and
- (2) this device must accept any interference, including interference that may cause undesired operation of the device.

### **Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence**

L'exploitation est autorisée aux deux conditions suivantes:

- (1) l'appareil ne doit pas produire de brouillage, et
- (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

### **RF Radiation Exposure Statement:**

This equipment complies with IC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 10mm between the radiator & your body. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

### **Déclaration d'exposition aux radiations:**

Cet équipement est conforme aux limites d'exposition aux rayonnements IC établies pour un environnement non contrôlé. Cet équipement doit être installé et utilisé avec un minimum de 10mm de distance entre la source de rayonnement et votre corps.

### **End Product Labeling:**

This module is designed to comply with the IC statement, IC: **10462A-WB207200**. The host system using this module must display a visible label indicating the following text:

"Contains IC: **10462A-WB207200**"

### **Manual Information to the End User**

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this

module.

The end user manual shall include all required regulatory information/warning as shown in this manual.

### 9.3. Europe

Hereby, Jorjin Technologies Inc. declares that the radio equipment type RF module is in compliance with Directive 2014/53/EU

The full text of the EU declaration of conformity is available at the following internet address:  
<https://www.jorjin.com/downloads/#474-wb2072-00>

The compliance has been verified in the operating frequency band of 2400 MHz to 2483.5 MHz. Developers and integrators that incorporate the WB2072-00 RF Module in any end products are responsible for obtaining applicable regulatory approvals for such end product.

The WB2072-00 has been tested in the 2400-GHz to 2483.5-GHz ISM frequency band at 3.3 V with a maximum peak power of 6.46 dBm EIRP across the temperature range  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  and tolerance.

#### Labeling and User Information Requirements

As a result of the conformity assessment procedure described in Annex III of the Directive 2014/53/EC, the end-customer equipment should be labeled as follows:



### 9.4. Japan

The WB2072-00 is certified as a module with type certification number 201-210215. End products that integrate this module do not need additional MIC Japan certification for the end product.

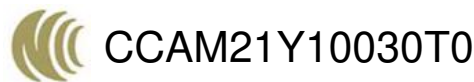
End product can display the certification label of the embedded module.



## 9.5. Taiwan

The WB2072-00 is certified as a module with type certification number CCAM21Y10030T0. End products that integrate this module do not need additional NCC Taiwan certification for the end product.

End product can display the certification label of the embedded module.



The user's manual should contain following warning (for RF device) in traditional Chinese:

注意


本產品符合低功率電波輻射性電機管理辦法：

LP0002 低功率射頻器材技術規範\_章節 3.8.2

取得審驗證明之低功率射頻器材，非經核准，公司、商號或使用者均不得擅自變更頻率、加大功率或變更原設計之特性及功能。

低功率射頻器材之使用不得影響飛航安全及干擾合法通信；經發現有干擾現象時，應立即停用，並改善至無干擾時方得繼續使用。

前述合法通信，指依電信管理法規定作業之無線電通信。低功率射頻器材須忍受合法通信或工業、科學及醫療用電波輻射性電機設備之干擾。

系統廠商應於平台上標示「本產品內含射頻模組：XXXXXXXXXXXXXXXXXX」字樣

## 10. HISTORY CHANGE

| Revision | Date       | Description   |
|----------|------------|---|
| R01      | 2020.12.16 | Official version released   |
| R02      | 2021.04.22 | 1. Add 9. REGULATORY INFORMATION<br>2. Update warning of NCC<br>3. Add MIC and NCC ID |
| R03      | 2021.05.04 | Modify Canada IC ID   |