REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Correct title to read ANALOG TO DIGITAL. Change conditions for timing tests, table I. Change figure 3. Editorial changes throughout.	90-01-24	M. A. Frye
B	Changes in accordance with NOR 5962-R231-94.	94-08-12	M. A. Frye
C	Update drawing to current requirements. Editorial changes throughout. - gap	01-08-30	Raymond Monnin
D	Redrawn. Paragraphs updated to MIL-PRF-38535 requirements. -drw	13-01-25	Charles F. Saffle

THE ORIGINAL FIRST SHEET OF THIS DRAWING HAS BEEN REPLACED.

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REV STATUS	REV	D	D	D	D	D	D	D	D	D	D	D	D	D	
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	

PMIC N/A

PREPARED BY
Joseph A. Kerby

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
http://www.landandmaritime.dla.mil

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
Charles E. Besore

APPROVED BY
Michael A. Frye

DRAWING APPROVAL DATE
87-08-18

REVISION LEVEL
D

MICROCIRCUIT, LINEAR, HIGH SPEED, ANALOG TO DIGITAL CONVERTER, MONOLITHIC SILICON

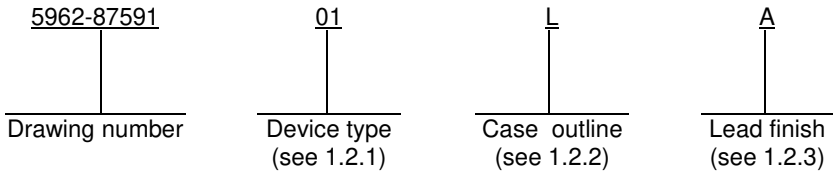
SIZE	CAGE CODE	
A	**67268**	**5962-87591**

SHEET 1 OF 13

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:



1.2.1 Device types. The device types identify the circuit function as follows:

Device type	Generic number	Circuit function
01	AD7572	12.5-microsecond, 11-bit linearity, 12-bit resolution CMOS A/D converter with 45 ppm/°C reference.
02	AD7572	12.5-microsecond, 11-bit linearity, 12-bit resolution CMOS A/D converter with 25 ppm/°C reference.
03	AD7572	12.5-microsecond, 12-bit linearity, 12-bit resolution CMOS A/D converter with 25 ppm/°C reference.
04	AD7572	5-microsecond, 11-bit linearity, 12-bit resolution CMOS A/D converter with 45 ppm/°C reference.
05	AD7572	5-microsecond, 11-bit linearity, 12-bit resolution CMOS A/D converter with 25 ppm/°C reference.
06	AD7572	5-microsecond, 12-bit linearity, 12-bit resolution CMOS A/D converter with 25 ppm/°C reference.

1.2.2 Case outlines. The case outlines are as designated in MIL-STD-1835 as follows:

Outline letter	Descriptive designator	Terminals	Package style
L	GDIP3-T24 or CDIP4-T24	24	Dual-in-line
3	CQCC1-N28	28	Leadless square chip carrier

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings. (T_A = +25°C, unless otherwise noted).

V_{DD} to DGND	-0.3 V dc to +7 V dc
V_{SS} to DGND	+0.3 V dc to -17 V dc
AGND to DGND	-0.3 V dc, V_{DD} +0.3 V dc
A_{IN} to AGND	-15 V dc to +15 V dc
Digital input voltage to DGND	-0.3 V dc, V_{DD} +0.3 V dc
Digital output voltage to DGND	-0.3 V dc, V_{DD} +0.3 V dc
Storage temperature range	-65°C to +150°C
Power dissipation ≤ +75°C	1,000 mW 1/
Thermal resistance (θ_{JC})	See MIL-STD-1835
Junction temperature (T_J)	+175°C

1.4 Recommended operating conditions.

Operating voltage range:	
Positive supply (V_{DD})	+4.75 V dc to +5.25 V dc
Negative supply (V_{SS})	-14.25 V dc to -15.75 V dc
Clock frequency (f_{CLK})	1.0 MHz for device types 01, 02, and 03 2.5 MHz for device types 04, 05, and 06
Analog input voltage range (A_{IN}) (specifications apply to slow memory mode)	0 to +5.0 V dc
Ambient operating temperature range (T_A)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://assist.dla.mil/quicksearch/ or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

1/ Derate power dissipation above +75°C by 10 mW/°C.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Load circuits. The load circuits shall be as specified on figures 2 and 3.

3.2.4 Timing diagrams. The timing diagrams shall be as specified on figures 4, 5, 6, and 7.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DLA Land and Maritime -VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DLA Land and Maritime -VA shall be required for any change that affects this drawing.

3.9 Verification and review. DLA Land and Maritime, DLA Land and Maritime's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ unless otherwise specified	Device types	Group A subgroups	Limits		Unit
					Min	Max	
Integral linearity error	LE	V_{DD} = 5 V, V_{SS} = -15 V	01, 02,	1		±1	LSB
			04, 05	2, 3		±1	
			03, 06	2, 3		±3/4	
			03, 06	12		±1/2	
Differential linearity error	DLE	V_{DD} = 5 V, V_{SS} = -15 V	All	1, 2, 3		±1	
Offset error	V_{OS}	V_{DD} = 5 V, V_{SS} = -15 V	All	1		±4	LSB
			01, 04	2, 3		±6	
			02, 05	2, 3		±5	
			03, 06	2, 3		±4	
			02, 03, 05, 06	12		±3	
Full scale error including internal voltage reference error, (Ideal last code transition = FS-3/2LSB's)	AE	V_{DD} = 5 V	All	1		±15	LSB
		V_{SS} = -15 V, Full scale = 5 V	02, 03, 05, 06	12		±10	
Full scale temperature coefficient, including internal voltage reference drift	dAE/dT	V_{DD} = 5 V	01, 04	2, 3		45	ppm/°C
		V_{SS} = -15 V	02, 03, 05, 06			25	
Analog input current	I_{IN}	A_{IN} = 5 V	All	1, 2, 3		3.5	mA
Internal reference voltage output	V_{REF}	V_{DD} = 5 V, V_{SS} = -15 V	All	1	-5.3	-5.2	V
Internal reference output current sink capability		Constant external load during conversion	All	13, 14, 15		550	µA
Digital input low voltage	V_{INL}	CS, RD, HBEN, CLK IN. V_{DD} = 4.75 V	All	1, 2, 3		0.8	V
Digital input high voltage	V_{INH}	V_{SS} = -15 V	All	1, 2, 3	2.4		
Digital input capacitance	C_{IN}		All	13		10	pF
Digital input current	I_{IN}	CS, RD, HBEN. V_{DD} = 5 .25 V, V_{SS} = -15 V, A_{IN} = 0 to V_{DD}	All	1, 2, 3		±10	µA
		CLK IN. V_{DD} = 5.25 V, V_{SS} = -15 V, A_{IN} = 0 to V_{DD}	All			±20	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ unless otherwise specified	Device types	Group A subgroups	Limits		Unit
					Min	Max	
Digital output low voltage	V_{OL}	D11-D0/8, BUSY, CLK OUT V_{DD} = 4.75 V, V_{SS} = -15 V, Isink = 1.6 mA, Isource = 200 µA	All	1, 2, 3		0.4	V
Digital output high voltage	V_{OH}		All	1, 2, 3	4.0		
Floating state leakage current	V_{OL}	D11-D0/8. V_{DD} = 5.25 V, V_{SS} = -15 V	All	1, 2, 3		±10	µA
Floating state output capacitance	C_{OUT}		All	13, 14, 15		15	pF
Conversion time using synchronous clock	t_{CONV}		04, 05, 06	13, 14, 15		5	µs
			01, 02, 03			12.5	
Conversion time using asynchronous clock 1/	t_{CONV}		04, 05, 06	9, 10, 11	4.8	5.2	
			01, 02, 03		12.0	13.0	
Power supply current from V_{DD}	I_{DD}	V_{DD} = 5.25 V, V_{SS} = -15.75 V	All	1, 2, 3		7	mA
Power supply current from V_{SS}	I_{SS}	CS = $\overline{RD}$ = $\overline{BUSY}$ = HIGH A_{IN} = 5 V	All	1, 2, 3		12	
$\overline{CS}$ to $\overline{RD}$ setup time	t_1	See figures 4, 5, 6, and 7 2/	All	9, 14, 15	0		ns
$\overline{RD}$ to $\overline{BUSY}$ propagation delay	t_2		All	9		190	
				14, 15		270	
Data access time after $\overline{RD}$, C_L = 60 pF (see figure 2) 4/	t_3 3/		All	9		110	
				14, 15		150	
Data access time after $\overline{RD}$, C_L = 100 pF (see figure 2)	t_3 3/		All	9		125	
				14, 15		170	
$\overline{RD}$ pulse width	t_4		All	9, 14, 15	t_3		
$\overline{CS}$ to $\overline{RD}$ hold time	t_5		All	9, 14, 15	0		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ unless otherwise specified	Device types	Group A subgroups	Limits		Unit
					Min	Max	
Data setup time after $\overline{BUSY}$, C_L = 60 pF (see figure 2)	t_6 3/	See figures 4, 5, 6, and 7 2/	All	9		70	ns
				14, 15		100	
Bus relinquish time (see figure 3)	t_7 5/		All	9	35	90	
				14, 15	20	90	
HBEN to $\overline{RD}$ setup time	t_8		All	9, 14, 15	0		
HBEN to $\overline{RD}$ hold time	t_9		All	9, 14, 15	0		
Delay between successive read operations	t_{10}		All	9, 14, 15	500		

1/ Conversion time using asynchronous clock is measured by setting the clock frequency at the appropriate value (see 1.4) and checking all remaining tested specifications.
2/ All input control signals are specified with $t_r = t_f = 5$ ns (10 percent to 90 percent of +5 V) and timed from a voltage level of 1.6 V. Time t_6 and t_{10} are measured only for the initial test and after process or design changes which may affect switching parameters.
3/ Time t_3 and t_6 are measured with the load circuits of figure 2 and defined as the time required for an output to cross 0.8 V or 2.4 V.
4/ If not tested, shall be guaranteed to the limits specified in table I herein.
5/ Time t_7 is defined as the time required for the data lines to change 0.5 V when loaded with the circuits of figure 3.

Device type	ALL	
Case outline	L	3
Terminal number	Terminal symbol	
1	AIN	NC
2	V_{REF}	AIN
3	AGND	V_{REF}
4	D11	AGND
5	D10	D11
6	D9	D10
7	D8	D9
8	D7	NC
9	D6	D8
10	D5	D7
11	D4	D6
12	DGND	D5
13	D3/11	D4
14	D2/10	DGND
15	D1/9	NC
16	D0/8	D3/11
17	CLK IN	D2/10
18	CLK OUT	D1/9
19	HBEN	D0/8
20	$\overline{RD}$	CLK IN
21	$\overline{CS}$	CLK OUT
22	$\overline{BUSY}$	NC
23	V_{SS}	HBEN
24	V_{DD}	$\overline{RD}$
25	- - -	$\overline{CS}$
26	- - -	$\overline{BUSY}$
27	- - -	V_{SS}
28	- - -	V_{DD}

NC = no connect

FIGURE 1. Terminal connections.

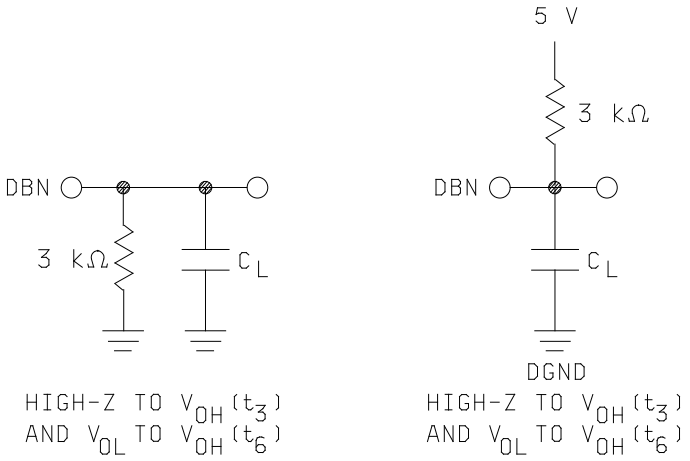


FIGURE 2. Load circuit for access time.

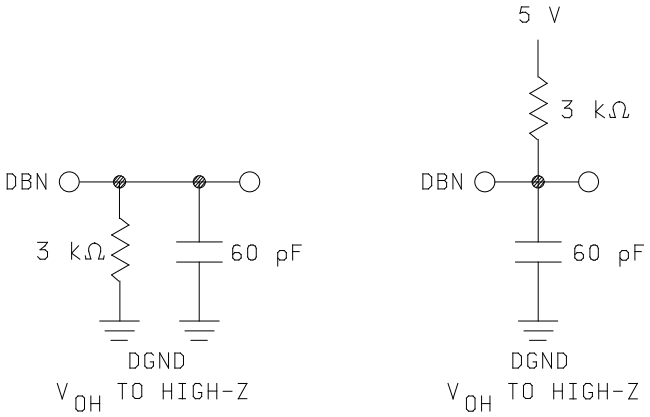


FIGURE 3. Load circuit for bus relinquish time.

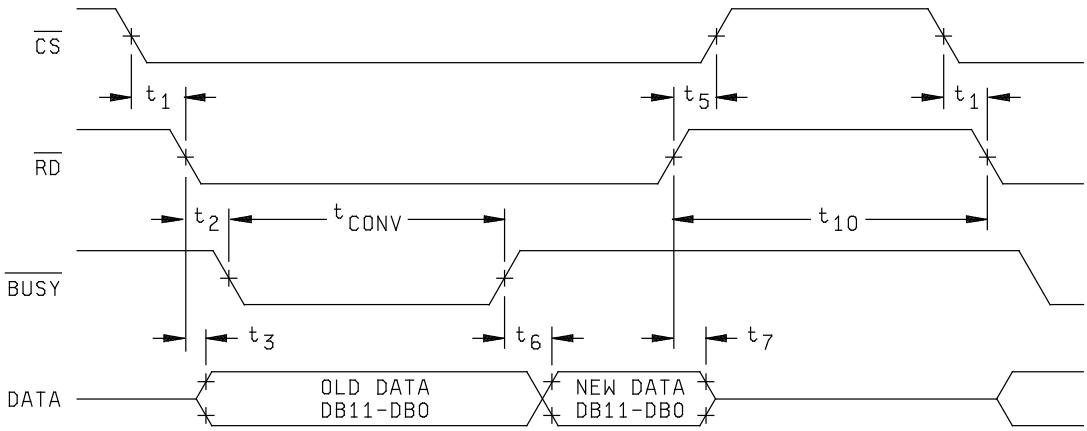


FIGURE 4. Slow memory mode, parallel read timing diagrams.

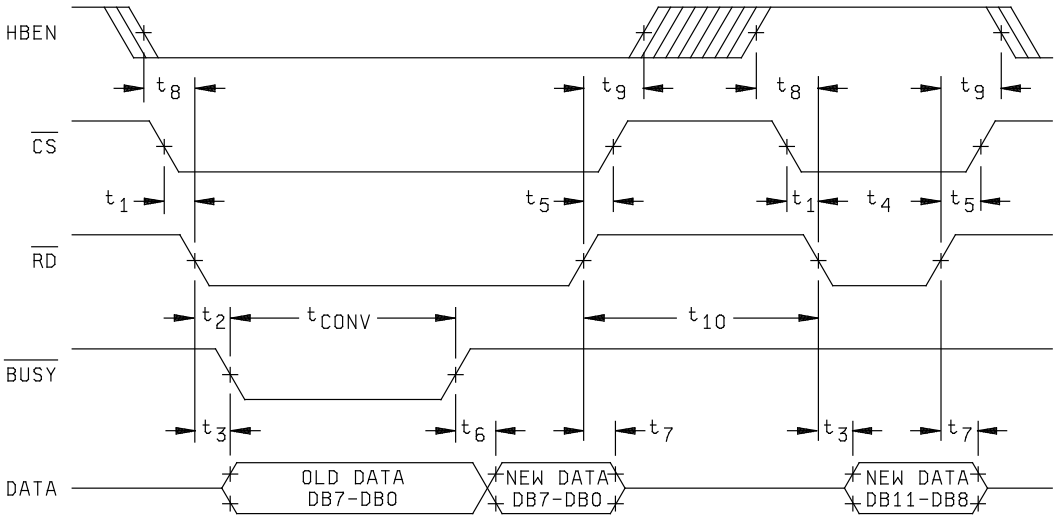


FIGURE 5. Slow memory mode, two byte read timing diagrams.

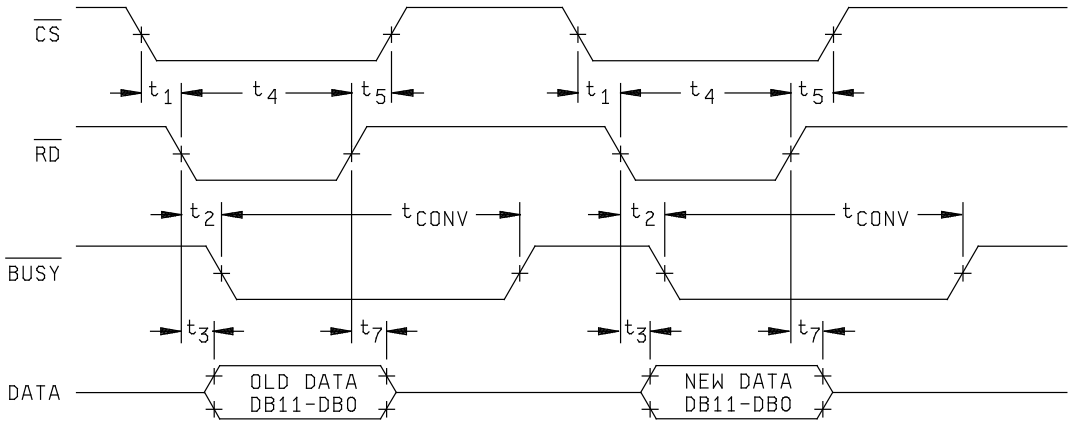


FIGURE 6. ROM mode, parallel read bus timing diagrams.

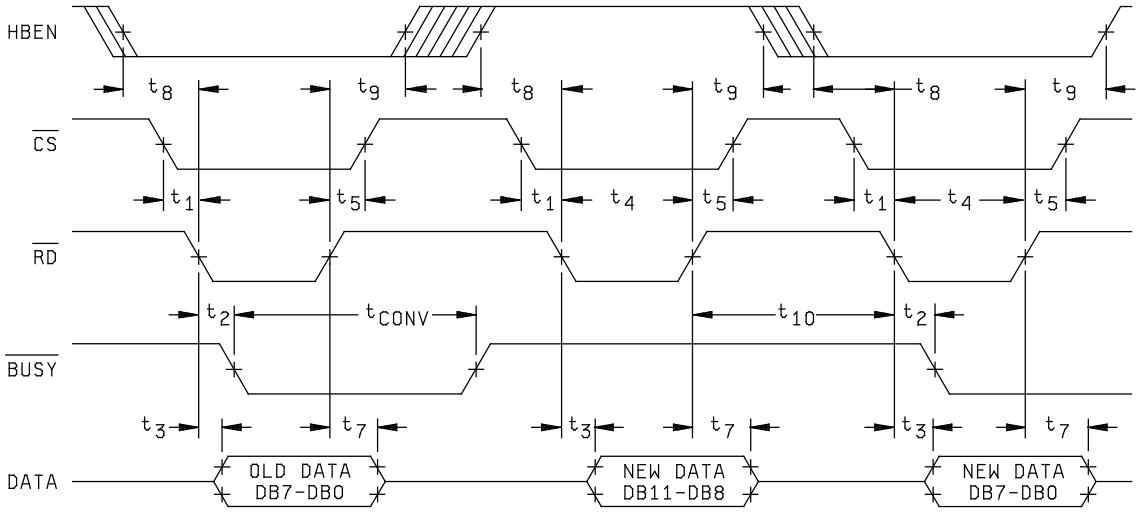


FIGURE 7. ROM mode, two byte read timing diagrams.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A or B. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

c. Special subgroup 12 (as referenced in table I) added for grading and selection tests at +25°C not included in PDA.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	1
Final electrical test parameters (method 5004)	1*, 2, 3, 9, 10, 11, 12
Group A test requirements (method 5005)	1, 2, 3, 9, 10, 11, 12, 13**, 14**, 15**
Groups C and D end-point electrical parameters (method 5005)	1, 12

* PDA applies to subgroup 1.
** Special subgroups 13, 14, and 15 shall be measured only for initial test and after process or design changes and shall be guaranteed to the limits specified in table I. Subgroup 13 is +25°C, 14 is +125°C, and 15 is -55°C.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, 6, 7, and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A or B. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform DLA Land and Maritime when a system application requires configuration control and the applicable SMD to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.5 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DLA Land and Maritime-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 13-01-25

Approved sources of supply for SMD 5962-87591 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8759101LA	24355	AD7572SQ12/883B
	1ES66	MX7572SQ12/883B
5962-87591013C	1ES66	MX7572SE12/883B
5962-8759102LA	3/	AD7572TQ12/883B
5962-87591023A	3/	AD7572TE12/883B
5962-8759103LA	3/	AD7572UQ12/883B
5962-87591033A	3/	AD7572UE12/883B
5962-8759104LA	24355	AD7572SQ05/883B
	1ES66	MX7572SQ05/883B
5962-87591043A	24355	AD7572SE05/883B
5962-87591043C	1ES66	MX7572SE05/883B
5962-8759105LA	24355	AD7572TQ05/883B
5962-87591053A	24355	AD7572TE05/883B
5962-8759106LA	3/	AD7572UQ05/883B
5962-87591063A	3/	AD7572UE05/883B

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
24355	Analog Devices Route 1 Industrial Park P.O. Box 9106 Norwood, MA 02062 Point of contact: Raheen Business Park Limerick, Ireland
1ES66	Maxim Integrated Products 120 San Gabriel Drive Sunnyvale, CA 94086-5125

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.