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## Features

- Frequency Range 5 GHz to 6 GHz
- $P_{out}$  25 dBm at 5.8 GHz
- Gain Typically 30 dB
- $P_{in}$  Typically 0 dBm
- $V_{CC}$  2.7V to 3.8V
- Power Consumption in Power-down Mode Typically  $< 1 \mu A$
- Package: QFN16 3 mm  $\times$  3 mm

## Benefits

- Biasing Control Extends Battery Time
- Simple Input and Output Matching
- Only One Single Supply Required
- No High-side Switching Transistor Required

## 1. Description

### 1.1 Process

This 5-GHz power amplifier (PA) is designed using Atmel's Silicon-Germanium (SiGe) process and provides high efficiency.

### 1.2 Circuitry

The PA, ATR7040, consists of a three-stage amplifier with a typical output power of 25 dBm. The output stage was implemented using an open-collector structure. Power up, power down, and output level are controlled at bias control pin 6 ( $V_{ctl}$ ).



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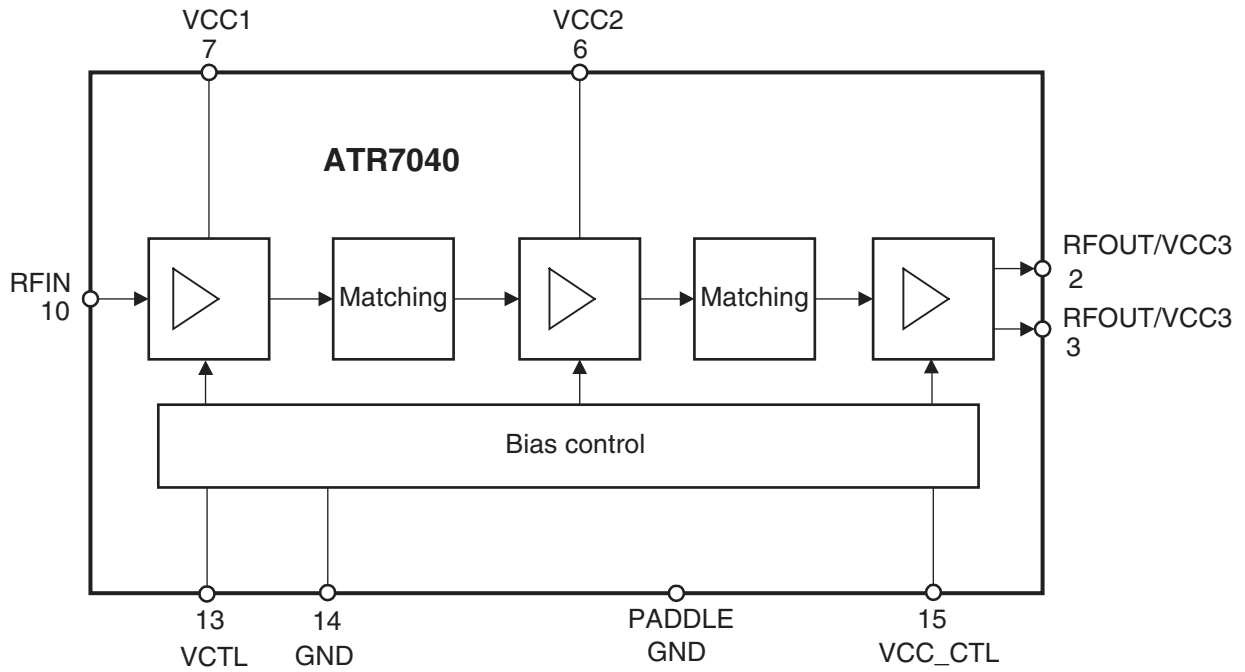
## 5.8 GHz WDCT Power Amplifier

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**ATR7040**



**Figure 1-1.** Block Diagram



## 2. Pin Configuration

Figure 2-1. Pinning QFN16

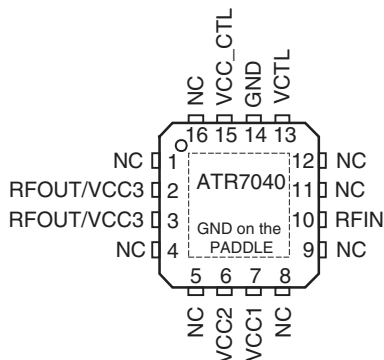


Table 2-1. Pin Description

Pin	Symbol	Function
1	NC	Not connected <sup>(1)</sup>
2	RFOUT	RF output and supply voltage for output amplifier stage
3	RFOUT	RF output and supply voltage for output amplifier stage
4	NC	Not connected <sup>(1)</sup>
5	NC	Not connected <sup>(1)</sup>
6	VCC2	Supply voltage for second amplifier stage
7	VCC1	Supply voltage for first amplifier stage
8	NC	Not connected <sup>(1)</sup>
9	NC	Not connected <sup>(1)</sup>
10	RFIN	RF input
11	NC	Not connected <sup>(1)</sup>
12	NC	Not connected <sup>(1)</sup>
13	VCTL	Control voltage for power ramping
14	GND	Ground
15	VCC_CTL	Supply voltage for biasing control block
16	NC	Not connected <sup>(1)</sup>
PADDLE	–	Ground

Note: 1. Pin can be connected to paddle for increased GND area

### 3. Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameters	Symbol	Value	Unit
Supply voltage	$V_{CC}$	5	V
Supply current	$I_{CC}$	400	mA
Junction temperature	$T_j$	150	°C
Storage temperature	$T_{Stg}$	-40 to +125	°C
Input RF power	$P_{in}$	10	dBm
Control voltage	$V_{ctl}$	2.5	V

Note: The part may not survive all maximums applied simultaneously.

Electrostatic sensitive device.  
Observe precautions for handling.



### 4. Thermal Resistance

Parameters	Symbol	Value	Unit
Junction ambient package QFN16, 3 × 3, slug soldered on PCB	$R_{thJA}$	40	K/W

### 5. Operating Range

Parameters	Symbol	Value	Unit
Supply voltage	$V_{CC}$	2.7 to 3.8	V
Operating frequency range	$f_{in}$	5100 to 5900	MHz
Ambient temperature range	$T_{amb}$	-25 to +75	°C

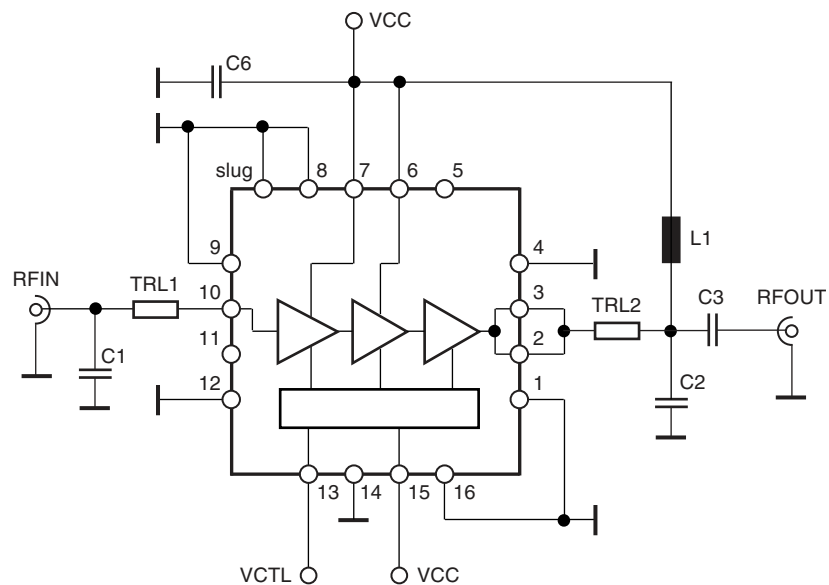
## 6. Electrical Characteristics

Operating conditions:  $V_{CC} = 3.6V$ ,  $V_{ctl} = 1.5V$ , input frequency = 5.8 GHz, input power 0 dBm, pulsed mode, duty cycle 10%,  $t_{on} = 1$  ms,  $T_{amb} = 25^{\circ}C$ , unless otherwise specified.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit
1.0	Frequency range	Depends on external circuitry			5100		5900	MHz
1.1	Supply voltage			$V_{CC}$	2.7	3.6	3.8	V
1.2	Input power			$P_{in}$		0		dBm
1.3	Saturated power output			$P_{sat}$		25		dBm
1.4	Output power deviation			$P_d$	-2		+2	dB
1.5	Control voltage range	PA operating mode		$V_{ctl}$	1.0		1.7	V
		Power-down mode		$V_{ctl}$			0.2	V
1.6	Control input current	PA on	5	$I_{ctl}$		90		$\mu A$
1.7	Input return loss	With external matching	10			-7	-6	dB
1.8	Isolation	$V_{ctl} \leq 0.2V$		$ISO_r$	33	35		dB
1.9	Power added efficiency	At power saturation, $P_{in} = 0$ dBm		PAE		35		%
1.10	Current consumption	For 25 dBm output power		$I_{cc}$		250		mA
1.11	Current consumption in power-down mode	$V_{ctl} \leq 0.2V$		$I_{cc}$		1		$\mu A$
1.12	Duty cycle of operation	At saturated output power				100		%

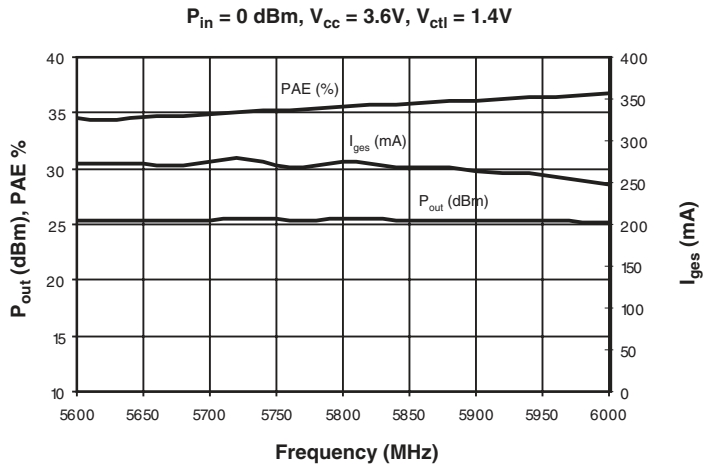
## 7. Application Circuit

Figure 7-1. Application Circuit

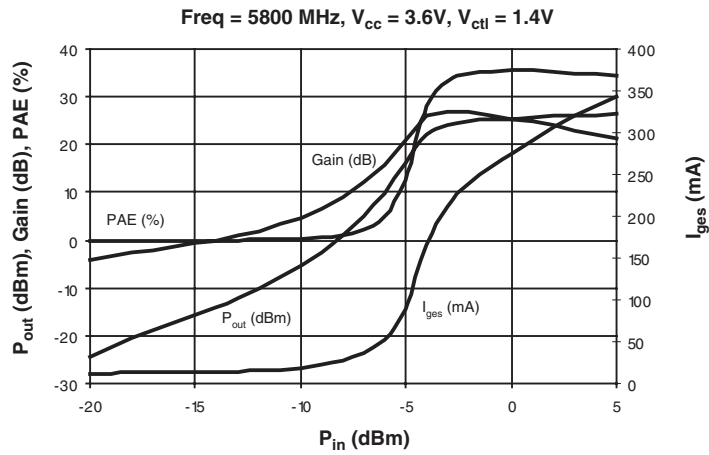


## 8. Diagrams

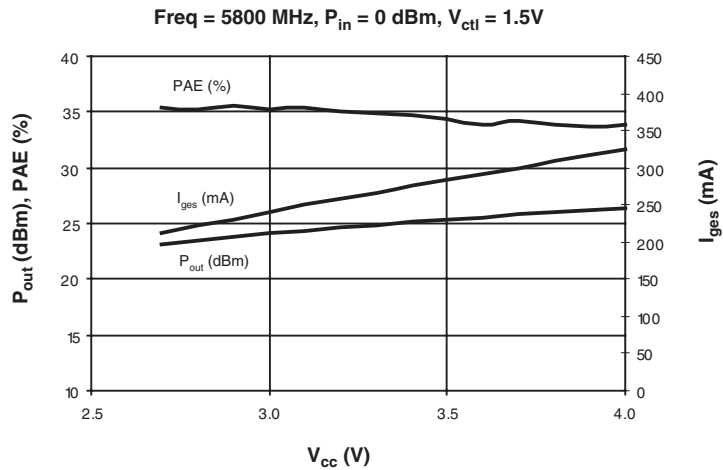
**Figure 8-1.** Output Power, Efficiency and Supply Currents Versus Input Frequency



**Figure 8-2.** Output Power, Gain, Efficiency and Supply Currents Versus Input Power



**Figure 8-3.** Output Power, Efficiency and Supply Currents Versus Operating Voltage



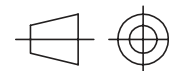
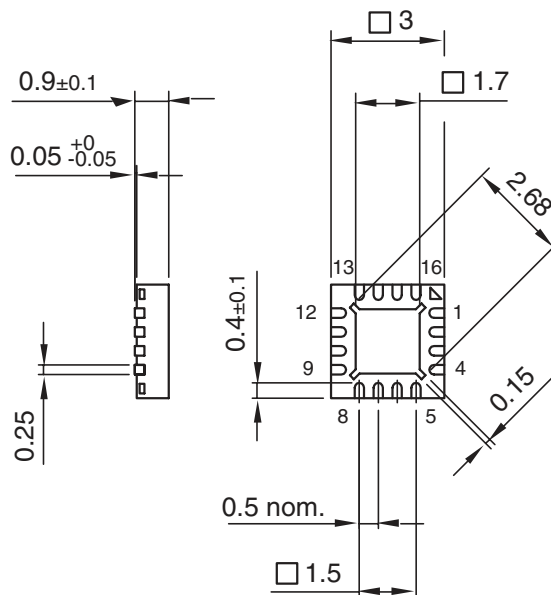
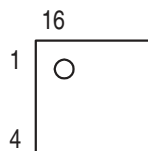
## 9. Ordering Information

Extended Type Number	Package	Remarks
ATR7040-PVPG	QFN16, 3 × 3	Taped and reeled, MOQ 2000, Pb-free
ATR7040-PVQG	QFN16, 3 × 3	Taped and reeled, MOQ 8000, Pb-free

## 10. Package Information

Package: QFN 16 - 3x3  
 Exposed pad 1.7x1.7  
 (acc. JEDEC OUTLINE No. MO-220)  
 Dimensions in mm

Not indicated tolerances ±0.05



technical drawings  
 according to DIN  
 specifications

Drawing-No.: 6.543-5115.01-4

Issue: 1; 07.03.05

Assembly Chip PAC



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