



# VND810SP-E

## DOUBLE CHANNEL HIGH SIDE DRIVER

**Table 1. General Features**

Type	R <sub>DS(on)</sub>	I <sub>out</sub>	V <sub>CC</sub>
VND810SP-E	160 mΩ (*)	3.5 A (*)	36 V

(\*) Per each channel

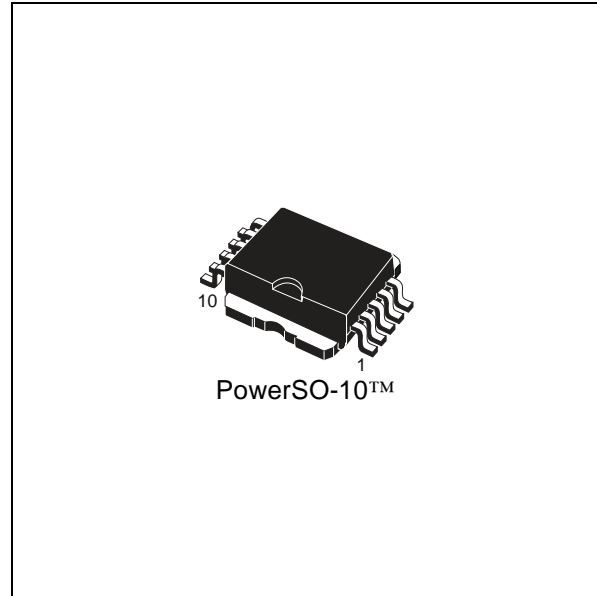
- CMOS COMPATIBLE INPUTS
- OPEN DRAIN STATUS OUTPUTS
- ON STATE OPEN LOAD DETECTION
- OFF STATE OPEN LOAD DETECTION
- SHORTED LOAD PROTECTION
- UNDERVOLTAGE AND OVERVOLTAGE SHUTDOWN
- PROTECTION AGAINST LOSS OF GROUND
- VERY LOW STAND-BY CURRENT
- REVERSE BATTERY PROTECTION (\*\*)
- IN COMPLIANCE WITH THE 2002/95/EC EUROPEAN DIRECTIVE

### DESCRIPTION

The VND810SP-E is a monolithic device made by using STMicroelectronics VIPower M0-3 Technology, intended for driving any kind of load with one side connected to ground.

Active V<sub>CC</sub> pin voltage clamp protects the device against low energy spikes (see ISO7637 transient compatibility table).

**Figure 1. Package**



Active current limitation combined with thermal shutdown and automatic restart protects the device against overload. The device detects open load condition both in on and off state. Output shorted to V<sub>CC</sub> is detected in the off state. Device automatically turns off in case of ground pin disconnection.

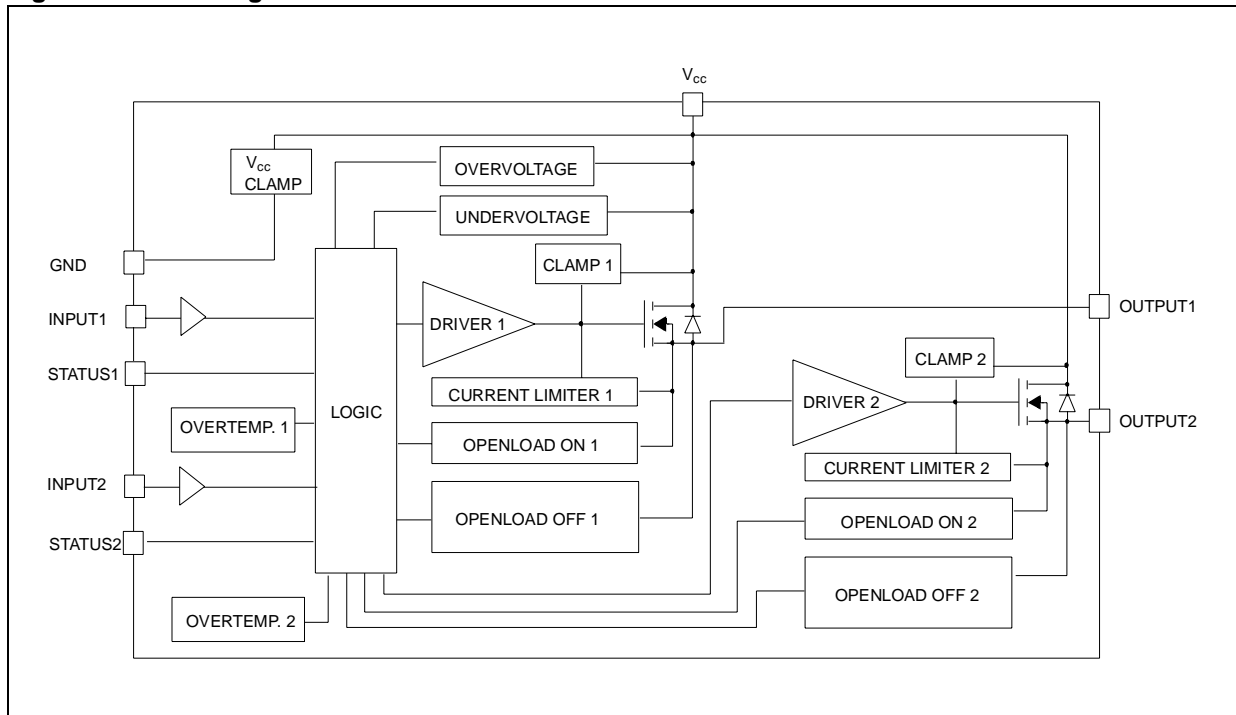
**Table 2. Order Codes**

Package	Tube	Tape and Reel
PowerSO-10™	VND810SP-E	VND810SPTR-E

Note: (\*\*) See application schematic at page 9

# VND810SP-E

**Figure 2. Block Diagram**



**Table 3. Absolute Maximum Ratings**

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage	41	V
- V <sub>CC</sub>	Reverse DC Supply Voltage	- 0.3	V
- I <sub>GND</sub>	DC Reverse Ground Pin Current	- 200	mA
I <sub>OUT</sub>	DC Output Current	Internally Limited	A
- I <sub>OUT</sub>	Reverse DC Output Current	- 6	A
I <sub>IN</sub>	DC Input Current	+/- 10	mA
I <sub>stat</sub>	DC Status Current	+/- 10	mA
V <sub>ESD</sub>	Electrostatic Discharge (Human Body Model: R=1.5KΩ; C=100pF)		
	- INPUT	4000	V
	- STATUS	4000	V
	- OUTPUT	5000	V
	- V <sub>CC</sub>	5000	V
E <sub>MAX</sub>	Maximum Switching Energy (L=1.4mH; R <sub>L</sub> =0Ω; V <sub>bat</sub> =13.5V; T <sub>jstart</sub> =150°C; I <sub>L</sub> =5A)	24	mJ
P <sub>tot</sub>	Power Dissipation T <sub>C</sub> =25°C	52	W
T <sub>j</sub>	Junction Operating Temperature	Internally Limited	°C
T <sub>C</sub>	Case Operating Temperature	- 40 to 150	°C
T <sub>stg</sub>	Storage Temperature	- 55 to 150	°C

Figure 3. Configuration Diagram (Top View) & Suggested Connections for Unused and N.C. Pins

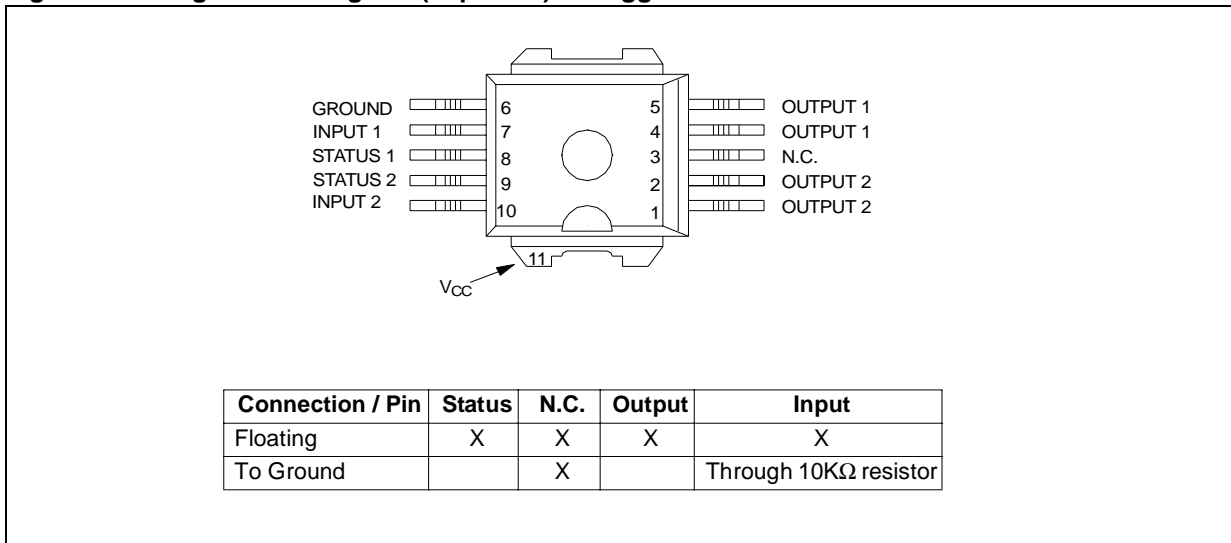


Figure 4. Current and Voltage Conventions

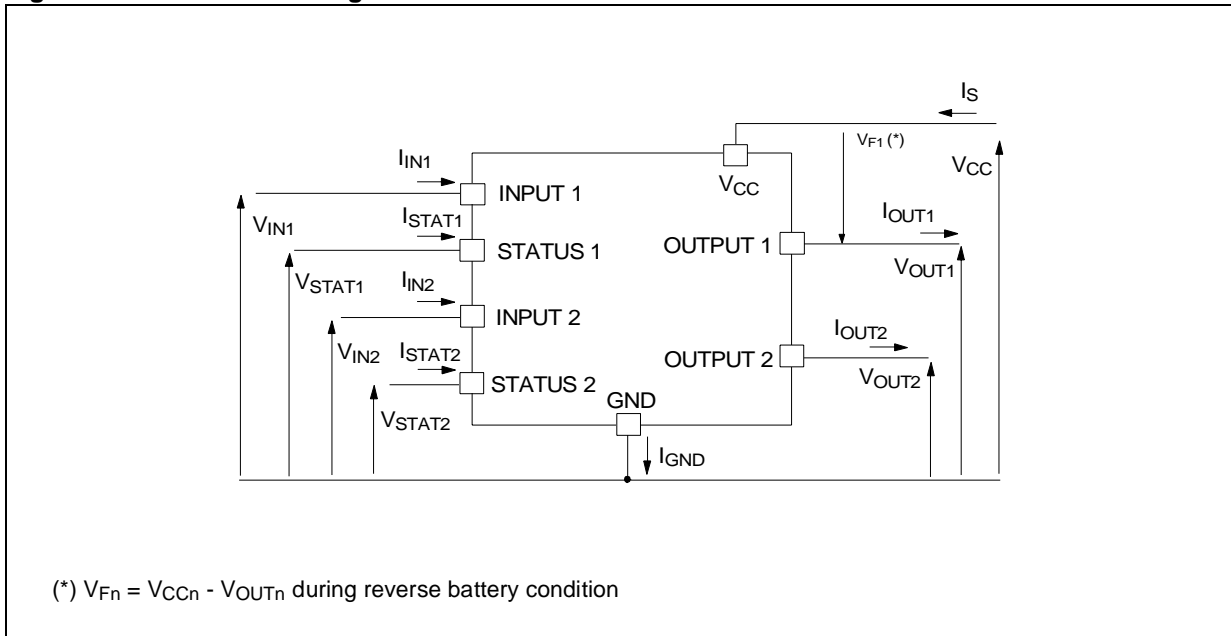


Table 4. Thermal Data

Symbol	Parameter	Value	Unit
R <sub>thj-case</sub>	Thermal Resistance Junction-case	2.4	°C/W
R <sub>thj-amb</sub>	Thermal Resistance Junction-ambient	52.4 <sup>(1)</sup>   37 <sup>(2)</sup>	°C/W

Note: 1. When mounted on a standard single-sided FR-4 board with 0.5 cm<sup>2</sup> of Cu (at least 35μm thick). Horizontal mounting and no artificial air flow.

Note: 2. When mounted on a standard single-sided FR-4 board with 6 cm<sup>2</sup> of Cu (at least 35μm thick). Horizontal mounting and no artificial air flow

**ELECTRICAL CHARACTERISTICS**

 (8V < V<sub>CC</sub> < 36V; -40°C < T<sub>j</sub> < 150°C, unless otherwise specified)

(Per each channel)

**Table 5. Power Output**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>CC</sub> (**)	Operating Supply Voltage		5.5	13	36	V
V <sub>USD</sub> (**)	Undervoltage Shut-down		3	4	5.5	V
V <sub>OV</sub> (**)	Overvoltage Shut-down		36			V
R <sub>ON</sub>	On State Resistance	I <sub>OUT</sub> =1A; T <sub>j</sub> =25°C I <sub>OUT</sub> =1A; V <sub>CC</sub> >8V			160 320	mΩ mΩ
I <sub>S</sub> (**)	Supply Current	Off State; V <sub>CC</sub> =13V; V <sub>IN</sub> =V <sub>OUT</sub> =0V Off State; V <sub>CC</sub> =13V; V <sub>IN</sub> =V <sub>OUT</sub> =0V; T <sub>j</sub> =25°C On State; V <sub>CC</sub> =13V; V <sub>IN</sub> =5V; I <sub>OUT</sub> =0A		12 12 5	40 25 7	μA μA mA
I <sub>L(off1)</sub>	Off State Output Current	V <sub>IN</sub> =V <sub>OUT</sub> =0V	0		50	μA
I <sub>L(off2)</sub>	Off State Output Current	V <sub>IN</sub> =0V; V <sub>OUT</sub> =3.5V	-75		0	μA
I <sub>L(off3)</sub>	Off State Output Current	V <sub>IN</sub> =V <sub>OUT</sub> =0V; V <sub>CC</sub> =13V; T <sub>j</sub> =125°C			5	μA
I <sub>L(off4)</sub>	Off State Output Current	V <sub>IN</sub> =V <sub>OUT</sub> =0V; V <sub>CC</sub> =13V; T <sub>j</sub> =25°C			3	μA

Note: (\*\*) Per device.

**Table 6. Protection (see note 1)**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
T <sub>TSD</sub>	Shut-down Temperature		150	175	200	°C
T <sub>R</sub>	Reset Temperature		135			°C
T <sub>hyst</sub>	Thermal Hysteresis		7	15		°C
t <sub>sdl</sub>	Status Delay in Overload Conditions	T <sub>j</sub> >T <sub>TSD</sub>			20	μs
I <sub>lim</sub>	Current limitation	5.5V < V <sub>CC</sub> < 36V	3.5	5	7.5 7.5	A A
V <sub>demag</sub>	Turn-off Output Clamp Voltage	I <sub>OUT</sub> =1A; L=6mH	V <sub>CC</sub> -41	V <sub>CC</sub> -48	V <sub>CC</sub> -55	V

Note: 1. To ensure long term reliability under heavy overload or short circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device is subjected to abnormal conditions, this software must limit the duration and number of activation cycles

**Table 7. V<sub>CC</sub> - Output Diode**

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V <sub>F</sub>	Forward on Voltage	-I <sub>OUT</sub> =0.5A; T <sub>j</sub> =150°C			0.6	V

## ELECTRICAL CHARACTERISTICS (continued)

Table 8. Status Pin

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V <sub>STAT</sub>	Status Low Output Voltage	I <sub>STAT</sub> = 1.6 mA			0.5	V
I <sub>LSTAT</sub>	Status Leakage Current	Normal Operation; V <sub>STAT</sub> = 5V			10	μA
C <sub>STAT</sub>	Status Pin Input Capacitance	Normal Operation; V <sub>STAT</sub> = 5V			100	pF
V <sub>SCL</sub>	Status Clamp Voltage	I <sub>STAT</sub> = 1mA I <sub>STAT</sub> = - 1mA	6	6.8 -0.7	8	V V

Table 9. Switching (V<sub>CC</sub>=13V)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
t <sub>d(on)</sub>	Turn-on Delay Time	R <sub>L</sub> =13Ω from V <sub>IN</sub> rising edge to V <sub>OUT</sub> =1.3V		30		μs
t <sub>d(off)</sub>	Turn-off Delay Time	R <sub>L</sub> =13Ω from V <sub>IN</sub> falling edge to V <sub>OUT</sub> =11.7V		30		μs
dV <sub>OUT</sub> /dt <sub>(on)</sub>	Turn-on Voltage Slope	R <sub>L</sub> =13Ω from V <sub>OUT</sub> =1.3V to V <sub>OUT</sub> =10.4V		See relative diagram		V/μs
dV <sub>OUT</sub> /dt <sub>(off)</sub>	Turn-off Voltage Slope	R <sub>L</sub> =13Ω from V <sub>OUT</sub> =11.7V to V <sub>OUT</sub> =1.3V		See relative diagram		V/μs

Table 10. Openload Detection

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I <sub>OL</sub>	Openload ON State Detection Threshold	V <sub>IN</sub> =5V	20	40	80	mA
t <sub>DOL(on)</sub>	Openload ON State Detection Delay	I <sub>OUT</sub> =0A			200	μs
V <sub>OL</sub>	Openload OFF State Voltage Detection Threshold	V <sub>IN</sub> =0V	1.5	2.5	3.5	V
t <sub>DOL(off)</sub>	Openload Detection Delay at Turn Off				1000	μs

Table 11. Logic Input

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V <sub>IL</sub>	Input Low Level				1.25	V
I <sub>IL</sub>	Low Level Input Current	V <sub>IN</sub> = 1.25V	1			μA
V <sub>IH</sub>	Input High Level		3.25			V
I <sub>IH</sub>	High Level Input Current	V <sub>IN</sub> = 3.25V			10	μA
V <sub>hyst</sub>	Input Hysteresis Voltage		0.5			V
V <sub>ICL</sub>	Input Clamp Voltage	I <sub>IN</sub> = 1mA I <sub>IN</sub> = -1mA	6	6.8 -0.7	8	V V

Figure 5.

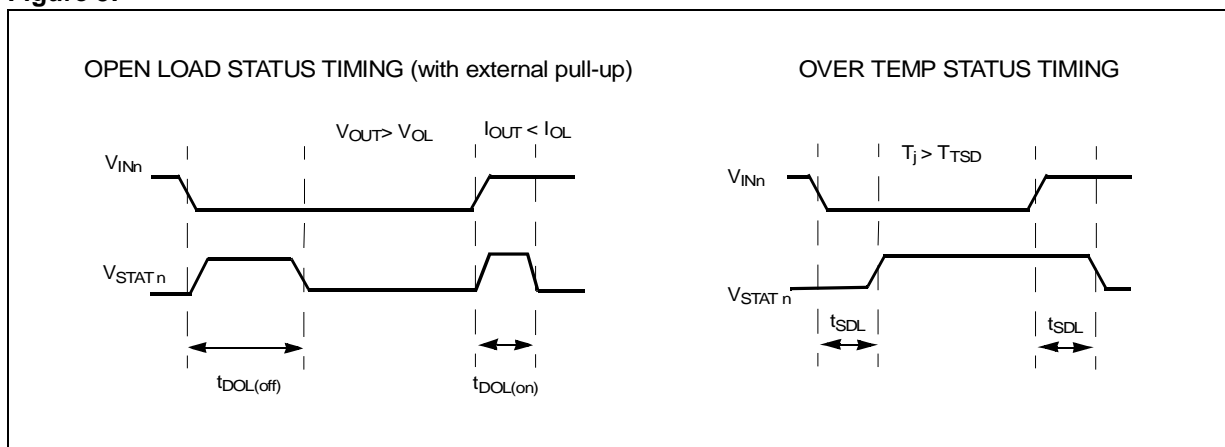


Table 12. Truth Table

CONDITIONS	INPUT	OUTPUT	SENSE
Normal Operation	L H	L H	H H
Current Limitation	L H H	L X X	H ( $T_j < T_{TSD}$ ) H ( $T_j > T_{TSD}$ ) L
Overtemperature	L H	L L	H L
Undervoltage	L H	L L	X X
Overvoltage	L H	L L	H H
Output Voltage > $V_{OL}$	L H	H H	L H
Output Current < $I_{OL}$	L H	L H	H L

Figure 6. Switching Time Waveforms

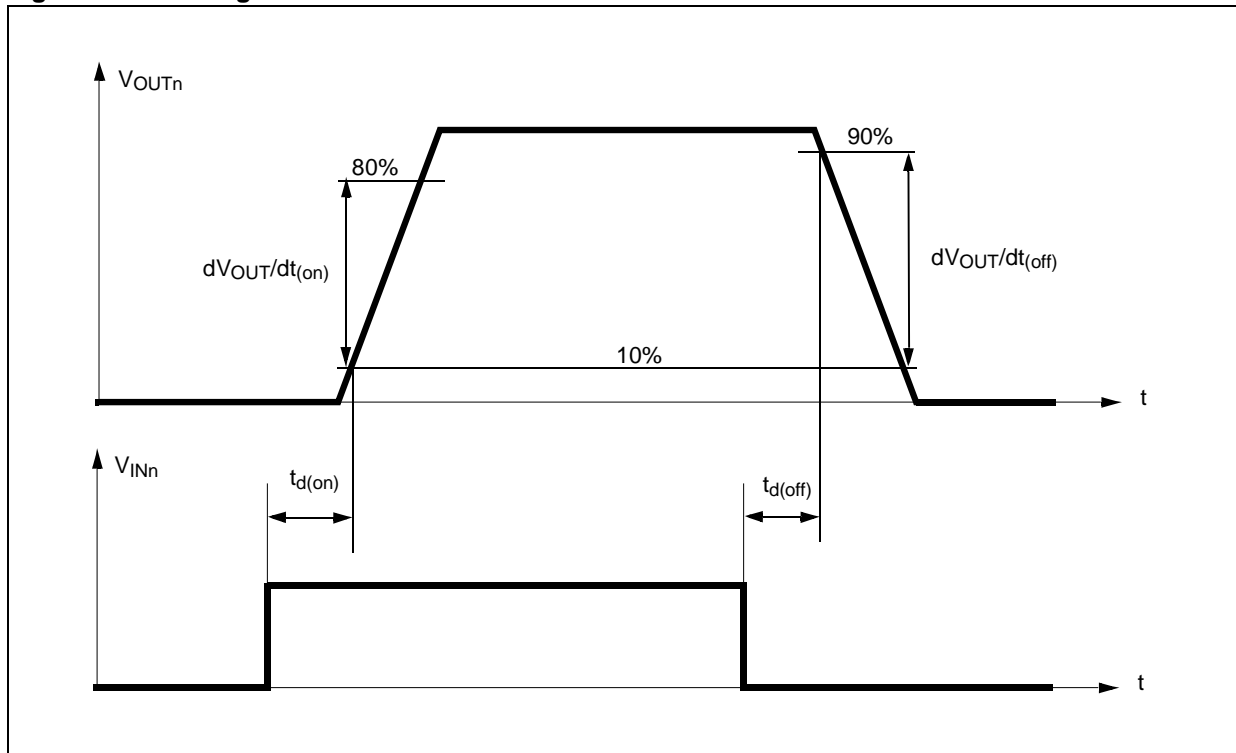


Table 13. Electrical Transient Requirements On V<sub>CC</sub> Pin

ISO T/R 7637/1 Test Pulse	TEST LEVELS				Delays and Impedance
	I	II	III	IV	
1	-25 V	-50 V	-75 V	-100 V	2 ms 10 Ω
2	+25 V	+50 V	+75 V	+100 V	0.2 ms 10 Ω
3a	-25 V	-50 V	-100 V	-150 V	0.1 μs 50 Ω
3b	+25 V	+50 V	+75 V	+100 V	0.1 μs 50 Ω
4	-4 V	-5 V	-6 V	-7 V	100 ms, 0.01 Ω
5	+26.5 V	+46.5 V	+66.5 V	+86.5 V	400 ms, 2 Ω

ISO T/R 7637/1 Test Pulse	TEST LEVELS RESULTS			
	I	II	III	IV
1	C	C	C	C
2	C	C	C	C
3a	C	C	C	C
3b	C	C	C	C
4	C	C	C	C
5	C	E	E	E

CLASS	CONTENTS
C	All functions of the device are performed as designed after exposure to disturbance.
E	One or more functions of the device is not performed as designed after exposure and cannot be returned to proper operation without replacing the device.

Figure 7. Waveforms

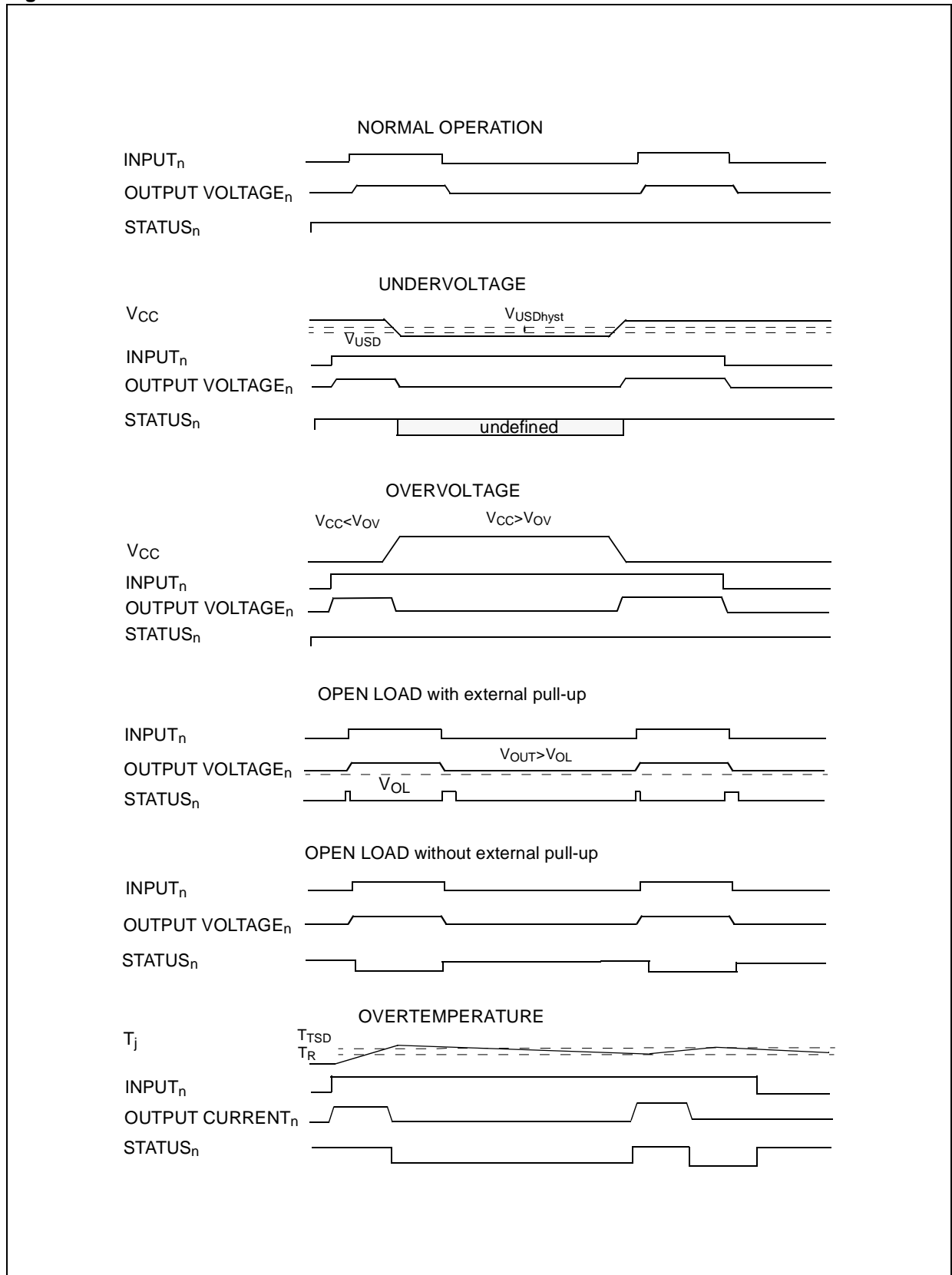
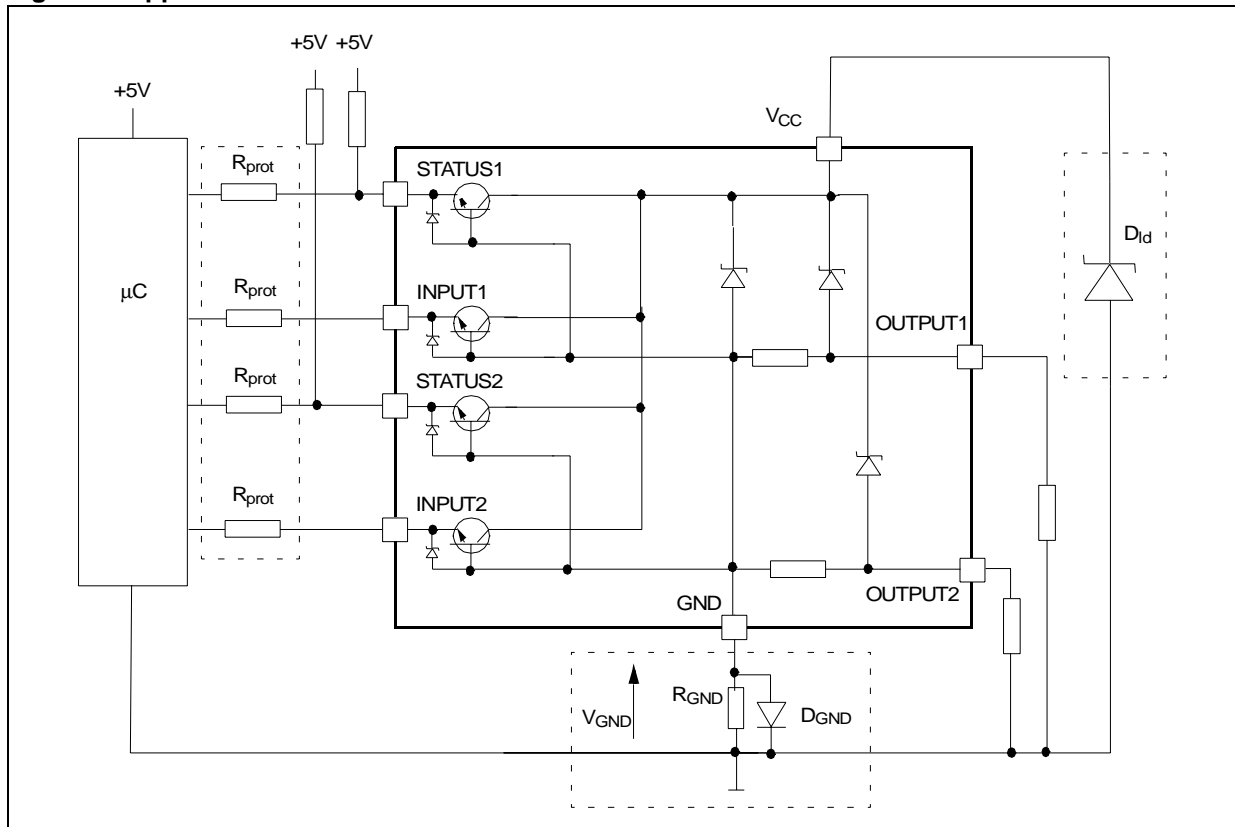




Figure 8. Application Schematic



### GND PROTECTION NETWORK AGAINST REVERSE BATTERY

**Solution 1:** Resistor in the ground line ( $R_{GND}$  only). This can be used with any type of load.

The following is an indication on how to dimension the  $R_{GND}$  resistor.

- 1)  $R_{GND} \leq 600\text{mV} / I_{S(\text{on})\text{max}}$ .
- 2)  $R_{GND} \geq (-V_{CC}) / (-I_{GND})$

where  $-I_{GND}$  is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device's datasheet.

Power Dissipation in  $R_{GND}$  (when  $V_{CC} < 0$ : during reverse battery situations) is:

$$P_D = (-V_{CC})^2 / R_{GND}$$

This resistor can be shared amongst several different HSD. Please note that the value of this resistor should be calculated with formula (1) where  $I_{S(\text{on})\text{max}}$  becomes the sum of the maximum on-state currents of the different devices.

Please note that if the microprocessor ground is not common with the device ground then the  $R_{GND}$  will produce a shift ( $I_{S(\text{on})\text{max}} * R_{GND}$ ) in the input thresholds and the status output values. this shift will vary. If a ground protection network is used and negative transient are present on the  $V_{CC}$  line, the control pins will be pulled negative.

ST suggests to insert a resistor ( $R_{prot}$ ) in line to prevent the  $\mu\text{C}$  I/Os pins to latch-up.

depending on how many devices are ON in the case of several high side drivers sharing the same  $R_{GND}$ .

If the calculated power dissipation leads to a large resistor or several devices have to share the same resistor then the ST suggests to utilize Solution 2 (see below).

**Solution 2:** A diode ( $D_{GND}$ ) in the ground line.

A resistor ( $R_{GND} = 1\text{k}\Omega$ ) should be inserted in parallel to  $D_{GND}$  if the device will be driving an inductive load.

This small signal diode can be safely shared amongst several different HSD. Also in this case, the presence of the ground network will produce a shift ( $\approx 600\text{mV}$ ) in the input threshold and the status output values if the microprocessor ground is not common with the device ground. This shift will not vary if more than one HSD shares the same diode/resistor network.

Series resistor in INPUT and STATUS lines are also required to prevent that, during battery voltage transient, the current exceeds the Absolute Maximum Rating.

Safest configuration for unused INPUT and STATUS pin is to leave them unconnected.

### LOAD DUMP PROTECTION

$D_{ld}$  is necessary (Voltage Transient Suppressor) if the load dump peak voltage exceeds  $V_{CC}$  max DC rating. The same applies if the device will be subject to transients on the  $V_{CC}$  line that are greater than the ones shown in the ISO T/R 7637/1 table.

**µC I/Os PROTECTION:**

If a ground protection network is used and negative transient are present on the V<sub>CC</sub> line, the control pins will be pulled negative. ST suggests to insert a resistor (R<sub>prot</sub>) in line to prevent the µC I/Os pins to latch-up.

The value of these resistors is a compromise between the leakage current of µC and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of µC I/Os.

$$-V_{CCpeak}/I_{latchup} \leq R_{prot} \leq (V_{OH\mu C} - V_{IH} - V_{GND}) / I_{IHmax}$$

Calculation example:

For V<sub>CCpeak</sub> = -100V and I<sub>latchup</sub> ≥ 20mA; V<sub>OHµC</sub> ≥ 4.5V  
 5kΩ ≤ R<sub>prot</sub> ≤ 65kΩ.

Recommended R<sub>prot</sub> value is 10kΩ.

**OPEN LOAD DETECTION IN OFF STATE**

Off state open load detection requires an external pull-up resistor (R<sub>PU</sub>) connected between OUTPUT pin and a positive supply voltage (V<sub>PU</sub>) like the +5V line used to

supply the microprocessor.

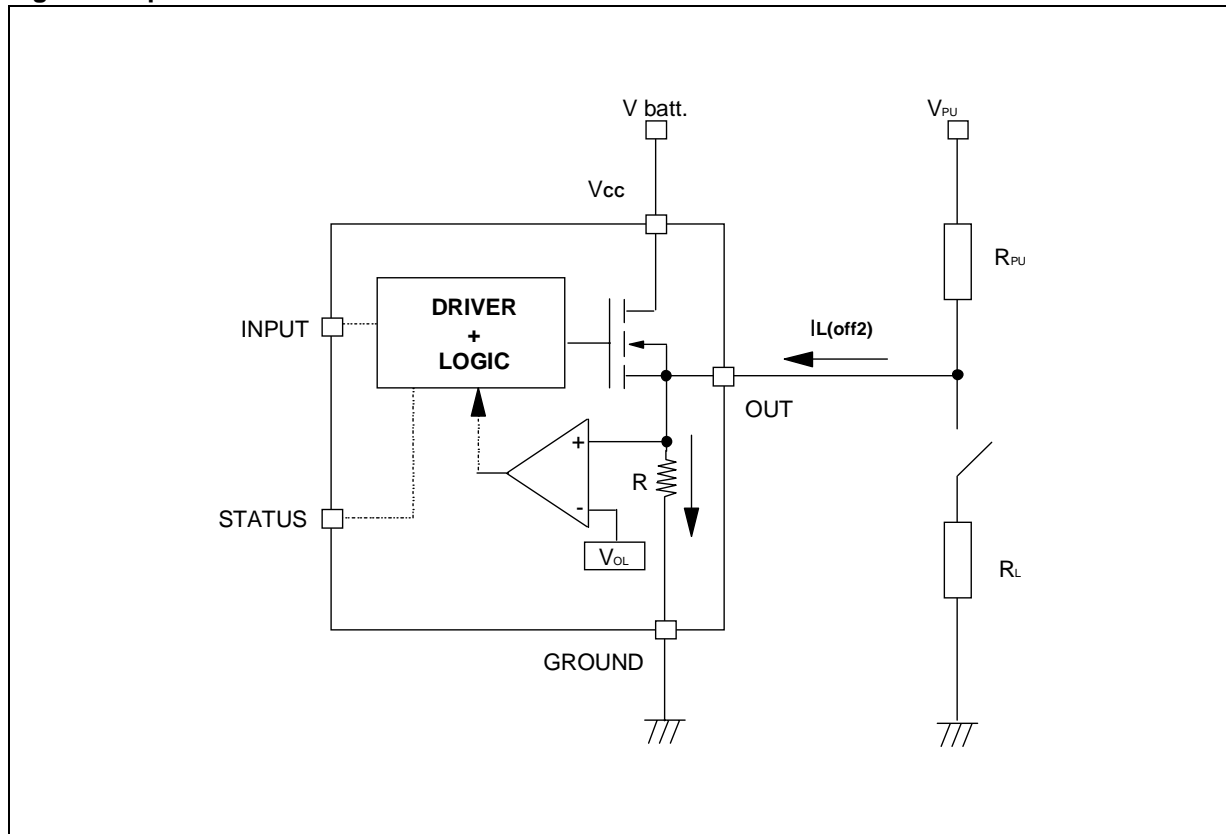
The external resistor has to be selected according to the following requirements:

- 1) no false open load indication when load is connected: in this case we have to avoid V<sub>OUT</sub> to be higher than V<sub>OLmin</sub>; this results in the following condition  
 $V_{OUT} = (V_{PU} / (R_L + R_{PU})) R_L < V_{OLmin}$ .
- 2) no misdetection when load is disconnected: in this case the V<sub>OUT</sub> has to be higher than V<sub>OLmax</sub>; this results in the following condition  
 $R_{PU} < (V_{PU} - V_{OLmax}) / I_{L(off2)}$ .

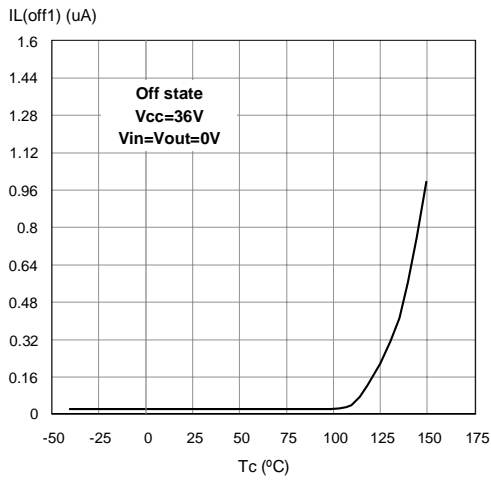
Because I<sub>s(OFF)</sub> may significantly increase if V<sub>out</sub> is pulled high (up to several mA), the pull-up resistor R<sub>PU</sub> should be connected to a supply that is switched OFF when the module is in standby.

The values of V<sub>OLmin</sub>, V<sub>OLmax</sub> and I<sub>L(off2)</sub> are available in the Electrical Characteristics section.

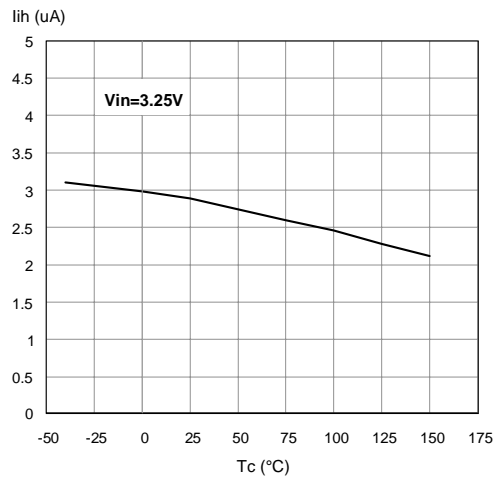
**Figure 9. Open Load detection in off state**



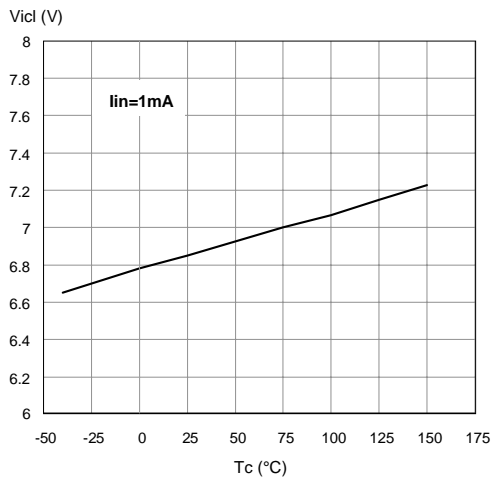
**Figure 10. Off State Output Current**



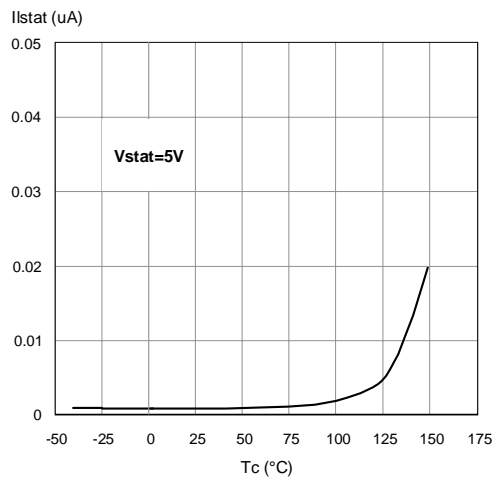
**Figure 13. High Level Input Current**



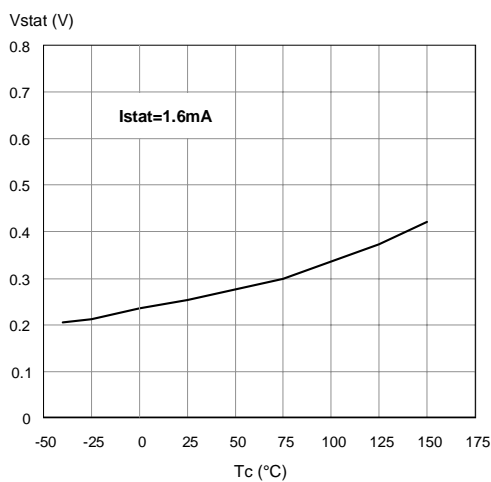
**Figure 11. Input Clamp Voltage**



**Figure 14. Status Leakage Current**



**Figure 12. Status Low Output Voltage**



**Figure 15. Status Clamp Voltage**

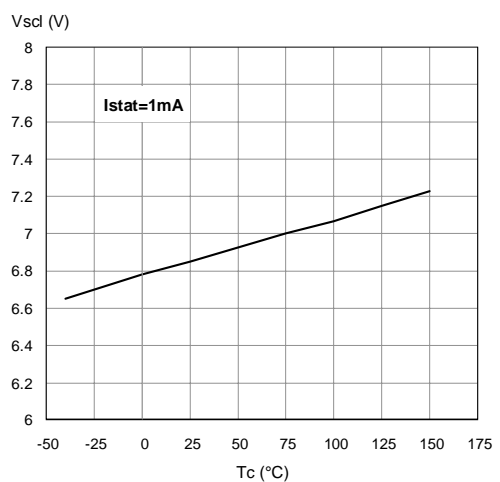


Figure 16. On State Resistance Vs  $T_{case}$

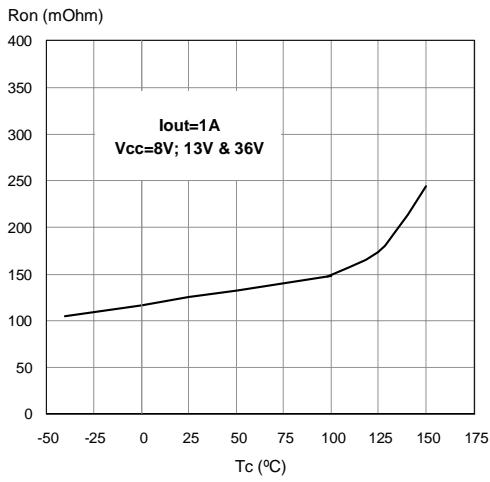


Figure 19. On State Resistance Vs  $V_{CC}$

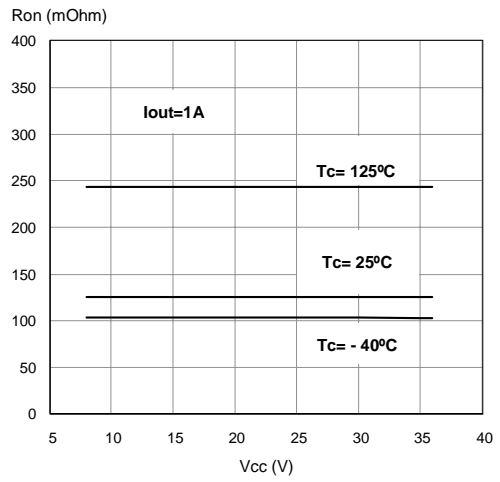


Figure 17. Openload On State Detection Threshold

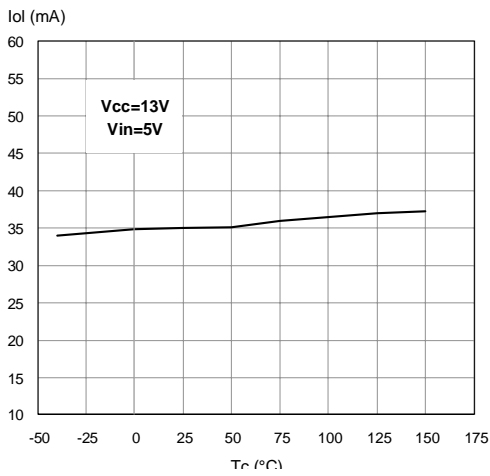


Figure 20. Openload Off State Detection Threshold

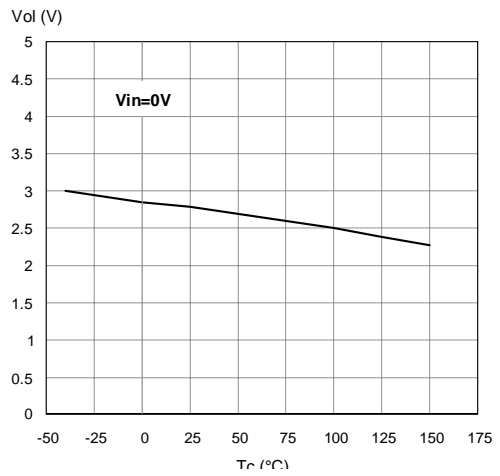


Figure 18. Input High Level

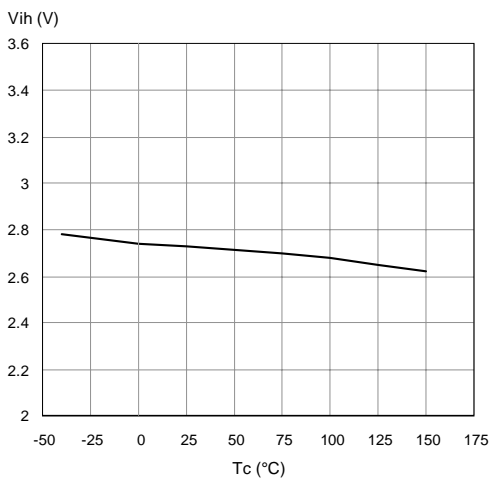


Figure 21. Input Low Level

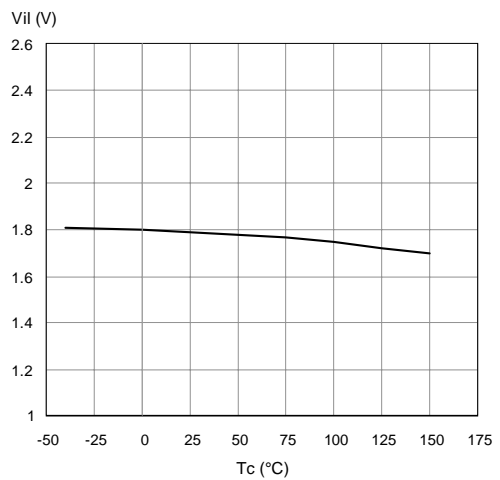


Figure 22. Input Hysteresis Voltage

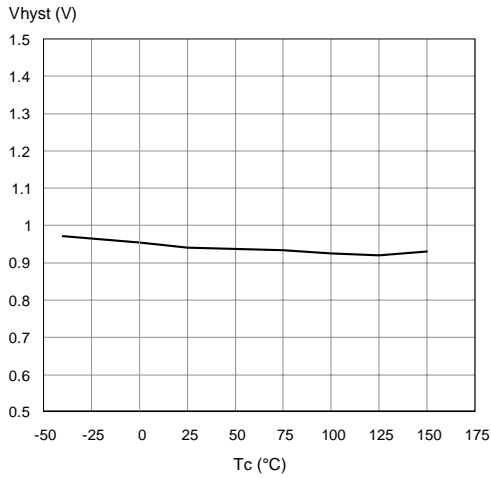


Figure 25. Overvoltage Shutdown

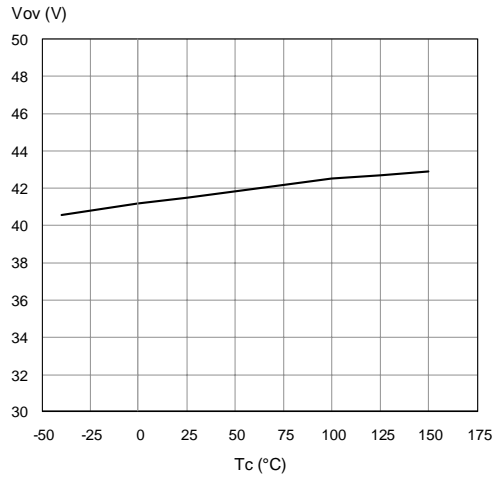


Figure 23. Turn-on Voltage Slope

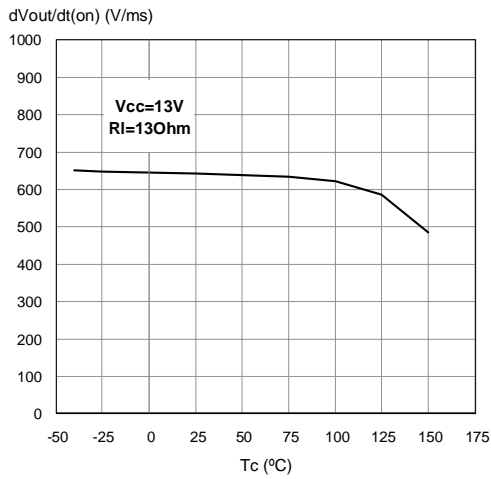


Figure 26. Turn-off Voltage Slope

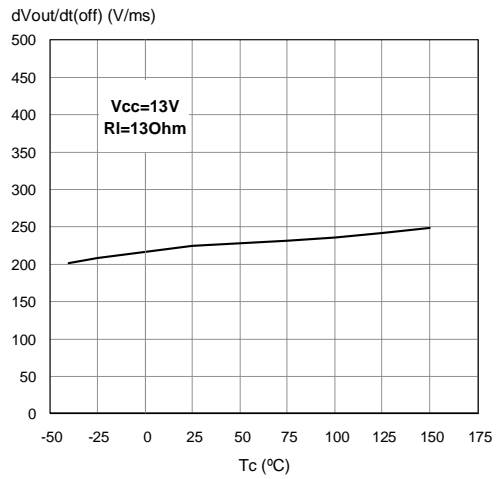


Figure 24. I<sub>LIM</sub> Vs T<sub>case</sub>

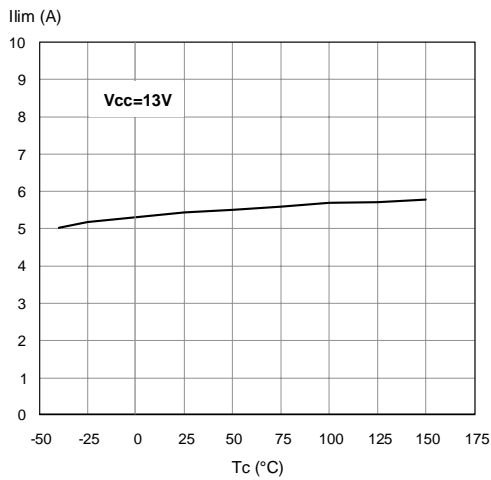
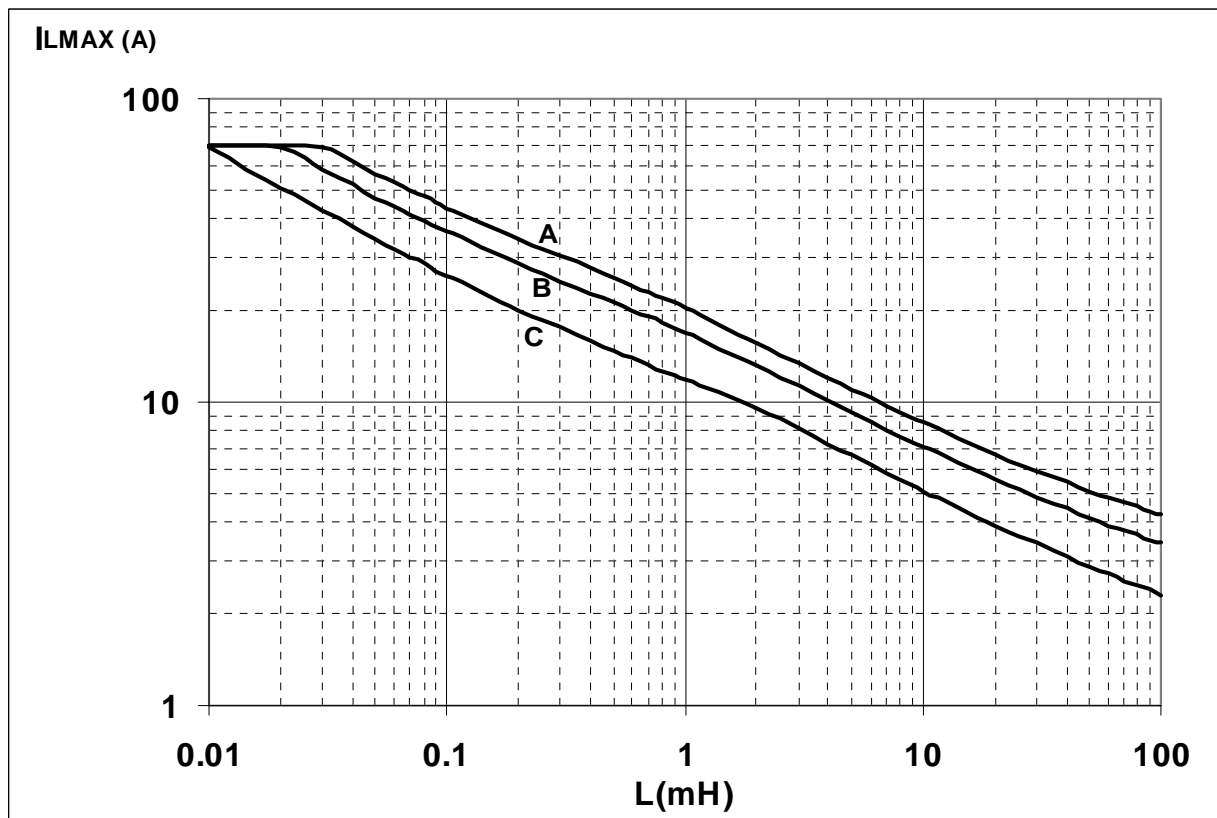


Figure 27. Maximum turn off current versus load inductance



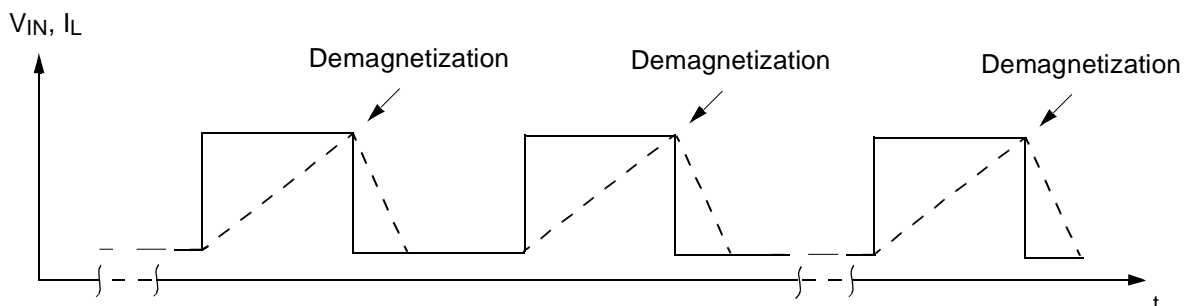
- A = Single Pulse at  $T_{Jstart}=150^{\circ}C$
- B= Repetitive pulse at  $T_{Jstart}=100^{\circ}C$
- C= Repetitive Pulse at  $T_{Jstart}=125^{\circ}C$

Values are generated with  $R_L=0\Omega$

In case of repetitive pulses,  $T_{Jstart}$  (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves B and C.

Conditions:

$V_{CC}=13.5V$



PowerSO-10™ Thermal Data

Figure 28. PowerSO-10™ PC Board

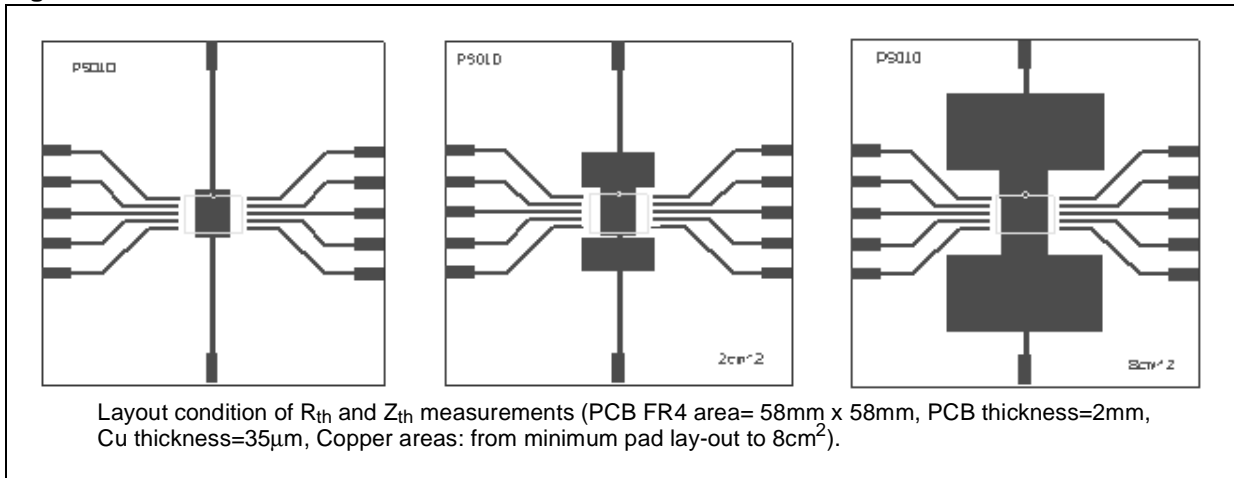


Figure 29. R<sub>thj-amb</sub> Vs PCB copper area in open box free air condition

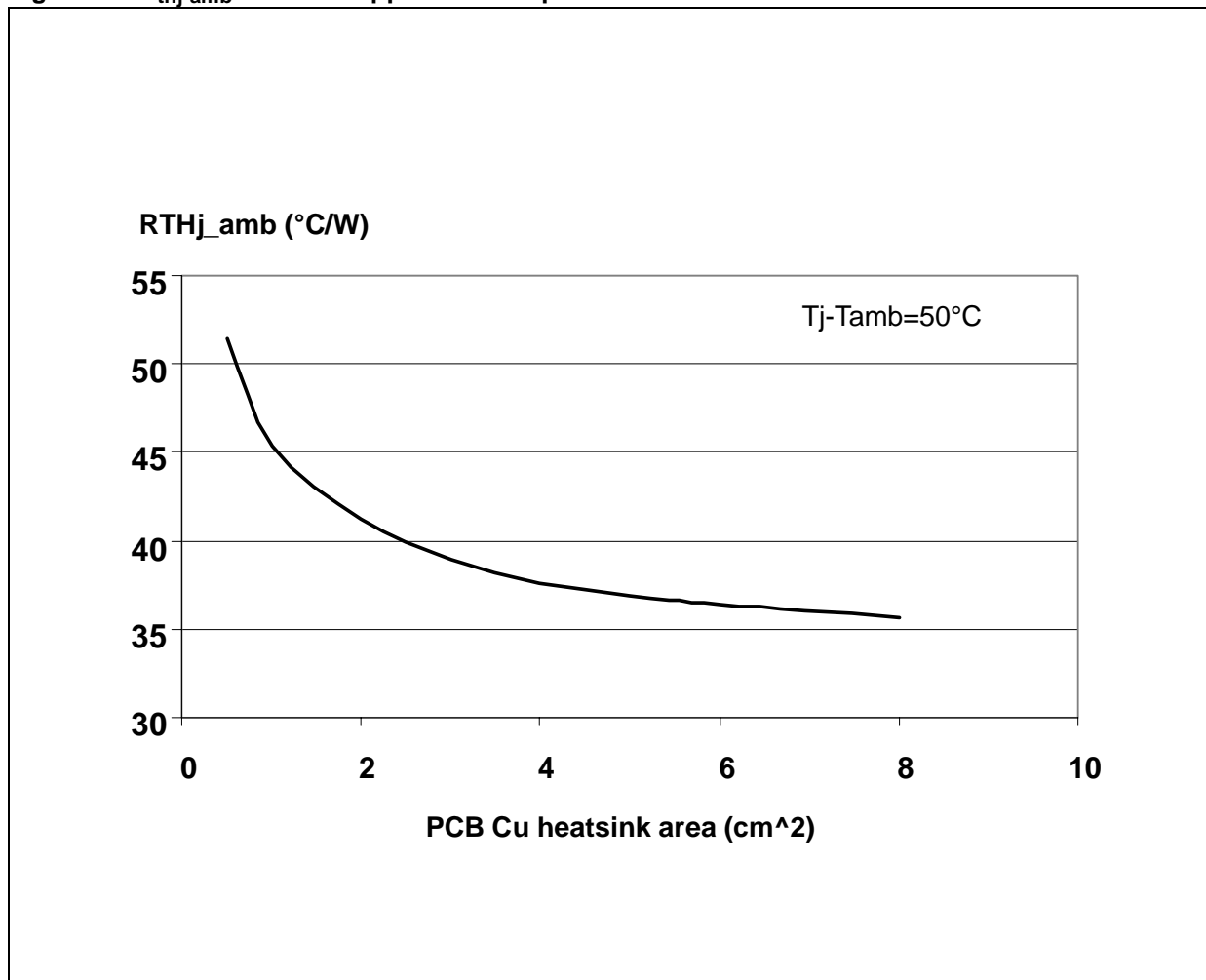


Figure 30. PowerSO-10 Thermal Impedance Junction Ambient Single Pulse

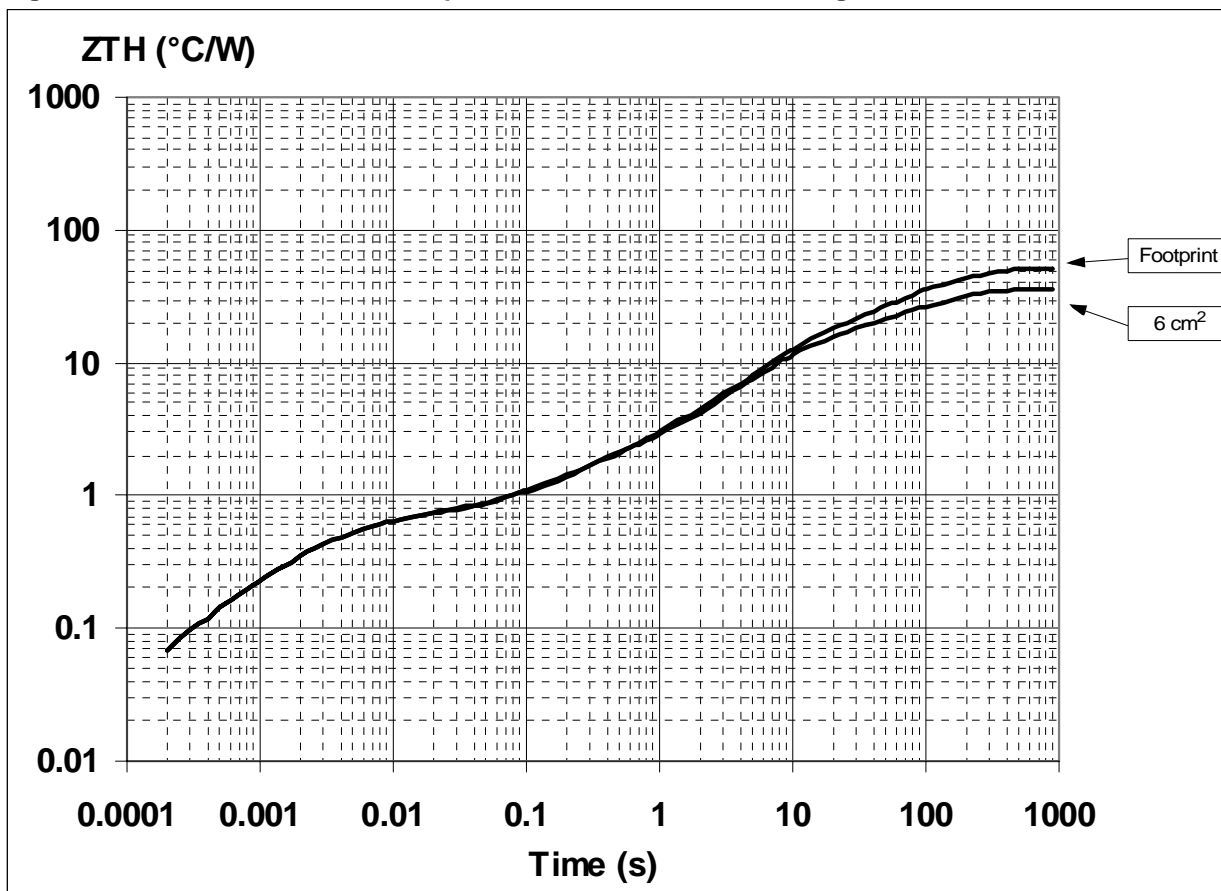
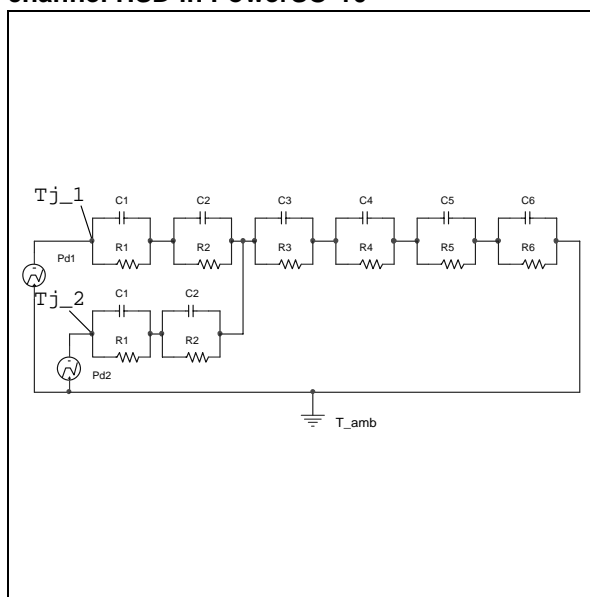


Figure 31. Thermal fitting model of a double channel HSD in PowerSO-10



Pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where  $\delta = t_p/T$

Table 14. Thermal Parameter

	Area/island (cm <sup>2</sup> )	Footprint	6
R1 (°C/W)		0.05	
R2 (°C/W)		0.3	
R3 (°C/W)		0.3	
R4 (°C/W)		0.8	
R5 (°C/W)		12	
R6 (°C/W)		37	22
C1 (W.s/°C)		0.001	
C2 (W.s/°C)		5.00E-03	
C3 (W.s/°C)		0.02	
C4 (W.s/°C)		0.3	
C5 (W.s/°C)		0.75	
C6 (W.s/°C)		3	5



PACKAGE MECHANICAL

Table 15. PowerSO-10™ Mechanical Data

Symbol	millimeters		
	Min	Typ	Max
A	3.35		3.65
A (*)	3.4		3.6
A1	0.00		0.10
B	0.40		0.60
B (*)	0.37		0.53
C	0.35		0.55
C (*)	0.23		0.32
D	9.40		9.60
D1	7.40		7.60
E	9.30		9.50
E2	7.20		7.60
E2 (*)	7.30		7.50
E4	5.90		6.10
E4 (*)	5.90		6.30
e		1.27	
F	1.25		1.35
F (*)	1.20		1.40
H	13.80		14.40
H (*)	13.85		14.35
h		0.50	
L	1.20		1.80
L (*)	0.80		1.10
a	0°		8°
α (*)	2°		8°

Note: (\*) Muar only POA P013P

Figure 32. PowerSO-10™ Package Dimensions

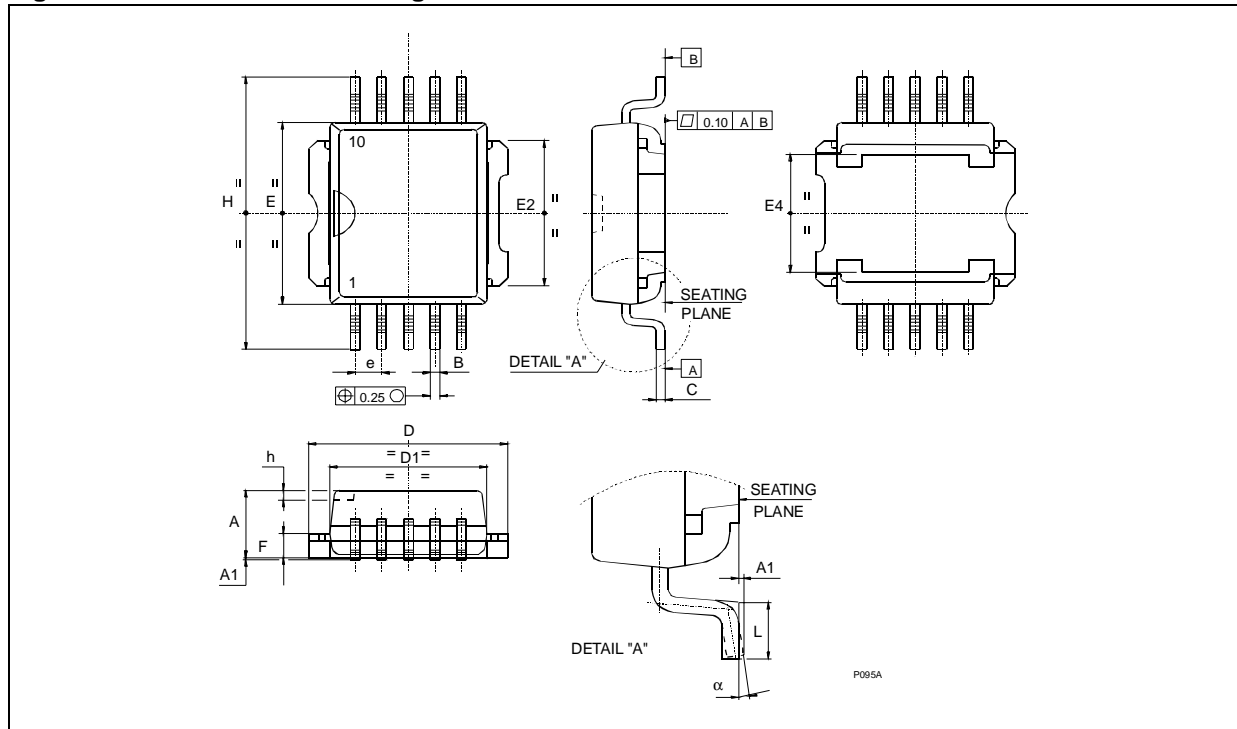


Figure 33. PowerSO-10™ Suggested Pad Layout And Tube Shipment (No Suffix)

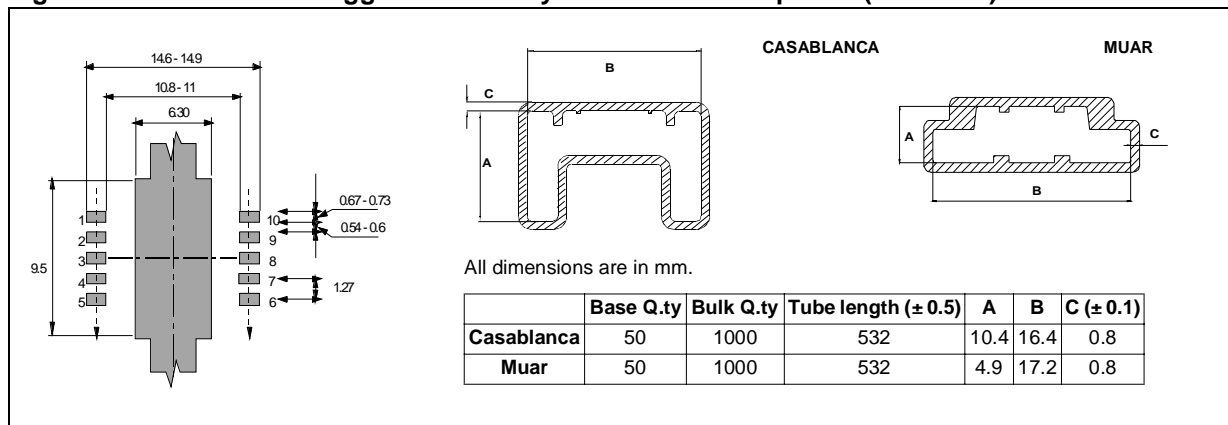
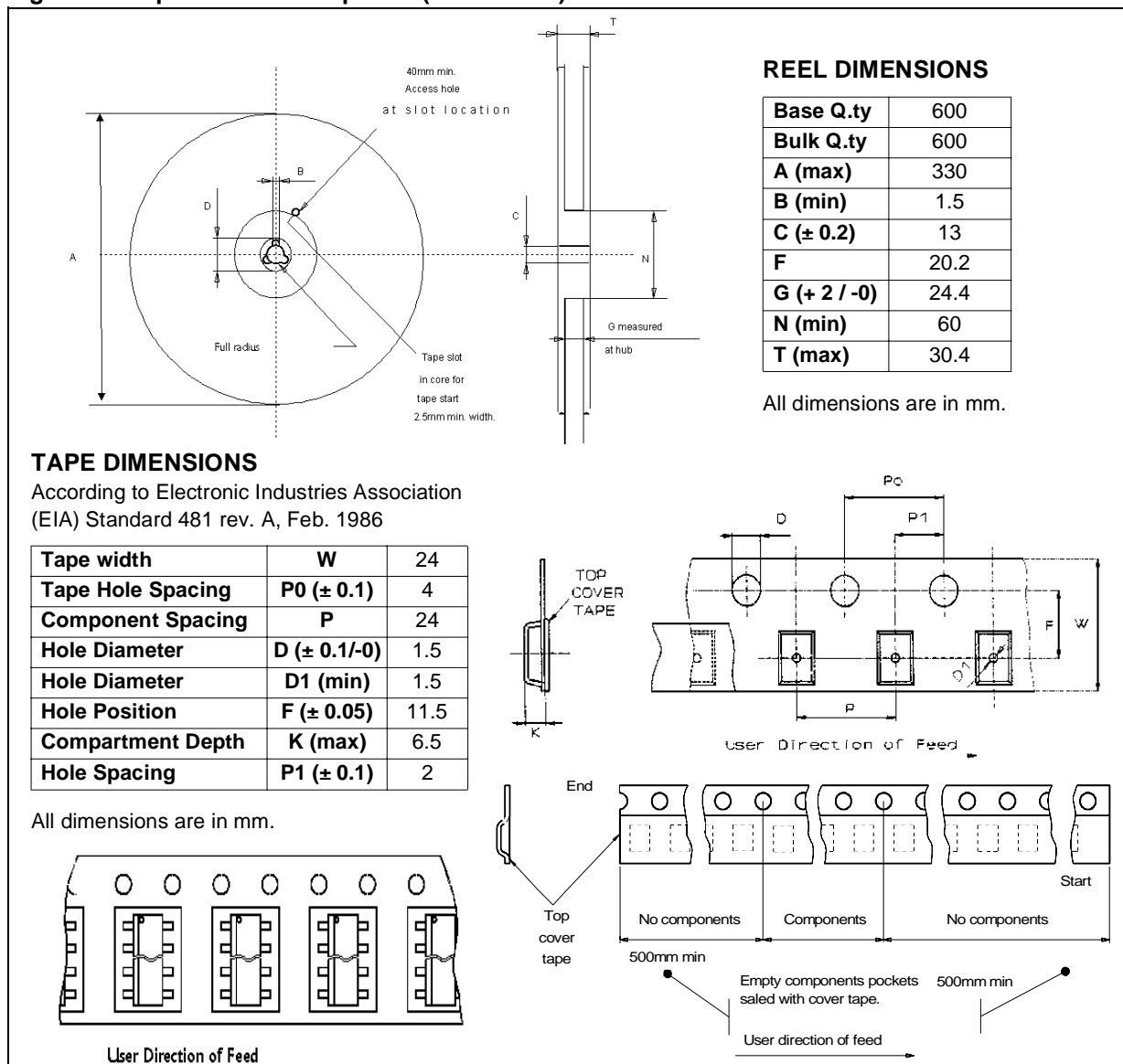


Figure 34. Tape And Reel Shipment (suffix “TR”)



**REVISION HISTORY**

<b>Date</b>	<b>Revision</b>	<b>Description of Changes</b>
Oct. 2004	1	- First Issue.

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