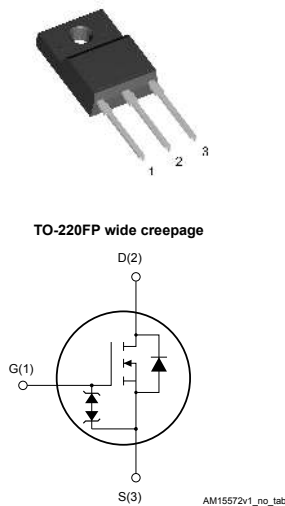


N-channel 600 V, 0.55 Ω typ., 7.5 A MDmesh M2 Power MOSFET in a TO-220FP wide creepage package



Features

Order code	V_{DS} at $T_{Jmax.}$	$R_{DS(on)}$ max.	I_D
STFH10N60M2	650 V	0.60 Ω	7.5 A

- Extremely low gate charge
- Excellent output capacitance (C_{OSS}) profile
- 100% avalanche tested
- Zener-protected
- Wide distance of 4.25 mm between the pins

Applications

- Switching applications
- LLC converters, resonant converters

Description

This device is an N-channel Power MOSFET developed using MDmesh M2 technology. Thanks to its strip layout and an improved vertical structure, the device exhibits low on-resistance and optimized switching characteristics, rendering it suitable for the most demanding high efficiency converters.

The TO-220FP wide creepage package provides increased surface insulation for Power MOSFETs to prevent failure due to arcing, which can occur in polluted environments.



Product status link

[STFH10N60M2](#)

Product summary

Order code	STFH10N60M2
Marking	10N60M2
Package	TO-220FP wide creepage
Packing	Tube

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	±25	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ °C}$	7.5	A
	Drain current (continuous) at $T_C = 100\text{ °C}$	4.9	
$I_{DM}^{(2)}$	Drain current (pulsed)	30	A
P_{TOT}	Total power dissipation at $T_C = 25\text{ °C}$	25	W
$dv/dt^{(3)}$	Peak diode recovery voltage slope	15	V/ns
$dv/dt^{(4)}$	MOSFET dv/dt ruggedness	50	
$V_{ISO}^{(5)}$	Insulation withstand voltage (RMS) from all three leads to external heat sink	2500	V
T_{stg}	Storage temperature range	-55 to 150	°C
T_j	Operating junction temperature range		

- Limited by package.
- Pulse limited by safe operating area.
- $I_{SD} \leq 7.5\text{ A}$, $di/dt \leq 400\text{ A}/\mu\text{s}$; $V_{DS\text{ peak}} < V_{(BR)DSS}$, $V_{DD} = 400\text{ V}$
- $V_{DS} \leq 480\text{ V}$.
- $t = 1\text{ s}$; $T_C = 25\text{ °C}$.

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	5	°C/W
R_{thJA}	Thermal resistance, junction-to-ambient	62.5	

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
$I_{AR}^{(1)}$	Avalanche current, repetitive or not repetitive	1.5	A
$E_{AS}^{(2)}$	Single pulse avalanche energy	110	mJ

- Pulse width limited by T_{jmax} .
- Starting $T_j = 25\text{ °C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$.

2 Electrical characteristics

($T_{\text{case}} = 25\text{ °C}$ unless otherwise specified)

Table 4. Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(\text{BR})\text{DSS}}$	Drain-source breakdown voltage	$V_{\text{GS}} = 0\text{ V}$, $I_{\text{D}} = 1\text{ mA}$	600			V
I_{DSS}	Zero gate voltage drain current	$V_{\text{GS}} = 0\text{ V}$, $V_{\text{DS}} = 600\text{ V}$			1	μA
		$V_{\text{GS}} = 0\text{ V}$, $V_{\text{DS}} = 600\text{ V}$, $T_{\text{case}} = 125\text{ °C}^{(1)}$			100	
I_{GSS}	Gate-body leakage current	$V_{\text{DS}} = 0\text{ V}$, $V_{\text{GS}} = \pm 25\text{ V}$			± 10	μA
$V_{\text{GS}(\text{th})}$	Gate threshold voltage	$V_{\text{DS}} = V_{\text{GS}}$, $I_{\text{D}} = 250\text{ }\mu\text{A}$	2	3	4	V
$R_{\text{DS}(\text{on})}$	Static drain-source on-resistance	$V_{\text{GS}} = 10\text{ V}$, $I_{\text{D}} = 3\text{ A}$		0.55	0.60	Ω

1. Defined by design, not subject to production test.

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iSS}	Input capacitance	$V_{\text{DS}} = 100\text{ V}$, $f = 1\text{ MHz}$, $V_{\text{GS}} = 0\text{ V}$	-	400	-	μF
C_{oSS}	Output capacitance		-	22	-	
C_{rSS}	Reverse transfer capacitance		-	0.84	-	
$C_{\text{oSS eq.}}^{(1)}$	Equivalent output capacitance	$V_{\text{DS}} = 0\text{ to }480\text{ V}$, $V_{\text{GS}} = 0\text{ V}$	-	83	-	μF
R_{G}	Intrinsic gate resistance	$f = 1\text{ MHz}$, $I_{\text{D}} = 0\text{ A}$	-	6.4	-	Ω
Q_{g}	Total gate charge	$V_{\text{DD}} = 480\text{ V}$, $I_{\text{D}} = 7.5\text{ A}$, $V_{\text{GS}} = 0\text{ to }10\text{ V}$ (see Figure 15. Test circuit for gate charge behavior)	-	13.5	-	nC
Q_{gs}	Gate-source charge		-	2.1	-	
Q_{gd}	Gate-drain charge		-	7.2	-	

1. $C_{\text{oSS eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oSS} when V_{DS} increases from 0 to 80% V_{DSS} .

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{\text{d}(\text{on})}$	Turn-on delay time	$V_{\text{DD}} = 300\text{ V}$, $I_{\text{D}} = 3.75\text{ A}$, $R_{\text{G}} = 4.7\text{ }\Omega$, $V_{\text{GS}} = 10\text{ V}$ (see Figure 14. Test circuit for resistive load switching times and Figure 19. Switching time waveform)	-	8.8	-	ns
t_{r}	Rise time		-	8	-	
$t_{\text{d}(\text{off})}$	Turn-off delay time		-	32.5	-	
t_{f}	Fall time		-	13.2	-	

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}^{(1)}$	Source-drain current		-		7.5	A
$I_{SDM}^{(2)}$	Source-drain current (pulsed)		-		30	A
$V_{SD}^{(3)}$	Forward on voltage	$V_{GS} = 0\text{ V}$, $I_{SD} = 7.5\text{ A}$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 7.5\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 60\text{ V}$ (see) Figure 16. Test circuit for inductive load switching and diode recovery times	-	270		ns
Q_{rr}	Reverse recovery charge		-	2		μC
I_{RRM}	Reverse recovery current		-	14.4		A
t_{rr}	Reverse recovery time	$I_{SD} = 7.5\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 60\text{ V}$, $T_j = 150\text{ }^\circ\text{C}$ (see) Figure 16. Test circuit for inductive load switching and diode recovery times	-	376		ns
Q_{rr}	Reverse recovery charge		-	2.8		μC
I_{RRM}	Reverse recovery current		-	15		A

1. Limited by package.
2. Pulse width is limited by safe operating area.
3. Pulse test: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics curves

Figure 1. Safe operating area

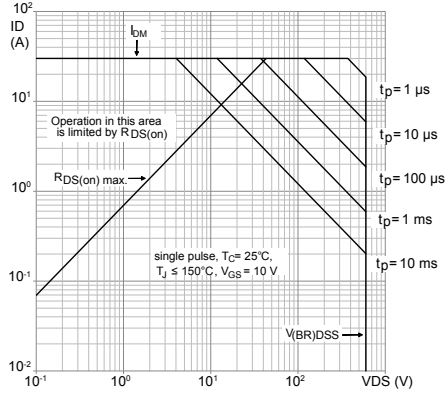


Figure 2. Maximum transient thermal impedance

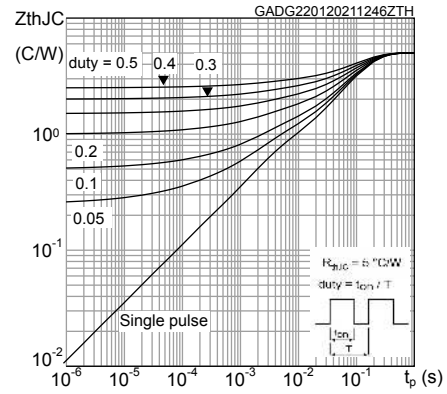


Figure 3. Output characteristics

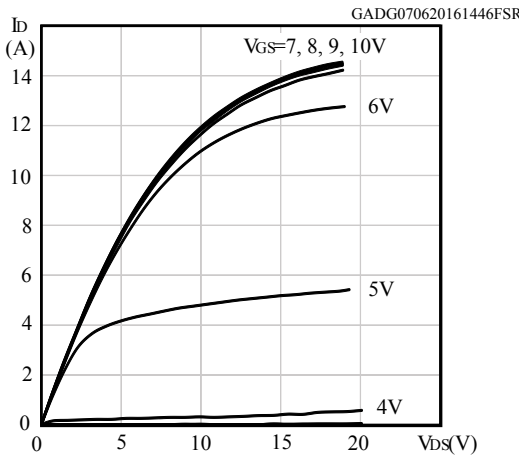


Figure 4. Transfer characteristics

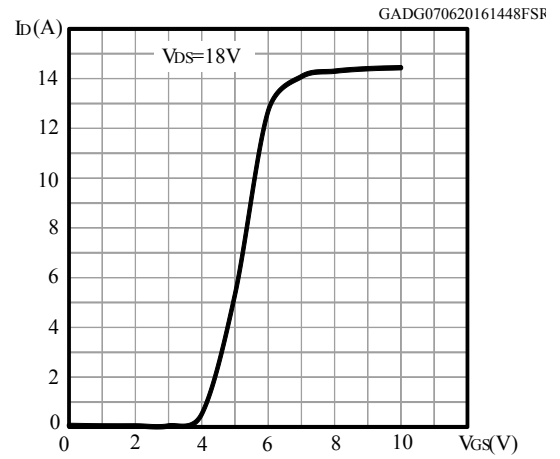


Figure 5. Gate charge vs gate-source voltage

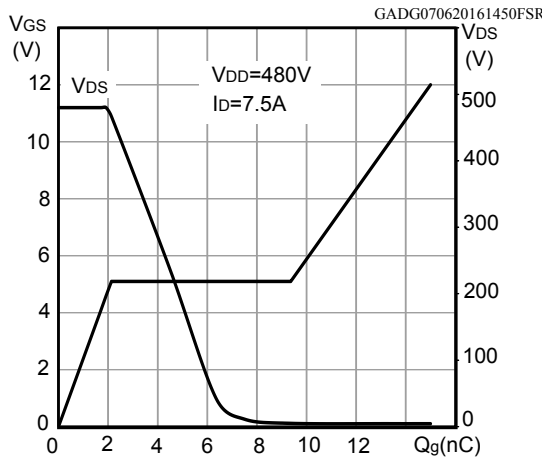


Figure 6. Static drain-source on-resistance

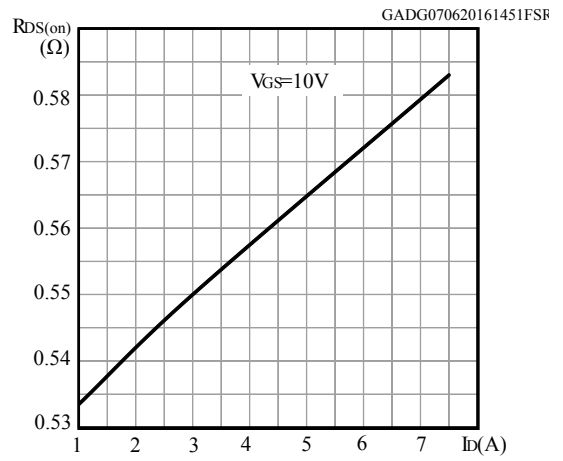


Figure 7. Capacitance variations

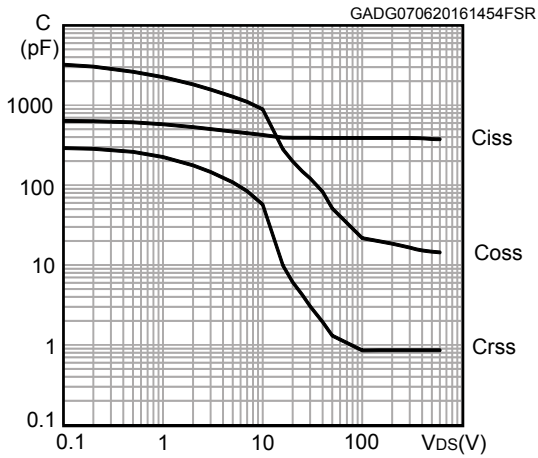


Figure 8. Normalized gate threshold voltage vs temperature

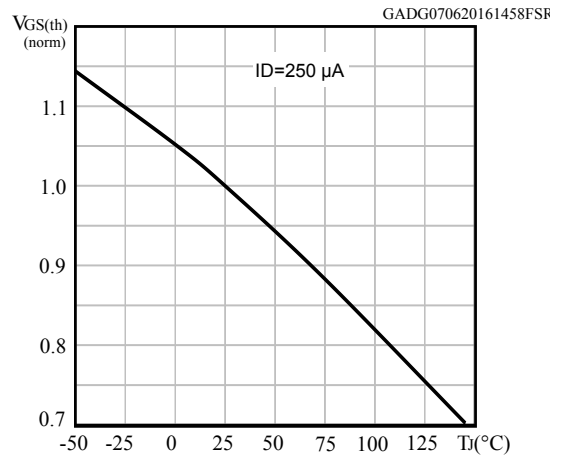


Figure 9. Normalized on-resistance vs temperature

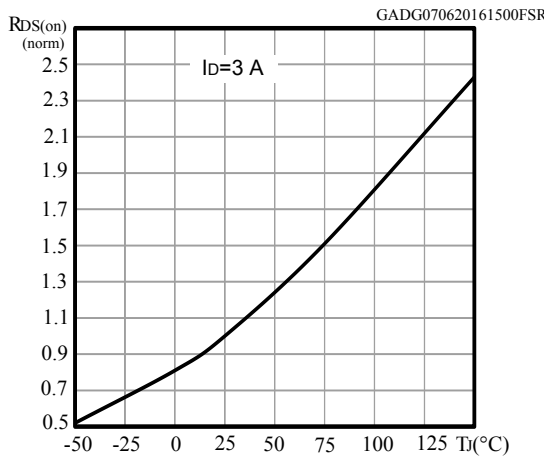


Figure 10. Source-drain diode forward characteristics

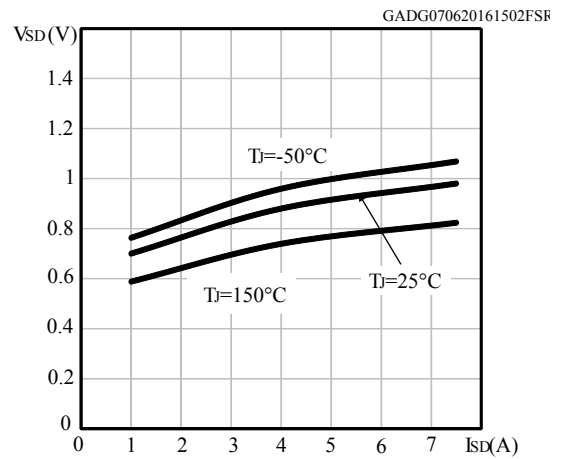


Figure 11. Normalized $V_{(BR)DSS}$ vs temperature

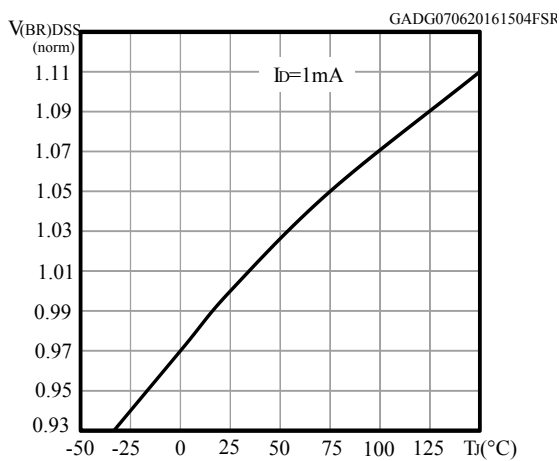
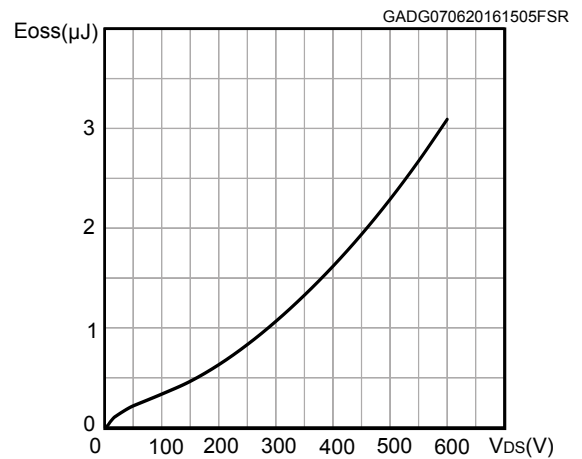
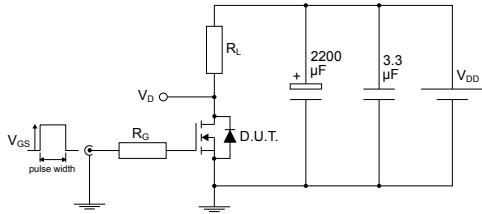


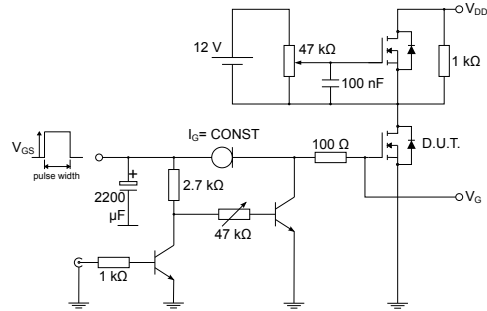
Figure 12. Output capacitance stored energy



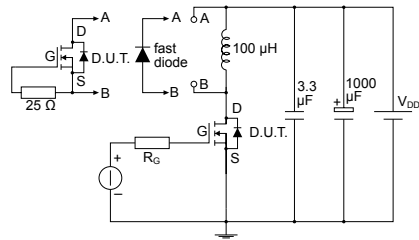
3 Test circuits

Figure 13. Test circuit for resistive load switching times


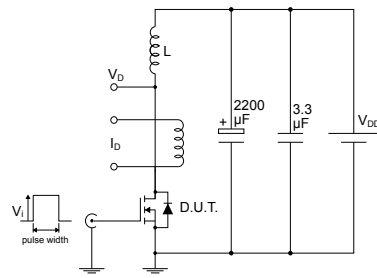
AM01468v1

Figure 14. Test circuit for gate charge behavior


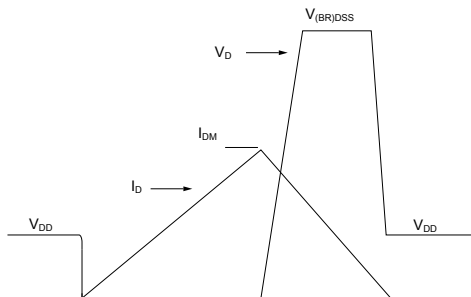
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Figure 15. Test circuit for inductive load switching and diode recovery times


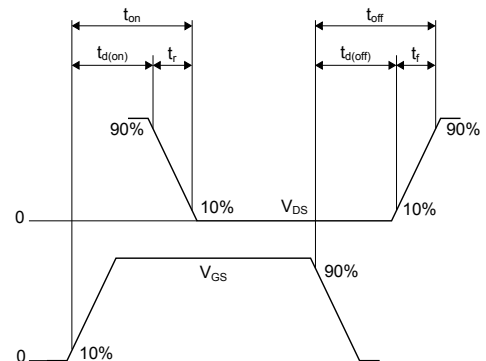
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Figure 16. Unclamped inductive load test circuit


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Figure 17. Unclamped inductive waveform


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Figure 18. Switching time waveform


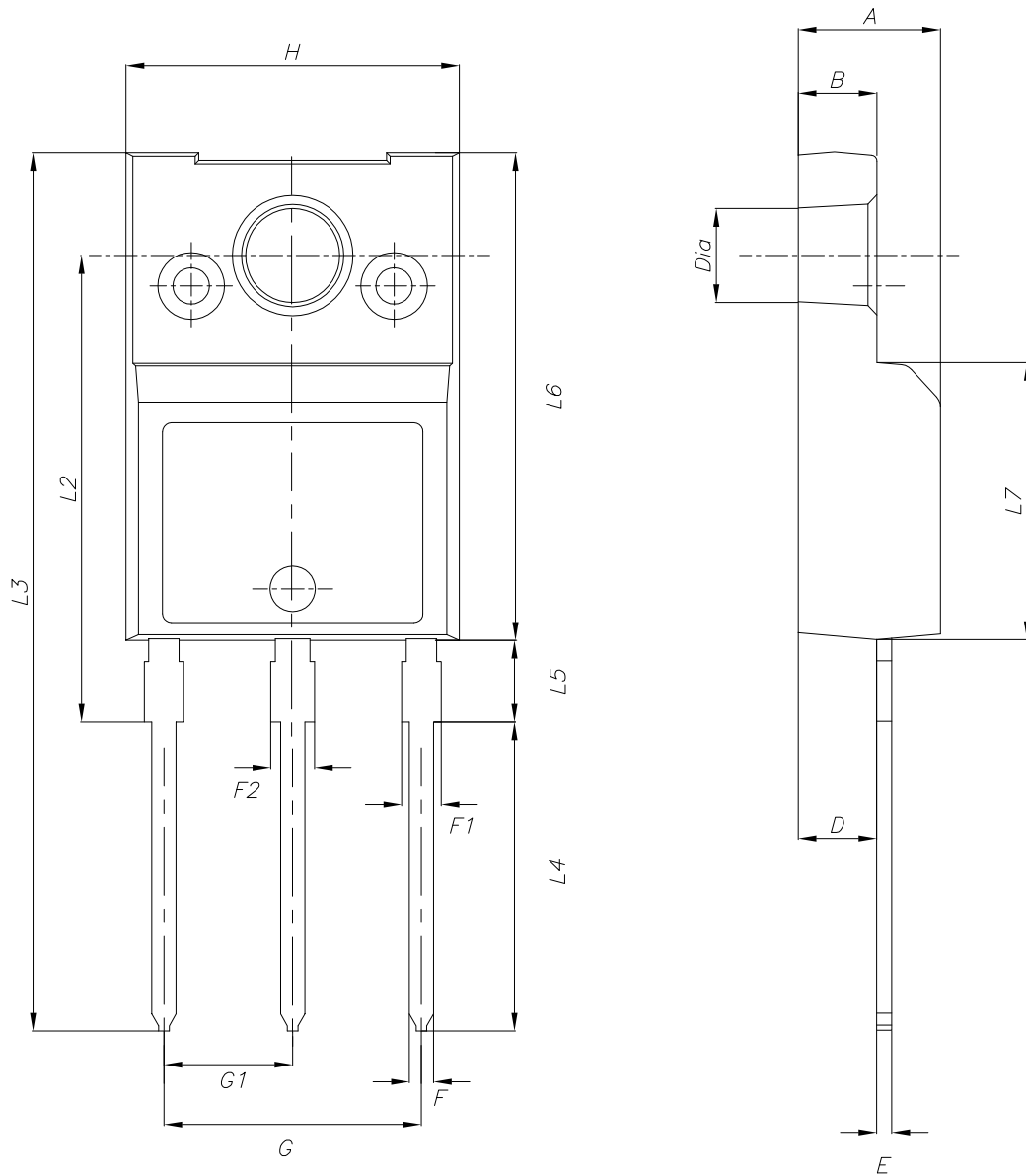
AM01473v1

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 TO-220FP wide creepage package information

Figure 19. TO-220FP wide creepage package outline



DM00260252_1

Table 8. TO-220FP wide creepage package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.60	4.70	4.80
B	2.50	2.60	2.70
D	2.49	2.59	2.69
E	0.46		0.59
F	0.76		0.89
F1	0.96		1.25
F2	1.11		1.40
G	8.40	8.50	8.60
G1	4.15	4.25	4.35
H	10.90	11.00	11.10
L2	15.25	15.40	15.55
L3	28.70	29.00	29.30
L4	10.00	10.20	10.40
L5	2.55	2.70	2.85
L6	16.00	16.10	16.20
L7	9.05	9.15	9.25
Dia	3.00	3.10	3.20

Revision history

Table 9. Document revision history

Date	Revision	Changes
07-Jun-2016	1	First release.
16-Jun-2016	2	Document status promoted from preliminary data to production data. Minor text changes.
18-Aug-2016	3	Modified: title and $R_{DS(on)}$ in cover page Modified: <i>Table 5: "On /off states"</i> and <i>Table 7: "Switching times"</i> Minor text changes
08-May-2017	4	Modified features on cover page. Modified Table 1 and Table 3. Minor text changes.
29-Jan-2021	5	Updated Figure 1 and Figure 2 . Minor text changes.

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