12-Bit Serial Input Multiplying DAC

AD5441

FEATURES

2.5 V to 5.5 V supply operation
True 12-bit accuracy
5 V operation @ <1 µA
Fast 3-wire serial input
Fast 5 µs settling time
1.9 MHz, 4-quadrant multiply BW
Upgrade for DAC8043 and DAC8043A
Standard and rotated pinout

APPLICATIONS

Ideal for PLC applications in industrial control
Programmable amplifiers and attenuators
Digitally controlled calibration and filters
Motion control systems

GENERAL DESCRIPTION

The AD5441 is an improved high accuracy 12-bit multiplying digital-to-analog converter (DAC) in space-saving 8-lead packages. Featuring serial input, double buffering, and excellent analog performance, the AD5441 is ideal for applications where PC board space is at a premium. Improved linearity and gain error performance permit reduced part counts through the elimination of trimming components. Separate input clock and load DAC control lines allow full user control of data loading and analog output.

The circuit consists of a 12-bit serial-in/parallel-out shift register, a 12-bit DAC register, a 12-bit CMOS DAC, and control logic. Serial data is clocked into the input register on the rising edge of the clock pulse. When the new data-word is clocked in, it is loaded into the DAC register with the $\overline{LD}$ input pin. Data in the DAC register is converted to an output current by the DAC.

Consuming only 1 µA from a single 5 V power supply, the AD5441 is the ideal low power, small size, high performance solution to many application problems.

The AD5441 is specified over the extended industrial (−40°C to +125°C) temperature range. It is available in an 8-lead LFCSP and an 8-lead MSOP.

FUNCTIONAL BLOCK DIAGRAM

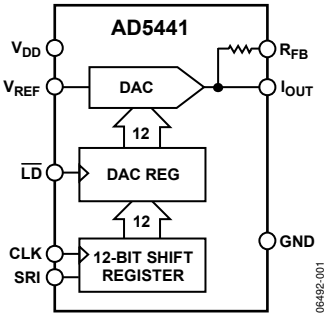

Figure 1.

Rev. A

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REVISION HISTORY

3/11—Rev. 0 to Rev. A

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1/08—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

V_{DD} = 5 V, V_{REF} = 10 V, −40°C < T_A < +155°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Condition
STATIC PERFORMANCE						
Resolution	N			12	Bits	
Relative Accuracy	INL			±0.5	LSB	
Differential Nonlinearity	DNL			±0.5	LSB	All grades monotonic to 12 bits
Gain Error	G_{FSE}			±1	LSB	Data = FFF_H
Gain Temperature Coefficient[1]	TCG_{FS}			±5	ppm/°C	I_{OUT} pin measured
Output Leakage Current	I_{LKG}			±5	nA	Data = 000_H, I_{OUT} pin measured
				±25	nA	T_A = −40°C, +125°C, data = 000_H, I_{OUT} pin measured
Zero-Scale Error	I_{ZSE}			±0.03	LSB	Data = 000_H
				±0.15	LSB	T_A = −40°C, +125°C, data = 000_H
REFERENCE INPUT						
Input Resistance	R_{REF}	7		15	kΩ	Absolute temperature coefficient < 50 ppm/°C
Input Capacitance[1]	C_{REF}		5		pF	
ANALOG OUTPUT						
Output Capacitance[1]	C_{OUT}		1		pF	Data = 000_H
			4		pF	Data = FFF_H
DIGITAL INPUTS						
Digital Input Low	V_{IL}			0.8	V	
Digital Input High	V_{IH}	2.4			V	
Input Leakage Current	I_{IL}			1	µA	V_{LOGIC} = 0 V to 5 V
Input Capacitance[1]	C_{IL}		4.0		pF	V_{LOGIC} = 0 V
AC CHARACTERISTICS[1]						
Output Current Settling Time	t_S		5		µs	To ±0.01% of full-scale, external op amp OP42
				0.5	µs	To ±0.01% of full-scale, 100 Ω terminated to ground
DAC Glitch	Q		40		nVs	Data = 000_H to FFF_H to 000_H, V_{REF} = 0 V, OP42
				1	nVs	Data = 000_H to FFF_H to 000_H, V_{REF} = 0 V, 100 Ω
Digital Feedthrough			5		nV	Using external op amp OP42
Feedthrough (V_{OUT}/V_{REF})	FT		1.4		mV p-p	V_{REF} = 20 V p-p, data = 000_H, f = 10 kHz
Total Harmonic Distortion	THD		−85		dB	V_{REF} = 6 V rms, data = FFF_H, f = 1 kHz
Output Noise Density	e_n			17	nV/√Hz	10 Hz to 100 kHz between R_{FB} and I_{OUT}
Multiplying Bandwidth	BW		1.9		MHz	−3 dB, V_{OUT}/V_{REF}, V_{REF} = 100 mV rms, data = FFF_H
SUPPLY CHARACTERISTICS[1]						
Power Supply Range	$V_{DD\ RANGE}$	2.5		5.5	V	
Positive Supply Current	I_{DD}			10	µA	V_{LOGIC} = 0 V or V_{DD}
Power Dissipation	P_{DISS}	2.5		5.5	µW	V_{LOGIC} = 0 V or V_{DD}
Power Supply Sensitivity	PSS			0.002	%/%	ΔV_{DD} = ±5%

[1] These parameters are guaranteed by design and not subject to production testing.

TIMING CHARACTERISTICS

All input control signals are specified with $t_R = t_F = 2$ ns (10% to 90% of V_{DD}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$; V_{DD} + 2.5 V to 5.5 V, V_{REF} = 10 V; temperature range = −40°C to +125°C; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2. Timing Characteristics

Parameter	2.5 V	5.5 V	Unit	Conditions/Comments
t_{DS}	10	5	ns min	Data setup
t_{DH}	5	5	ns min	Data hold
t_{CH}	15	10	ns min	Clock width high
t_{CL}	15	10	ns min	Clock width low
t_{LD}	20	10	ns min	Load pulse width
t_{LD1}	0	0	ns min	$\overline{LD}$ DAC high to MSB CLK high
t_{ASB}	0	0	ns min	LSB CLK to $\overline{LD}$ DAC

Timing Diagrams

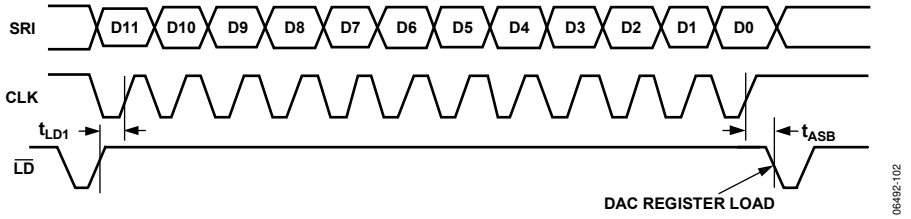

Figure 2. Full Data Transmission

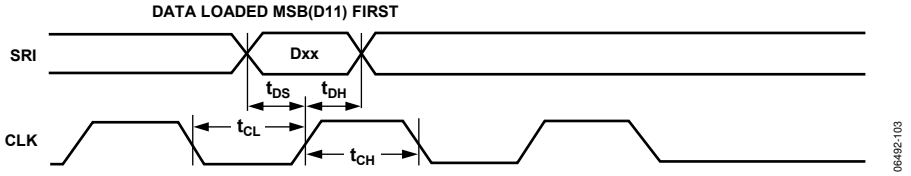

Figure 3. Bit Data Transmission

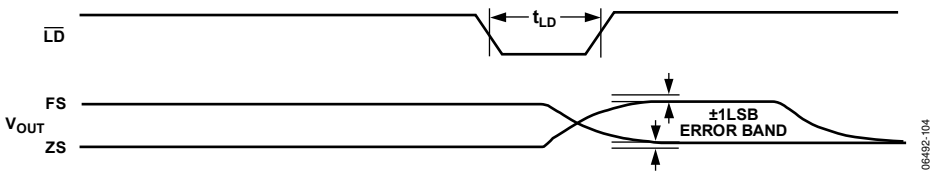

Figure 4. Output Transition

Table 3. Control Logic Truth Table

CLK	$\overline{LD}$	Serial Shift Register Function	DAC Register Function
↑ [1]	H	Shift register data advanced one bit	Latched
↑	L	Shift register data advanced one bit	Transparent
H or L	L	No effect	Updated with current shift register contents
L	↑ [1]	No effect	Latched all 12 bits

[1] ↑ equals positive logic transition.

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
V_{DD} to GND	−0.3 V, +8 V
V_{REF} to GND	±18 V
R_{FB} to GND	±18 V
Logic Inputs to GND	−0.3 V, V_{DD} + 0.3 V
I_{OUT} to GND	−0.3 V, V_{DD} + 0.3 V
I_{OUT} Short Circuit to GND	50 mA
Package Power Dissipation	$(T_J \text{ max} - T_A)/\theta_{JA}$
Maximum Junction Temperature (T_J max)	150°C
Operating Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 5.

Package Type	θ_{JA}	θ_{JC}	Unit
8-Lead MSOP	142	44	°C/W
8-Lead LFCSP[1]	75	18	°C/W

[1] Exposed pad soldered to the ground plane.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

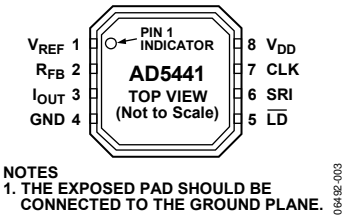

Figure 5. 8-Lead LFCSP Pin Configuration

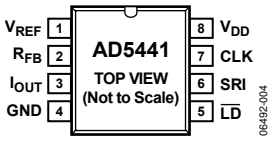

Figure 6. 8-Lead MSOP Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{REF}	DAC Reference Input Pin. Establishes DAC full-scale voltage. Constant input resistance vs. code.
2	R_{FB}	Internal Matching Feedback Resistor. Connect to external op amp output.
3	I_{OUT}	DAC Current Output, full-scale output 1 LSB less than reference input voltage $-V_{REF}$.
4	GND	Analog and Digital Ground.
5	$\overline{LD}$	Load Strobe, Level-Sensitive Digital Input. Transfers shift-register data to DAC register while active low. See Table 3 for operation.
6	SRI	12-Bit Serial Register Input. Data loads directly into the shift register MSB first. Extra leading bits are ignored.
7	CLK	Clock Input. Positive-edge clocks data into shift register.
8	V_{DD}	Positive Power Supply Input. Specified range of operation 5 V ± 10%.
	EP	Exposed Pad. The exposed pad should be connected to the ground plane.

TYPICAL PERFORMANCE CHARACTERISTICS

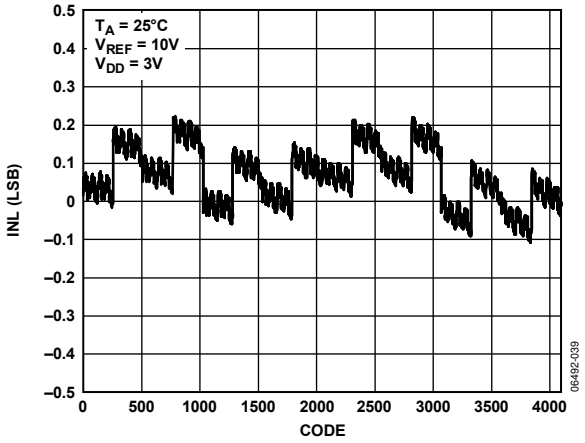

Figure 7. INL vs. Code, 3 V

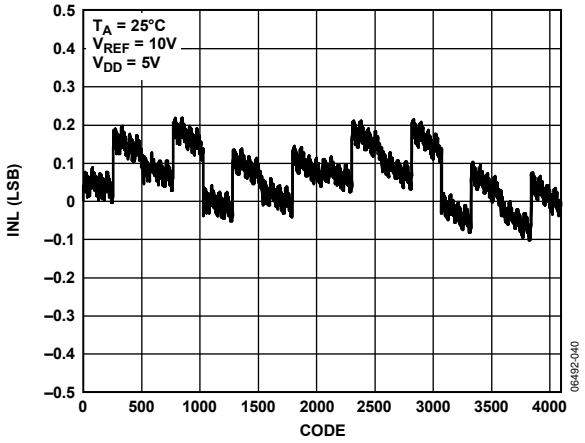

Figure 10. INL vs. Code, 5 V

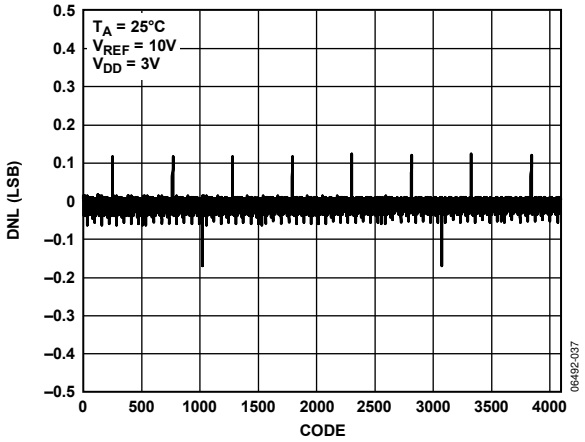

Figure 8. DNL vs. Code, 3 V

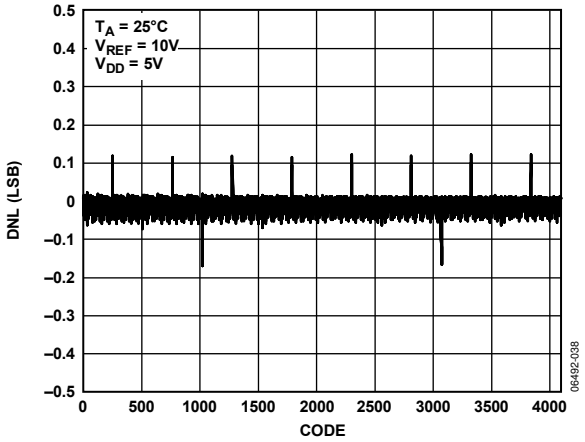

Figure 11. DNL vs. Code, 5 V

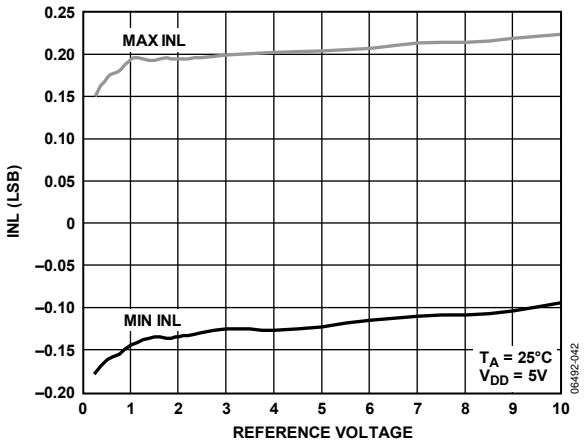

Figure 9. INL vs. Reference, 5 V

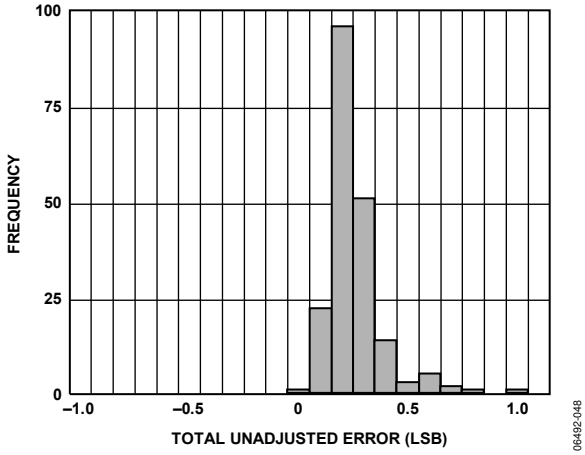

Figure 12. Total Unadjusted Error Histogram

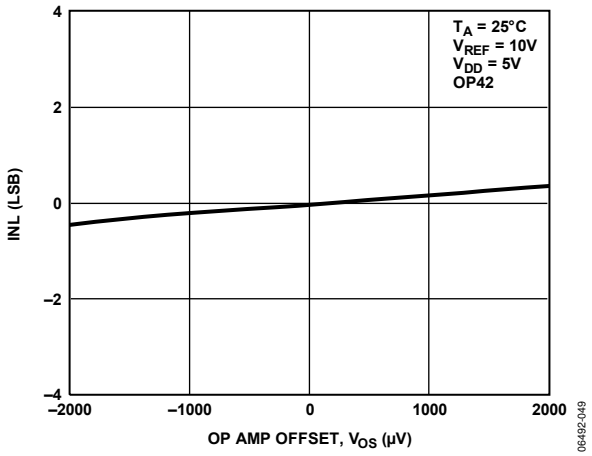

Figure 13. Integral Nonlinearity Error vs. External Op Amp

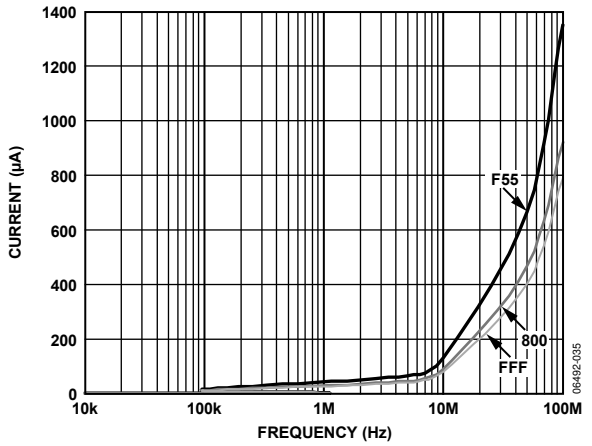

Figure 14. Supply Current vs. Clock Frequency

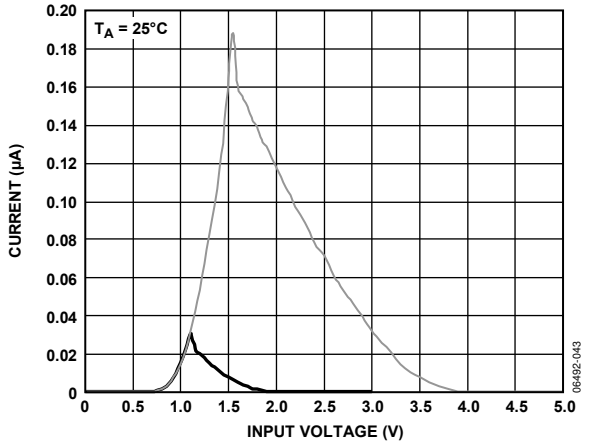

Figure 15. Supply Current vs. Logic Input Voltage

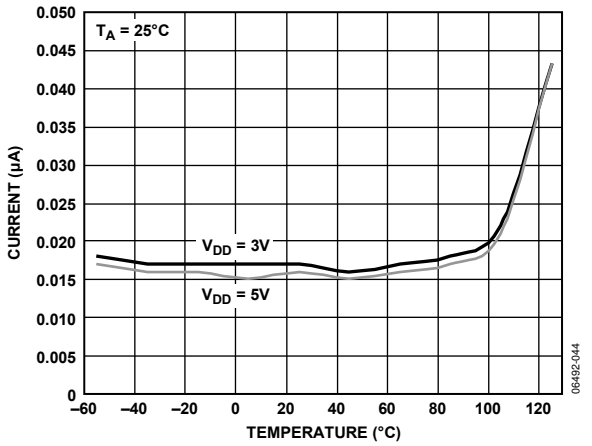

Figure 16. Supply Current vs. Temperature

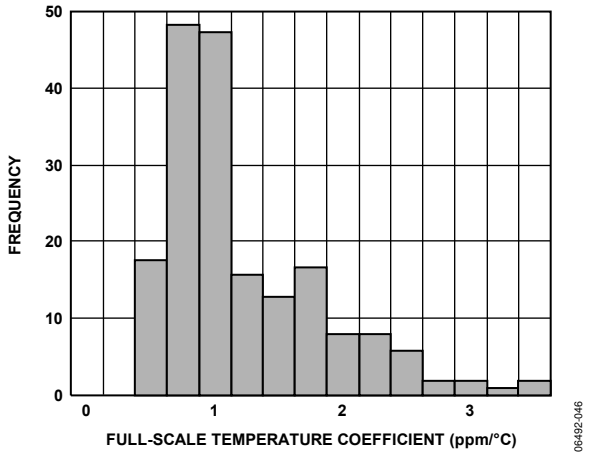

Figure 17. Full-Scale Output Temperature Coefficient Histogram

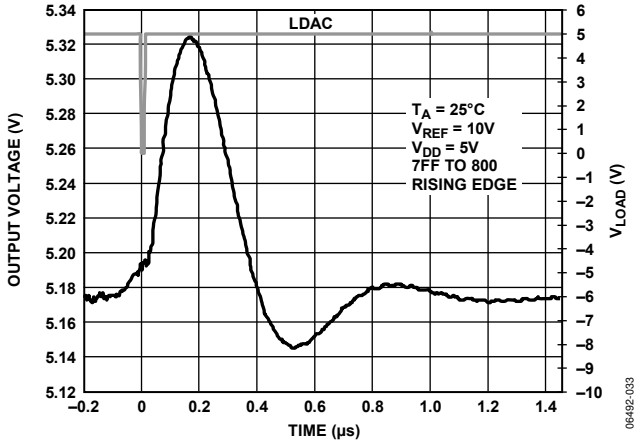

Figure 18. Midscale Transitions

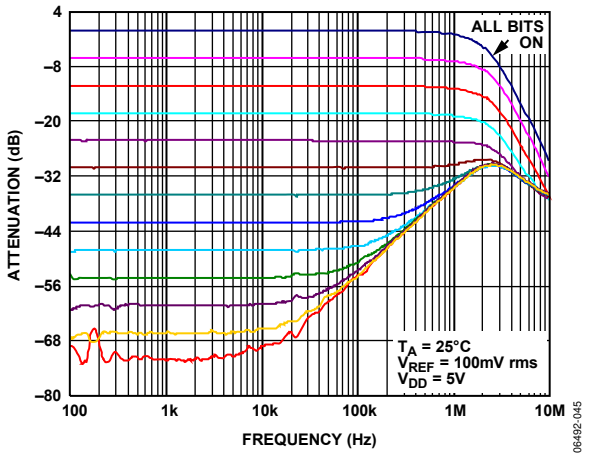

Figure 19. Reference Multiplying Bandwidth

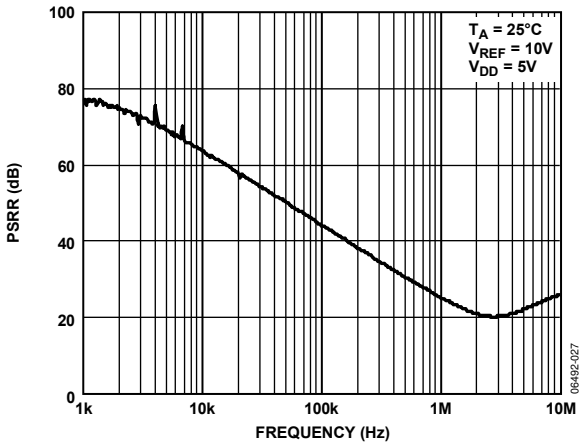

Figure 20. PSRR vs. Frequency

TERMINOLOGY

Relative Accuracy (INL)
Relative accuracy or endpoint nonlinearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for zero and full scale and is normally expressed in LSBs or as a percentage of the full-scale reading.

Differential Nonlinearity (DNL)
DNL is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of −1 LSB maximum over the operating temperature range ensures monotonicity.

Gain Error
Gain error or full-scale error is a measure of the output error between an ideal DAC and the actual device output. For these DACs, ideal maximum output is V_{REF} − 1 LSB. Gain error of the DACs is adjustable to zero with external resistance.

Zero Scale Error
Calculated from worst-case R_{REF}

$$I_{ZSE}(\text{LSB}) = (R_{REF} \times I_{LKG} \times 4096)/V_{REF}.$$

Output Leakage Current
Output leakage current is the current that flows into the DAC ladder switches when they are turned off. For the I_{OUT} terminal, it can be measured by loading all 0s to the DAC and measuring the I_{OUT} current.

Output Capacitance
Capacitance from $I_{OUT}1$ to AGND.

Digital-to-Analog Glitch Impulse
The amount of charge injected from the digital inputs to the analog output when the inputs change state. This is normally specified as the area of the glitch in either pA-s or nV-s, depending on whether the glitch is measured as a current or voltage signal.

Digital Feedthrough
When the device is not selected, high frequency logic activity on the digital inputs of the device may be capacitively coupled through the device and produce noise on the I_{OUT} pins. This noise is coupled from the outputs of the device onto follow-on circuitry. This noise is digital feedthrough.

Multiplying Feedthrough Error
This is the error due to capacitive feedthrough from the DAC reference input to the DAC $I_{OUT}1$ terminal when all 0s are loaded to the DAC.

Total Harmonic Distortion (THD)
The DAC is driven by an ac reference. The ratio of the rms sum of the harmonics of the DAC output to the fundamental value is the THD. Usually only the lower order harmonics, such as second to fifth, are included.

$$THD = 20\log\frac{\sqrt{V2^2 + V3^2 + V4^2 + V5^2}}{V1}$$

Compliance Voltage Range
The maximum range of (output) terminal voltage for which the device provides the specified characteristics.

Output Noise Spectral Density

Calculation from

$$e_n = \sqrt{4KTRB}$$

where:
K is Boltzmann Constant (J/°K).
R is resistance (Ω).
T is the resistor temperature (°K).
B is the 1 Hz bandwidth.

PARAMETER DEFINITIONS

GENERAL CIRCUIT INFORMATION

The AD5441 is a 12-bit multiplying DAC with a low temperature coefficient. It contains an R-2R resistor ladder network, data input and control logic, and two data registers.

The digital circuitry forms an interface in which serial data can be loaded under microprocessor control into a 12-bit shift register and then transferred, in parallel, to the 12-bit DAC register.

The analog portion of the AD5441 contains an inverted R-2R ladder network consisting of silicon-chrome, highly stable (50 ppm/°C), thin-film resistors, and 12 pairs of NMOS current-steering switches, see Figure 21. These switches steer binarily weighted currents into either I_{OUT} or GND; this yields a constant current in each ladder leg, regardless of digital input code. This constant current results in a constant input resistance at V_{REF} equal to R. The V_{REF} input may be driven by any reference voltage or current, ac or dc, that is within the limits stated in the Absolute Maximum Ratings.

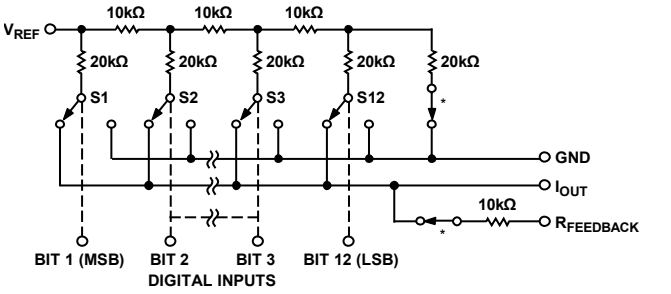

Figure 21. Simplified DAC Circuit

The 12 output current steering NMOS FET switches are in series with each R-2R resistor.

To further ensure accuracy across the full temperature range, MOS switches that are always on were included in series with the feedback resistor and the terminating resistor of the R-2R ladder. Figure 21 shows the location of the series switches.

During any testing of the resistor ladder or $R_{FEEDBACK}$ (such as incoming inspection), V_{DD} must be present to turn on these series switches.

OUTPUT IMPEDANCE

The output resistance of the AD5441, as in the case of the output capacitance, varies with the digital input code. This resistance, looking back into the I_{OUT} terminal, may be between 10 kΩ (the feedback resistor alone when all digital inputs are low) and 7.5 kΩ (the feedback resistor in parallel with approximate 30 kΩ of the R-2R ladder network resistance when any single bit logic is high). Static accuracy and dynamic performance are affected by these variations.

APPLICATIONS INFORMATION

In most applications, linearity depends upon the potential of the I_{OUT} and GND pins being at the same voltage potential. The DAC is connected to an external precision op amp inverting input. The external amplifiers noninverting input should be tied directly to ground without the usual bias current compensating resistor (see Figure 22 and Figure 24). The selected amplifier should have a low input bias current and low drift over temperature. The amplifiers input offset voltage should be nulled to less than 200 mV (less than 10% of 1 LSB). All grounded pins should tie to a single common ground point to avoid ground loops. The V_{DD} power supply should have a low noise level with adequate bypassing. It is best to operate the AD5441 from the analog power supply and grounds.

UNIPOLAR 2-QUADRANT MULTIPLYING

The most straightforward application of the AD5441 is in the 2-quadrant multiplying configuration shown in Figure 22. If the reference input signal is replaced with a fixed dc voltage reference, the DAC output provides a proportional dc voltage output according to the transfer equation

$$V_{OUT} = -D/4096 \times V_{REF}$$

where:
D is the decimal data loaded into the DAC register.
V_{REF} is the externally applied reference voltage source.

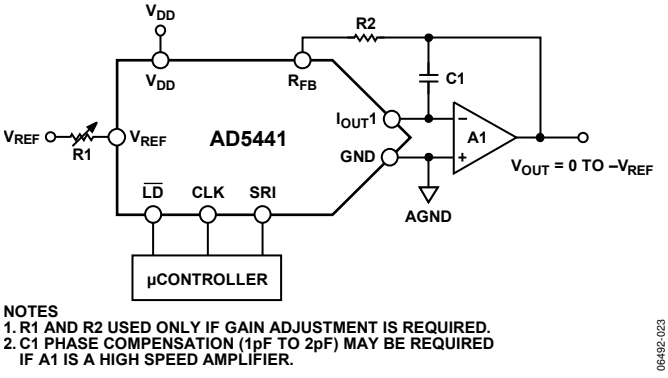

Figure 22. Unipolar (2-Quadrant) Operation

BIPOLAR 4-QUADRANT MULTIPLYING

Figure 24 shows a suggested circuit to achieve 4-quadrant multiplying operation. The summing amplifier multiplies V_{OUT1} by 2 and offsets the output with the reference voltage so that a midscale digital input code of 2048 places V_{OUT2} at 0 V. The negative full-scale voltage is V_{REF} when the DAC is loaded with all zeros. The positive full-scale output is $-(V_{REF} - 1\ LSB)$ when the DAC is loaded with all ones. Therefore, the digital coding is offset binary. The voltage output transfer equation for various input data and reference (or signal) values follows

$$V_{OUT2} = (D/2048 - 1) - V_{REF}$$

where:
D is the decimal data loaded into the DAC register.
V_{REF} is the externally applied reference voltage source.

INTERFACE LOGIC INFORMATION

The AD5441 has been designed for ease of operation. The timing diagram in Figure 2 illustrates the input register loading sequence. Note that the most significant bit (MSB) is loaded first. Once the 12-bit input register is full, the data is transferred to the DAC register by taking $\overline{LD}$ momentarily low.

DIGITAL SECTION

The digital inputs of the AD5441, SRI, $\overline{LD}$, and CLK, are TTL-compatible. The input voltage levels affect the amount of current drawn from the supply; peak supply current occurs as the digital input (V_{IN}) passes through the transition region. See Figure 15 for the supply current vs. logic input voltage graph. Maintaining the digital input voltage levels as close as possible to the supplies, V_{DD} and GND, minimizes supply current consumption. The digital inputs of the AD5441 were designed with ESD resistance incorporated through careful layout and the inclusion of input protection circuitry. Figure 23 shows the input protection diodes and series resistor; this input structure is duplicated on each digital input. High voltage static charges applied to the inputs are shunted to the supply and ground rails through forward-biased diodes. These protection diodes were designed to clamp the inputs to well below dangerous levels during static discharge conditions.

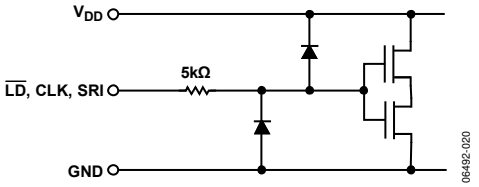

Figure 23. Digital Input Protection

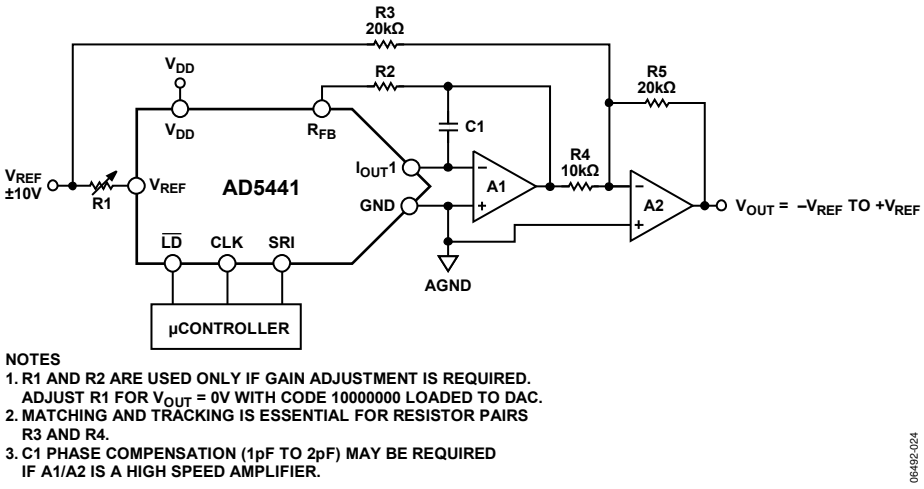

Figure 24. Bipolar (4-Quadrant) Operation

OUTLINE DIMENSIONS

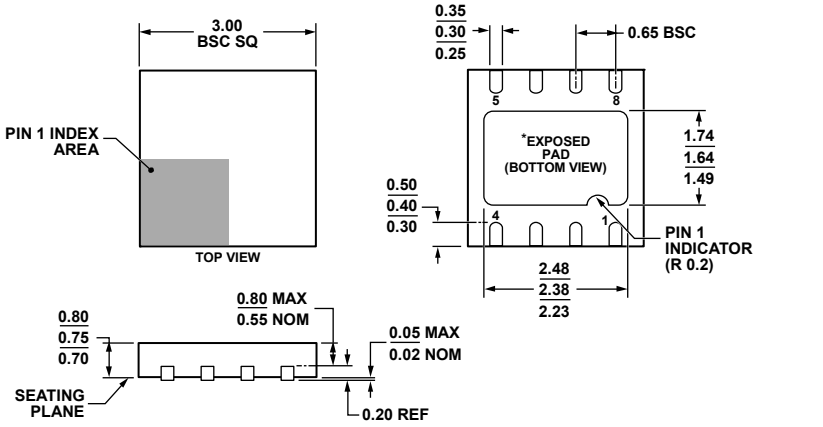

Figure 25. 8-Lead Lead Frame Chip Scale Package [LFCSP_WD]
3 mm × 3 mm Body, Very Very Thin, Dual Lead
(CP-8-3)
Dimensions are shown in millimeters

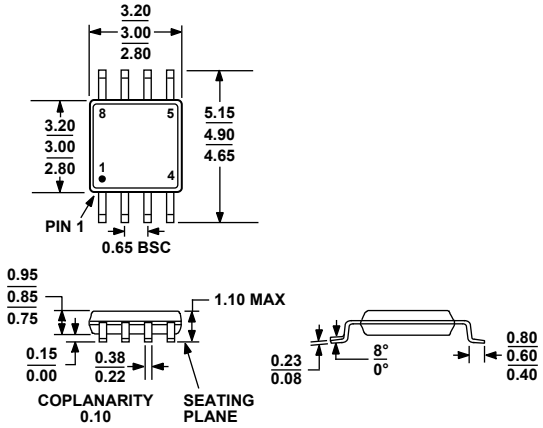

Figure 26. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions are shown in millimeters

ORDERING GUIDE

Model[1]	INL (LSB)	Temperature Range	Package Description	Package Option	Branding
AD5441BCPZ-R2	±0.5	−40°C to +125°C	8-Lead LFCSP_WD	CP-8-3	DBD
AD5441BCPZ-REEL7	±0.5	−40°C to +125°C	8-Lead LFCSP_WD	CP-8-3	DBD
AD5441BRMZ	±0.5	−40°C to +125°C	8-Lead MSOP	RM-8	DBC
AD5441BRMZ-REEL7	±0.5	−40°C to +125°C	8-Lead MSOP	RM-8	DBC

[1] Z = RoHS Compliant Part.

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