Burr-Brown Products
from Texas Instruments

OPA688

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SpeedPLUS™ Unity Gain Stable, Wideband VOLTAGE LIMITING AMPLIFIER

FEATURES

- HIGH LINEARITY NEAR LIMITING
- FAST RECOVERY FROM OVERDRIVE: 2.4ns
- LIMITING VOLTAGE ACCURACY: ±15mV
- –3dB BANDWIDTH (G = +1): 530MHz
- SLEW RATE: 1000V/μs
- ±5V AND 5V SUPPLY OPERATION
- HIGH GAIN VERSION: OPA689

APPLICATIONS

- FAST LIMITING ADC INPUT BUFFERS
- CCD PIXEL CLOCK STRIPPING
- VIDEO SYNC STRIPPING
- HF MIXERS
- IF LIMITING AMPLIFIERS
- AM SIGNAL GENERATION
- NON-LINEAR ANALOG SIGNAL PROCESSING
- COMPARATORS

DESCRIPTION

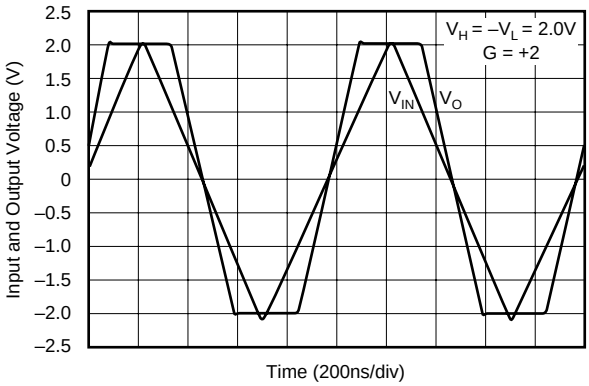
The OPA688 is a wideband, unity gain stable voltage-feedback op amp that offers bipolar output voltage limiting. Two buffered limiting voltages take control of the output when it attempts to drive beyond these limits. This new output limiting architecture holds the limiter offset error to ±15mV. The op amp operates linearly to within 30mV of the output limit voltages.

The combination of narrow nonlinear range and low limiting offset allows the limiting voltages to be set within 100mV of the desired linear output range. A fast 2.4ns recovery from limiting ensures that overdrive signals will be transparent to the signal channel. Implementing the limiting function at the output, as opposed to the input, gives the specified limiting accuracy for any gain, and allows the OPA688 to be used in all standard op amp applications.

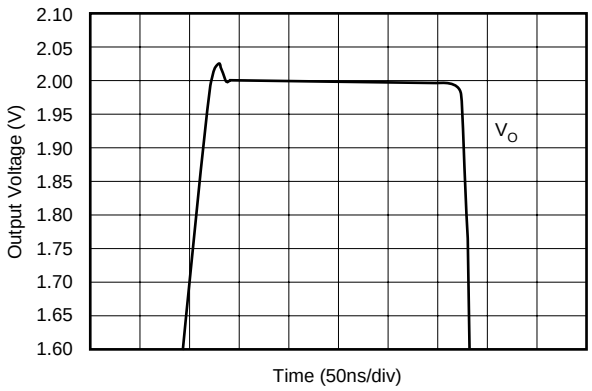
Non-linear analog signal processing will benefit from the OPA688's sharp transition from linear operation to output limiting. The quick recovery time supports high-speed applications.

The OPA688 is available in an industry standard pinout SO-8 package. For higher gain, or transimpedance applications requiring output limiting with fast recovery, consider the OPA689.

LIMITED OUTPUT RESPONSE



DETAIL OF LIMITED OUTPUT VOLTAGE



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SPECIFICATIONS: $V_S = \pm 5V$

G = +2, R_L = 500Ω, R_F = 402Ω, $V_H = -V_L$ = 2V (Figure 1 for AC performance only), unless otherwise noted.

PARAMETER	CONDITIONS	OPA688U TYP +25°C	OPA688U GUARANTEED[1] +25°C	0°C to +70°C	–40°C to +85°C	UNITS	MIN/ MAX	TEST LEVEL[2]
AC PERFORMANCE (see Figure 1)								
Small Signal Bandwidth	V_O < 0.2Vp-p							
	G = +1, R_F = 25Ω	530	—	—	—	MHz	typ	C
	G = +2	260	150	140	135	MHz	min	B
	G = –1	230	—	—	—	MHz	typ	C
Gain-Bandwidth Product (G ≥ +5)	V_O < 0.2Vp-p	290	175	170	160	MHz	min	B
Gain Peaking	G = +1, R_F = 25Ω, V_O < 0.2Vp-p	11	—	—	_	dB	typ	C
0.1dB Gain Flatness Bandwidth	V_O < 0.2Vp-p	50	—	—	—	MHz	typ	C
Large Signal Bandwidth	V_O = 4Vp-p, $V_H = -V_L$ = 2.5V	145	100	95	90	MHz	min	B
Step Response:								
Slew Rate	4V Step, $V_H = -V_L$ = 2.5V	1000	800	770	650	V/µs	min	B
Rise/Fall Time	0.2V Step	1.2	2.6	2.7	3	ns	max	B
Settling Time: 0.05%	2V Step	7	—	—	—	ns	typ	C
Spurious Free Dynamic Range	f = 5MHz, V_O = 2Vp-p	66	62	58	53	dB	min	B
Differential Gain	NTSC, PAL, R_L = 500Ω	0.02	—	—	—	%	typ	C
Differential Phase	NTSC, PAL, R_L = 500Ω	0.01	—	—	—	degrees	typ	C
Input Noise:								
Voltage Noise Density	f ≥ 1MHz	6.3	7.2	7.8	8	nV/√Hz	max	B
Current Noise Density	f ≥ 1MHz	2.0	2.5	2.9	3.6	pA/√Hz	max	B
DC PERFORMANCE (V_{CM} = 0)								
Open Loop Voltage Gain (A_{OL})	V_O = ±0.5V	52	**46**	44	43	dB	min	A
Input Offset Voltage		±2	**±6**	±7	±9	mV	max	A
Average Drift		—	—	±14	±14	µV/°C	max	B
Input Bias Current[3]		+6	**±12**	±13	±20	µA	max	A
Average Drift		—	—	–60	–90	nA/°C	max	B
Input Offset Current		±0.3	**±2**	±3	±4	µA	max	A
Average Drift		—	—	±10	±10	nA/°C	max	B
INPUT								
Common-Mode Rejection	Input Referred, V_{CM} = ±0.5V	57	**50**	49	47	dB	min	A
Common-Mode Input Range[4]		±3.3	**±3.2**	±3.2	±3.1	V	min	A
Input Impedance								
Differential-Mode		0.4 || 1	—	—	—	MΩ || pF	typ	C
Common-Mode		1 || 1	—	—	—	MΩ || pF	typ	C
OUTPUT	$V_H = -V_L$ = 4.3V							
Output Voltage Range	R_L ≥ 500Ω	±4.1	**±3.9**	±3.9	±3.8	V	min	A
Current Output, Sourcing	V_O = 0	105	**90**	85	80	mA	min	A
Sinking	V_O = 0	–85	**–70**	–65	–60	mA	min	A
Closed-Loop Output Impedance	G = +1, R_F = 25Ω, f < 100kHz	0.2	—	—	—	Ω	typ	C
POWER SUPPLY								
Operating Voltage, Specified		±5	—	—	—	V	typ	C
Maximum		—	**±6**	±6	±6	V	max	A
Quiescent Current, Maximum		15.8	**17**	19	20	mA	max	A
Minimum		15.8	**14**	12.8	11	mA	min	A
Power Supply Rejection Ratio	$+V_S$ = 4.5V to 5.5V							
+PSR (Input Referred)		60	**55**	54	52	dB	min	A
OUTPUT VOLTAGE LIMITERS	Pins 5 and 8							
Default Limit Voltage	Limiter Pins Open	±3.3	**±3.0**	±3.0	±2.9	V	min	A
Minimum Limiter Separation ($V_H - V_L$)		200	200	200	200	mV	min	B
Maximum Limit Voltage		—	±4.3	±4.3	±4.3	V	max	B
Limiter Input Bias Current Magnitude [5]	V_O = 0							
Maximum		54	**65**	68	70	µA	max	A
Minimum		54	**35**	34	31	µA	min	A
Average Drift		—	—	40	45	nA/°C	max	B
Limiter Input Impedance		2 || 1	—	—	—	MΩ || pF	typ	C
Limiter Feedthrough[6]	f = 5MHz	–60	—	—	—	dB	typ	C
DC Performance in Limit Mode	V_{IN} = ±2V							
Limiter Offset	($V_O - V_H$) or ($V_O - V_L$)	±15	**±35**	±40	±40	mV	max	A
Op Amp Input Bias Current Shift[3]		3	—	—	—	µA	typ	C
AC Performance in Limit Mode								
Limiter Small Signal Bandwidth	V_{IN} = ±2V, V_O < 0.02Vp-p	450	—	—	—	MHz	typ	C
Limiter Slew Rate[7]		100	—	—	—	V/µs	typ	C
Limited Step Response	2x Overdrive							
Overshoot	V_{IN} = 0 to ±2V Step	250	—	—	—	mV	typ	C
Recovery Time	V_{IN} = ±2V to 0V Step	2.4	2.8	3.0	3.2	ns	max	B
Linearity Guardband[8]	f = 5MHz, V_O = 2Vp-p	30	—	—	—	mV	typ	C

SPECIFICATIONS: $V_S = \pm 5V$ (Cont.)

G = +2, R_L = 500Ω, R_F = 402Ω, $V_H = -V_L$ = 2V (Figure 1 for AC performance only), unless otherwise noted.

PARAMETER	CONDITIONS	OPA688U TYP +25°C	OPA688U GUARANTEED(1) +25°C	0°C to +70°C	–40°C to +85°C	UNITS	MIN/ MAX	TEST LEVEL(2)
THERMAL CHARACTERISTICS								
Temperature Range	Specification: U	–40 to +85	—	—	—	°C	typ	C
Thermal Resistance	Junction-to-Ambient							
U 8-Pin SO-8		125	—	—	—	°C/W	typ	C

NOTES: (1) Junction Temperature = Ambient Temperature for low temperature limit and 25°C guaranteed specifications. Junction Temperature = Ambient Temperature + 23°C at high temperature limit guaranteed specifications. (2) TEST LEVELS: (A) 100% tested at 25°C. Over temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value for information only. (3) Current is considered positive out of node. (4) CMIR tested as < 3dB degradation from minimum CMRR at specified limits. (5) I_{VH} (V_H bias current) is positive, and I_{VL} (V_L bias current) is negative, under these conditions. See Note 3, Figure 1 and Figure 8 . (6) Limiter feedthrough is the ratio of the output magnitude to the sinewave added to V_H (or V_L) when V_{IN} = 0. (7) V_H slew rate conditions are: V_{IN} = +2V, G = +2, V_L = –2V, V_H = step between 2V and 0V. V_L slew rate conditions are similar. (8) Linearity Guardband is defined for an output sinusoid (f = 5MHz, $V_O = 0V_{DC} \pm 1$Vp-p) centered between the limiter levels (V_H and V_L). It is the difference between the limiter level and the peak output voltage where SFDR decreases by 3dB (see Figure 9).

SPECIFICATIONS: V_S = +5V

G = +2, R_L = 500Ω tied to V_{CM} = 2.5V, R_F = 402Ω, $V_L = V_{CM} - 1.2$V, $V_H = V_{CM} + 1.2$V (Figure 2 for AC performance only), unless otherwise noted.

PARAMETER	CONDITIONS	OPA688U TYP +25°C	OPA688U GUARANTEED(1) +25°C	0°C to +70°C	–40°C to +85°C	UNITS	MIN/ MAX	TEST LEVEL(2)
AC PERFORMANCE (see Figure 2)								
Small Signal Bandwidth	V_O < 0.2Vp-p							
	G = +1, R_F = 25Ω	515	—	—	—	MHz	typ	C
	G = +2	240	110	105	100	MHz	min	B
	G = –1	190	—	—	—	MHz	typ	C
Gain-Bandwidth Product (G ≥ +5)	V_O < 0.2Vp-p	275	130	125	120	MHz	min	B
Gain Peaking	G = +1, R_F = 25Ω, V_O < 0.2Vp-p	10	—	—	—	dB	typ	C
0.1dB Gain Flatness Bandwidth	V_O < 0.2Vp-p	50	—	—	—	MHz	typ	C
Large Signal Bandwidth	V_O = 2Vp-p	240	110	105	100	MHz	min	B
Step Response:								
Slew Rate	2V Step	1000	800	770	650	V/µs	min	B
Rise/Fall Time	0.2V Step	2.3	2.6	2.7	3	ns	max	B
Settling Time: 0.05%	1V Step	12	—	—	—	ns	typ	C
Spurious Free Dynamic Range	f = 5MHz, V_O = 2Vp-p	64	60	56	51	dB	min	B
Input Noise:								
Voltage Noise Density	f ≥ 1MHz	6.3	7.2	7.8	8	nV/√Hz	max	B
Current Noise Density	f ≥ 1MHz	2.0	2.5	2.9	3.6	pA/√Hz	max	B
DC PERFORMANCE	V_{CM} = 2.5V							
Open Loop Voltage Gain (A_{OL})	V_O = ±0.5V	52	**46**	44	43	dB	min	A
Input Offset Voltage		±2	**±6**	±7	±9	mV	max	A
Average Drift		—	—	±14	±14	µV/°C	max	B
Input Bias Current(3)		+6	**±12**	±13	±20	µA	max	A
Average Drift		—	—	–60	–90	nA/°C	max	B
Input Offset Current		±0.3	**±2**	±3	±4	µA	max	A
Average Drift		—	—	±10	±10	nA/°C	max	B
INPUT								
Common-Mode Rejection	Input Referred, V_{CM} = ±0.5V	55	**48**	47	45	dB	min	A
Common-Mode Input Range(4)		V_{CM} ±0.8	**V_{CM} ±0.7**	V_{CM} ±0.7	V_{CM} ±0.6	V	min	A
Input Impedance								
Differential-Mode		0.4 || 1	—	—	—	MΩ || pF	typ	C
Common-Mode		1 || 1	—	—	—	MΩ || pF	typ	C
OUTPUT	$V_H = V_{CM} + 1.8$V, $V_L = = V_{CM} - 1.8$V							
Output Voltage Range	R_L ≥ 500Ω	V_{CM} ±1.6	**V_{CM} ±1.4**	V_{CM} ±1.4	V_{CM} ±1.3	V	min	A
Current Output, Sourcing	V_O = 2.5V	70	**60**	55	50	mA	min	A
Sinking	V_O = 2.5V	–60	**–50**	–45	–40	mA	min	A
Closed-Loop Output Impedance	G = +1, R_F = 25Ω, f < 100kHz	0.2	—	—	—	Ω	typ	C
POWER SUPPLY	Single Supply Operation							
Operating Voltage, Specified		+5	—	—	—	V	typ	C
Maximum		—	**+12**	+12	+12	V	max	A
Quiescent Current, Maximum		13	**15**	15	16	mA	max	A
Minimum		13	**11**	10	9	mA	min	A
Power Supply Rejection Ratio	V_S = 4.5V to 5.5V							
+PSR (Input Referred)		60	—	—	—	dB	typ	C

SPECIFICATIONS: V_S = +5V (Cont.)

G = +2, R_L = 500Ω tied to V_{CM} = 2.5V, R_F = 402Ω, V_L = –1.2V, V_H = +1.2V (Figure 2 for AC performance only), unless otherwise noted.

		OPA688U						
		TYP	GUARANTEED[1]					
PARAMETER	CONDITIONS	+25°C	+25°C	0°C to +70°C	–40°C to +85°C	UNITS	MIN/ MAX	TEST LEVEL[2]
OUTPUT VOLTAGE LIMITERS	Pins 5 and 8							
Default Limiter Voltage	Limiter Pins Open	V_{CM} ±0.9	**V_{CM} ±0.6**	V_{CM} ±0.6	V_{CM} ±0.6	V	min	A
Minimum Limiter Separation (V_H – V_L)		200	200	200	200	mV	min	B
Maximum Limit Voltage		—	V_{CM} ±1.8	V_{CM} ±1.8	V_{CM} ±1.8	V	max	B
Limiter Input Bias Current Magnitude[5]	V_O = 2.5V							
Maximum		35	**65**	75	85	µA	max	A
Minimum		35	**0**	0	0	µA	min	A
Average Drift		—	—	30	50	nA/°C	max	B
Limiter Input Impedance		2 || 1	—	—	—	MΩ || pF	typ	C
Limiter Feedthrough[6]	f = 5MHz	–60	—	—	—	dB	typ	C
DC Performance in Limit Mode	V_{IN} = V_{CM} ±1.2V							
Limiter Voltage Accuracy	(V_O – V_H) or (V_O – V_L)	±15	**±35**	±40	±40	mV	max	A
Op Amp Bias Current Shift[3]		5	—	—	—	µA	typ	C
AC Performance in Limit Mode								
Limiter Small Signal Bandwidth	V_{IN} = V_{CM} ±1.2V, V_O < 0.02Vp-p	300	—	—	—	MHz	typ	C
Limiter Slew Rate[7]		20	—	—	—	V/µs	typ	C
Limited Step Response	2x Overdrive							
Overshoot	V_{IN} = V_{CM} to V_{CM} ±1.2V Step	55	—	—	—	mV	typ	C
Recovery Time	V_{IN} = V_{CM} ±1.2V to V_{CM} Step	15	—	—	—	ns	max	C
Linearity Guardband[8]	f = 5MHz, V_O = 2Vp-p	30	—	—	—	mV	max	C
THERMAL CHARACTERISTICS								
Temperature Range	Specification: P, U	–40 to +85	—	—	—	°C	typ	C
Thermal Resistance	Junction-to-Ambient							
U 8-Pin SO-8		125	—	—	—	°C/W	typ	C

NOTES: (1) Junction Temperature = Ambient Temperature for low temperature limit and 25°C guaranteed specifications. Junction Temperature = Ambient Temperature + 23°C at high temperature limit guaranteed specifications. (2) TEST LEVELS: (A) 100% tested at 25°C. Over temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value for information only. (3) Current is considered positive out of node. (4) CMIR tested as < 3dB degradation from minimum CMRR at specified limits. (5) I_{VH} (V_H bias current) is negative, and I_{VL} (V_L bias current) is positive, under these conditions. See Note 3, Figures 2, and Figure 8. (6) Limiter feedthrough is the ratio of the output magnitude to the sinewave added to V_H (or V_L) when V_{IN} = 0. (7) V_H slew rate conditions are: V_{IN} = V_{CM} +0.4V, G = +2, V_L = V_{CM} –1.2V, V_H = step between V_{CM} + 1.2V and V_{CM}. V_L slew rate conditions are similar. (8) Linearity Guardband is defined for an output sinusoid (f = 5MHz, V_O = V_{CM} ±1Vp-p) centered between the limiter levels (V_H and V_L). It is the difference between the limiter level and the peak output voltage where SFDR decreases by 3dB (see Figure 9).

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	$\pm 6.5 V_{DC}$
Internal Power Dissipation	See Thermal Characteristics
Common-Mode Input Voltage	$\pm V_S$
Differential Input Voltage	$\pm V_S$
Limiter Voltage Range	$\pm (V_S - 0.7V)$
Storage Temperature Range: P, U	–40°C to +125°C
Lead Temperature (DIP, soldering, 10s)	+300°C
(SO-8, soldering, 3s)	+260°C
Junction Temperature	+175°C

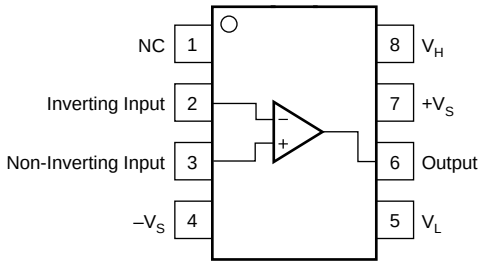
ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

PIN CONFIGURATION

Top View **SO**



PACKAGE/ORDERING INFORMATION

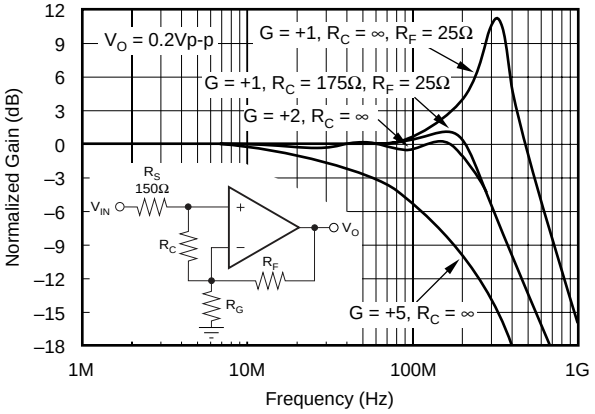
PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER(1)	TRANSPORT MEDIA
OPA688U	SO-8 Surface Mount	182	–40°C to +85°C	OPA688U	OPA688U	Rails
"	"	"	"	"	OPA688U/2K5	Tape and Reel

NOTE: (1) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /2K5 indicates 2500 devices per reel). Ordering 2500 pieces of OPA688U/2K5" will get a single 2500-piece Tape and Reel.

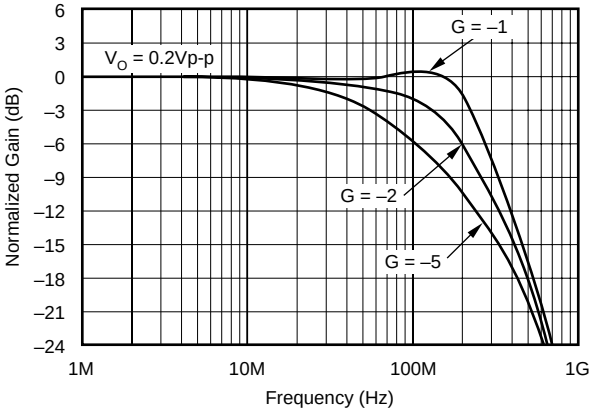
TYPICAL PERFORMANCE CURVES: $V_S = \pm 5V$

G = +2, R_L = 500Ω, R_F = 402Ω, $V_H = -V_L$ = 2V (Figure 1 for AC performance only), unless otherwise noted.

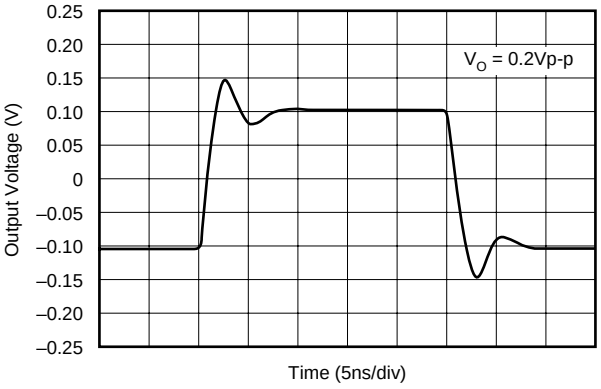
NON-INVERTING SMALL-SIGNAL FREQUENCY RESPONSE



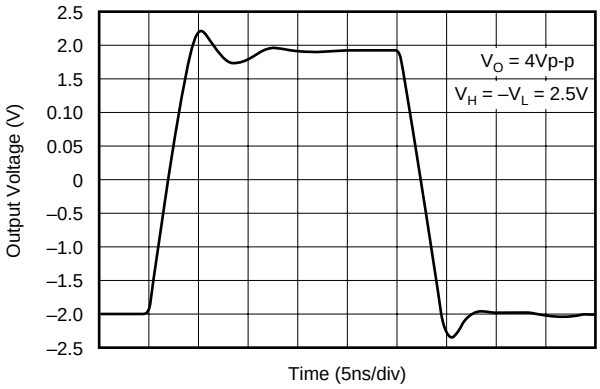
INVERTING SMALL-SIGNAL FREQUENCY RESPONSE



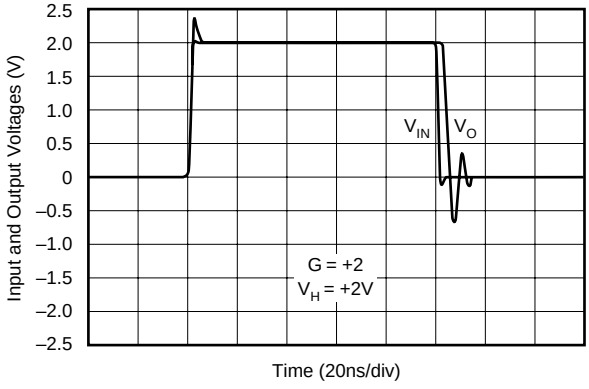
SMALL-SIGNAL PULSE RESPONSE



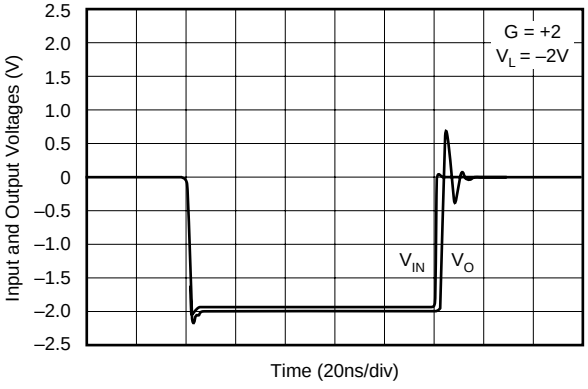
LARGE-SIGNAL PULSE RESPONSE



V_H—LIMITED PULSE RESPONSE



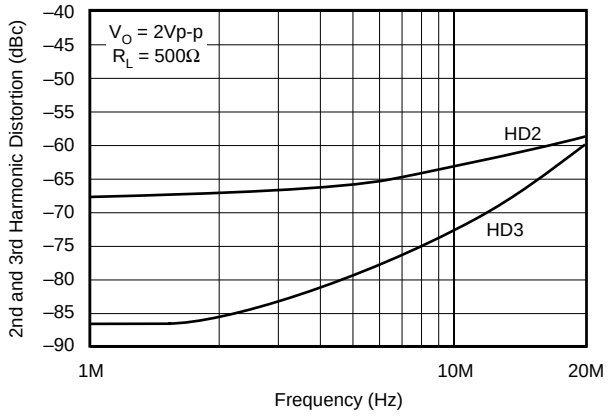
V_L—LIMITED PULSE RESPONSE



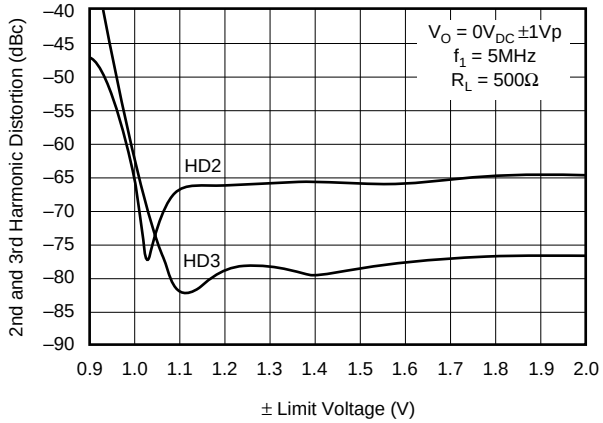
TYPICAL PERFORMANCE CURVES: $V_S = \pm 5V$ (Cont.)

G = +2, R_L = 500Ω, R_F = 402Ω, $V_H = -V_L$ = 2V (Figure 1 for AC performance only), unless otherwise noted.

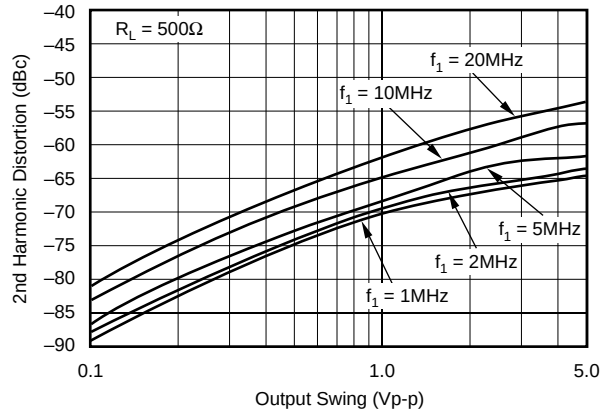
HARMONIC DISTORTION vs FREQUENCY



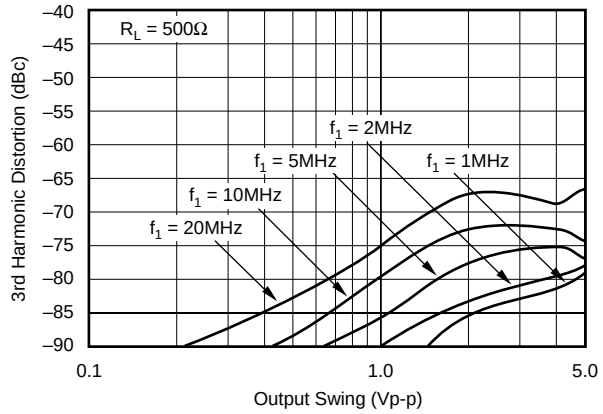
HARMONIC DISTORTION NEAR LIMIT VOLTAGES



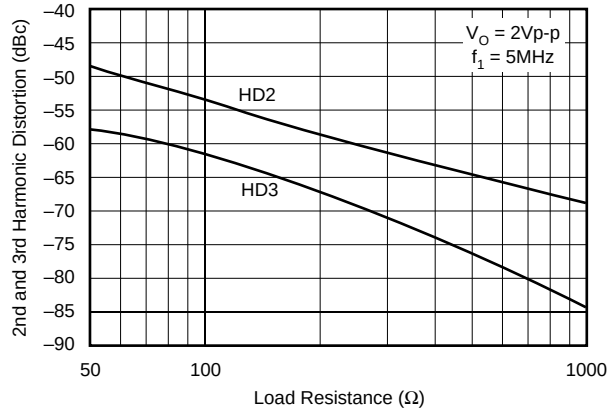
2ND HARMONIC DISTORTION vs OUTPUT SWING



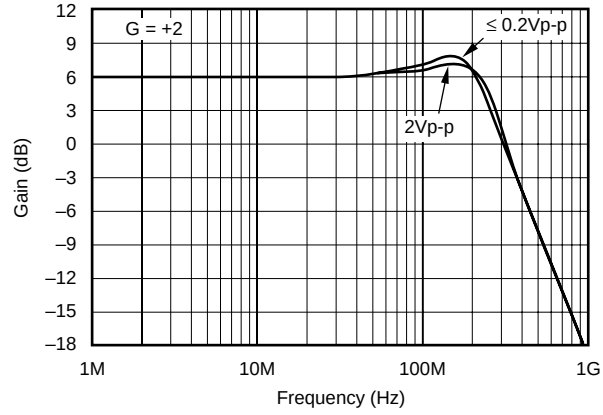
3RD HARMONIC DISTORTION vs OUTPUT SWING



HARMONIC DISTORTION vs LOAD RESISTANCE



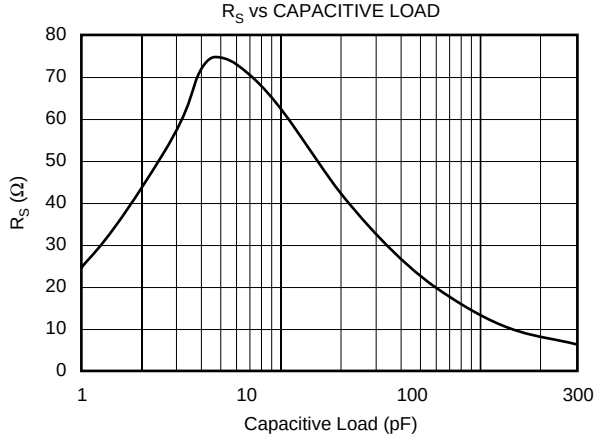
LARGE-SIGNAL FREQUENCY RESPONSE



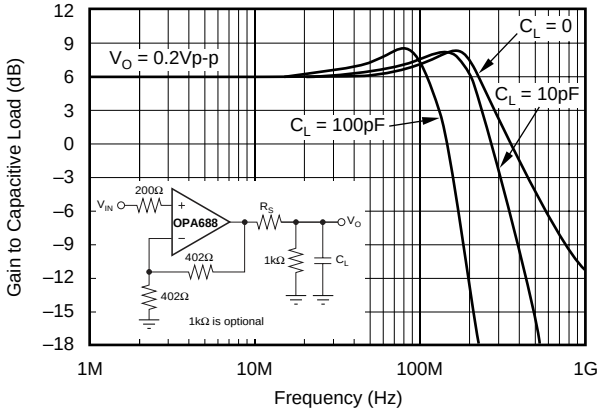
TYPICAL PERFORMANCE CURVES: $V_S = \pm 5V$ (Cont.)

G = +2, R_L = 500Ω, R_F = 402Ω, $V_H = -V_L$ = 2V (Figure 1 for AC performance only), unless otherwise noted.

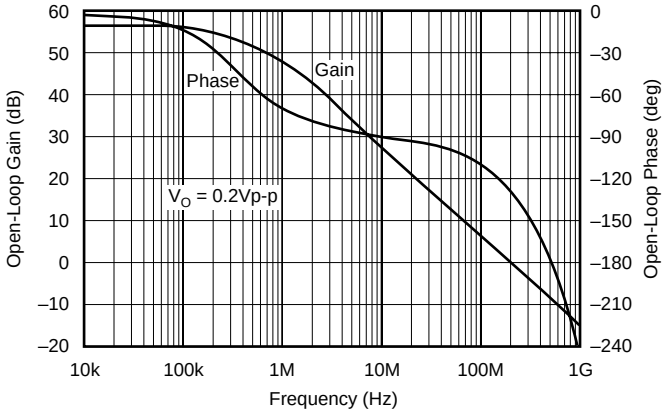
R_S vs CAPACITIVE LOAD



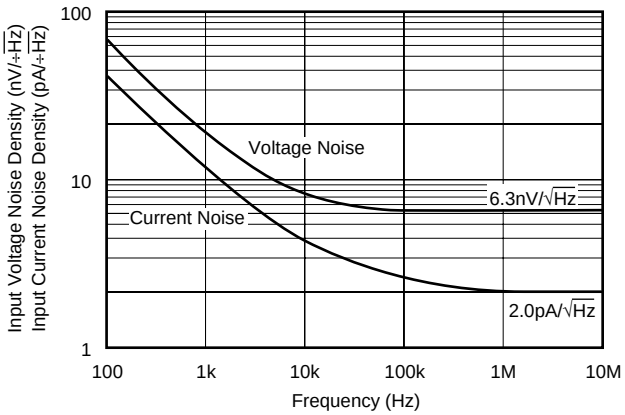
FREQUENCY RESPONSE vs CAPACITIVE LOAD



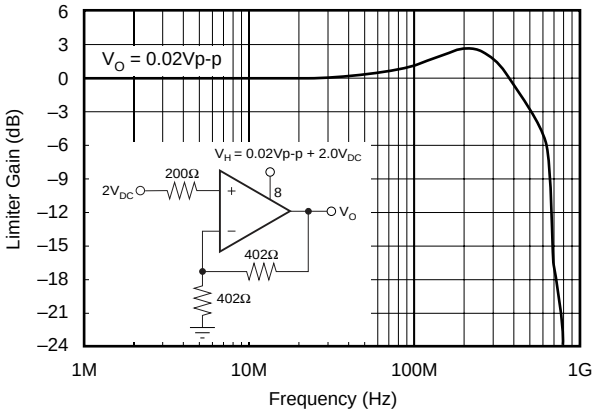
OPEN-LOOP FREQUENCY RESPONSE



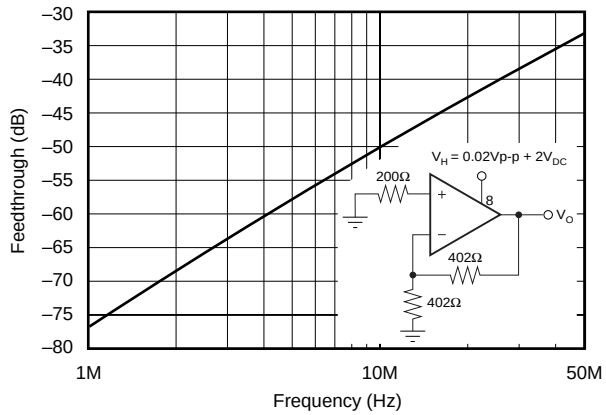
INPUT NOISE DENSITY



LIMITER SMALL-SIGNAL FREQUENCY RESPONSE



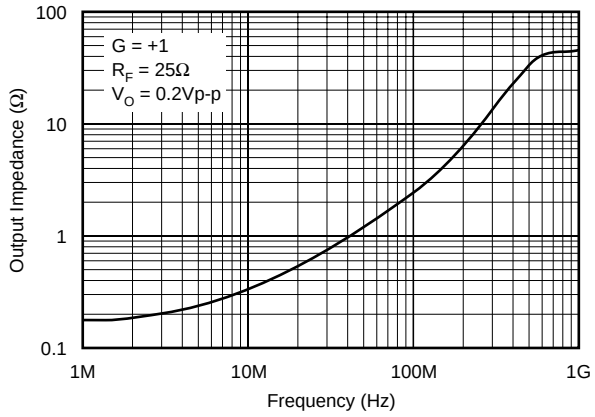
LIMITER FEEDTHROUGH



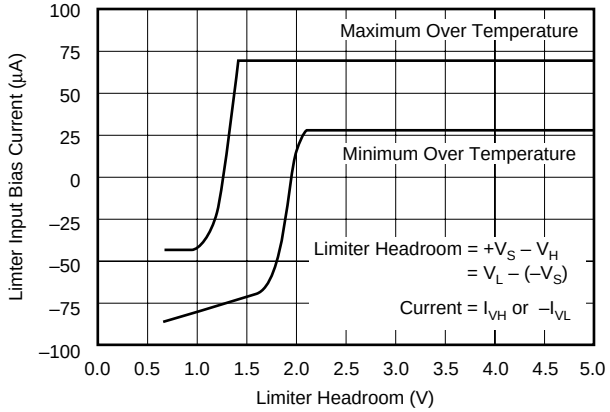
TYPICAL PERFORMANCE CURVES: $V_S = \pm 5V$ (Cont.)

G = +2, R_L = 500Ω, R_F = 402Ω, $V_H = -V_L$ = 2V (Figure 1 for AC performance only), unless otherwise noted.

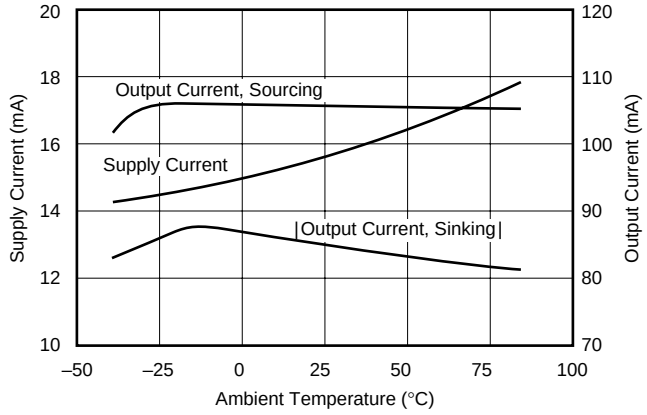
CLOSED-LOOP OUTPUT IMPEDANCE



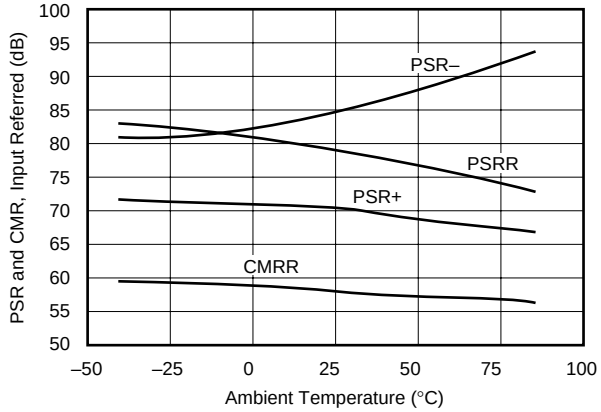
LIMITER INPUT BIAS CURRENT vs BIAS VOLTAGE



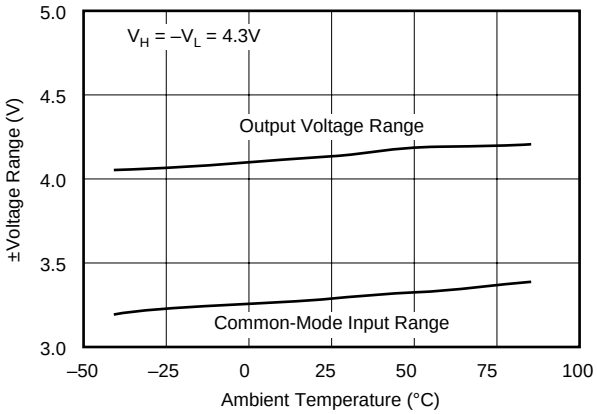
SUPPLY AND OUTPUT CURRENTS vs TEMPERATURE



PSR AND CMR vs TEMPERATURE



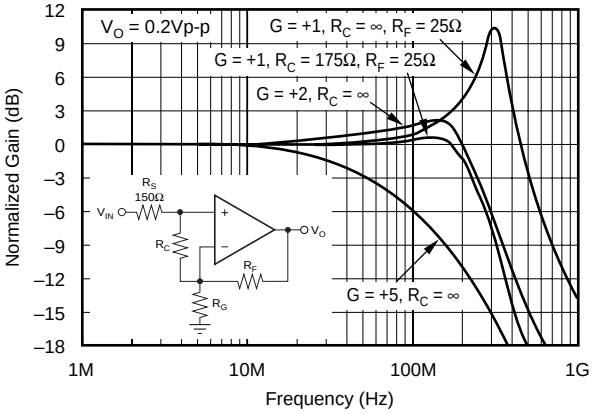
VOLTAGE RANGES vs TEMPERATURE



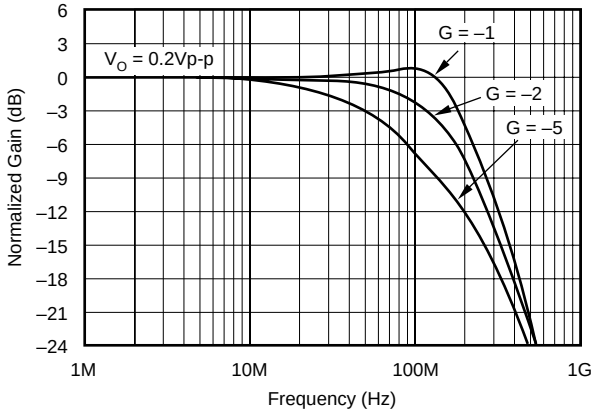
TYPICAL PERFORMANCE CURVES: V_S = +5V

G = +2, R_F = 402Ω, R_L = 500Ω tied to V_{CM} = 2.5V, $V_L = V_{CM} - 1.2V$, $V_H = V_{CM} + 1.2V$, (Figure 2 for AC performance only), unless otherwise noted.

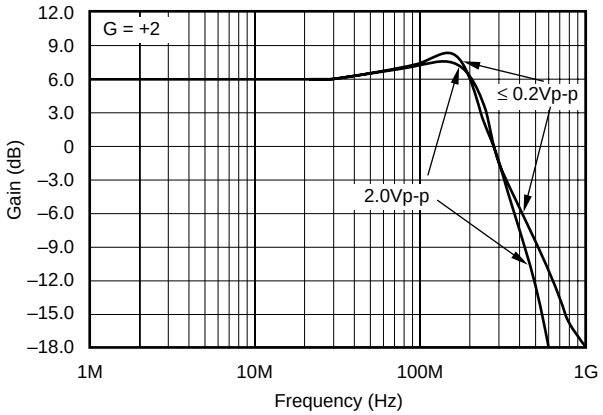
NON-INVERTING SMALL-SIGNAL FREQUENCY RESPONSE



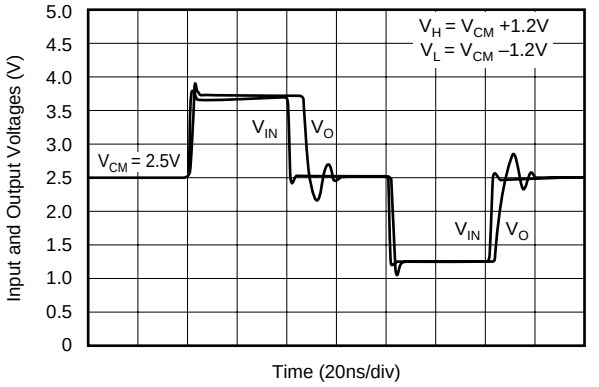
INVERTING SMALL-SIGNAL FREQUENCY RESPONSE



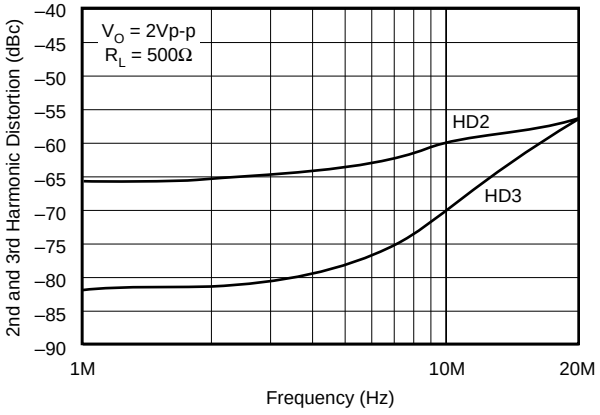
LARGE-SIGNAL FREQUENCY RESPONSE



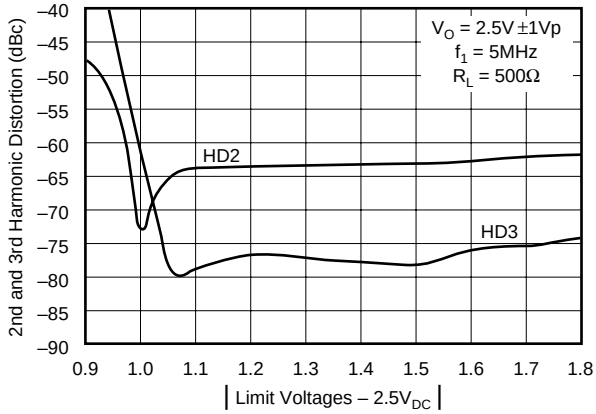
V_H AND V_L—LIMITED PULSE RESPONSE



HARMONIC DISTORTION vs FREQUENCY



HARMONIC DISTORTION NEAR LIMIT VOLTAGES



TYPICAL APPLICATIONS

DUAL-SUPPLY, NON-INVERTING AMPLIFIER

Figure 1 shows a non-inverting gain amplifier for dual-supply operation. This circuit was used for AC characterization of the OPA688, with a 50Ω source, which it matches, and a 500Ω load. The power-supply bypass capacitors are shown explicitly in Figures 1 and 2, but will be assumed in the other figures. The limiter voltages (V_H and V_L) and their bias currents (I_{VH} and I_{VL}) have the polarities shown.

SINGLE-SUPPLY, NON-INVERTING AMPLIFIER

Figure 2 shows an AC-coupled, non-inverting gain amplifier for single +5V supply operation. This circuit was used for AC characterization of the OPA688, with a 50Ω source, which it matches, and a 500Ω load. The power-supply bypass capacitors are shown explicitly in Figures 1 and 2, but will be assumed in the other figures. The limiter voltages (V_H and V_L) and their bias currents (I_{VH} and I_{VL}) have the polarities shown. Notice that the single-supply circuit can use three resistors to set V_H and V_L, where the dual-supply circuit usually uses four to reference the limit voltages to ground.

LIMITED OUTPUT, ADC INPUT DRIVER

Figure 3 shows a simple ADC (Analog-to-Digital Converter) driver that operates on a single supply, and gives excellent distortion performance. The limit voltages track the input range of the converter, completely protecting against input overdrive.

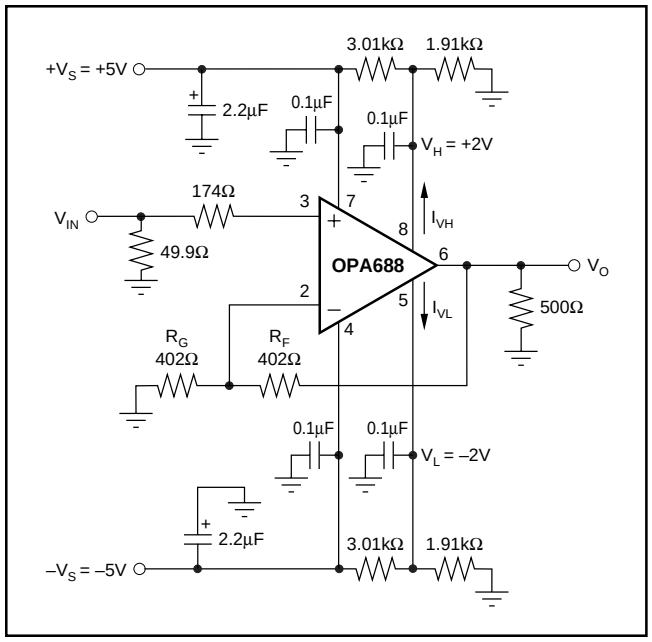


FIGURE 1. DC-Coupled, Dual Supply Amplifier.

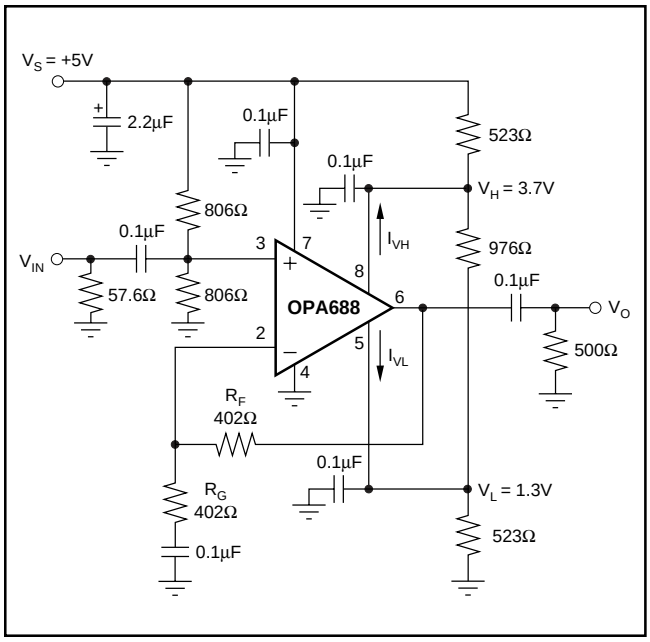


FIGURE 2. AC-Coupled, Single Supply Amplifier.

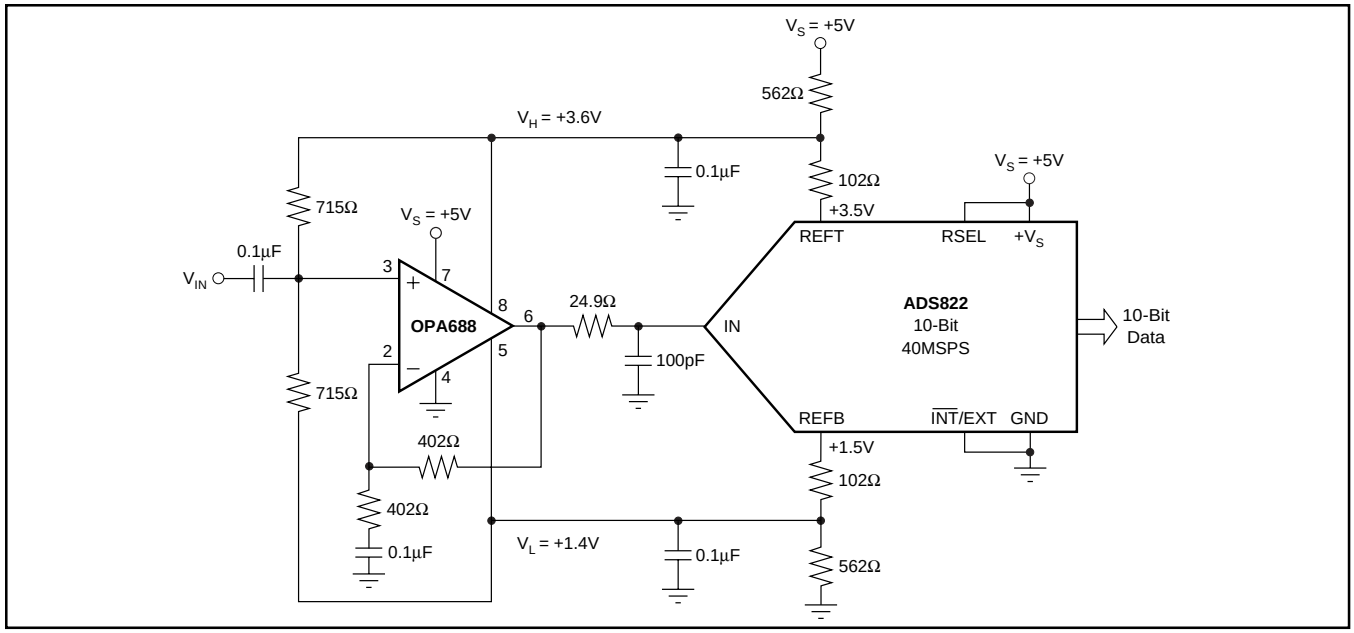


FIGURE 3. Single Supply, Limiting ADC Input Driver.

PRECISION HALF WAVE RECTIFIER

Figure 4 shows a half wave rectifier with outstanding precision and speed. V_H (pin 8) will default to a voltage between 3.1 and 3.8V if left open, while the negative limit is set to ground.

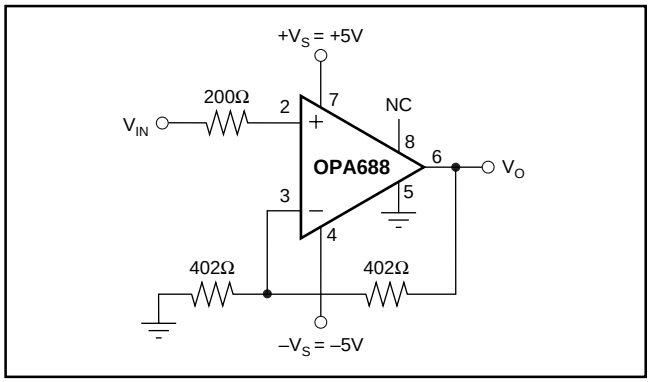


FIGURE 4. Precision Half Wave Rectifier.

VERY HIGH SPEED SCHMITT TRIGGER

Figure 5 shows a very high-speed Schmitt trigger. The output levels are precisely defined, and the switching time is exceptional. The output voltage swings between ±2V.

UNITY-GAIN BUFFER

Figure 6 shows a unity-gain voltage buffer using the OPA688. The feedback resistor (R_F) isolates the output from any board inductance between pins 2 and 6. We recommend that $R_F \geq 24.9\Omega$ for unity-gain buffer applications. R_C is an optional compensation resistor that reduces the peaking typically seen at G = +1. Choosing $R_C = R_S + R_F$ gives a unity gain buffer with approximately the G = +2 frequency response.

DC RESTORER

Figure 7 shows a DC restorer using the OPA688 and OPA660. The OPA660's OTA amplifier is used as a Current Conveyor (CCII) in this circuit, with a current gain of 1.0. When V_O tries to go below ground, CCII charges C_1 through D_1, which restores the output back to ground. D_1 adds a propagation delay to the restoration process, which then has an exponential decay with time constant R_1C_1/G (G = +2 = the OPA688 gain). When the signal is above ground, it decays to ground with a time constant of R_2C_1. The OPA688 output recovers very quickly from overdrive.

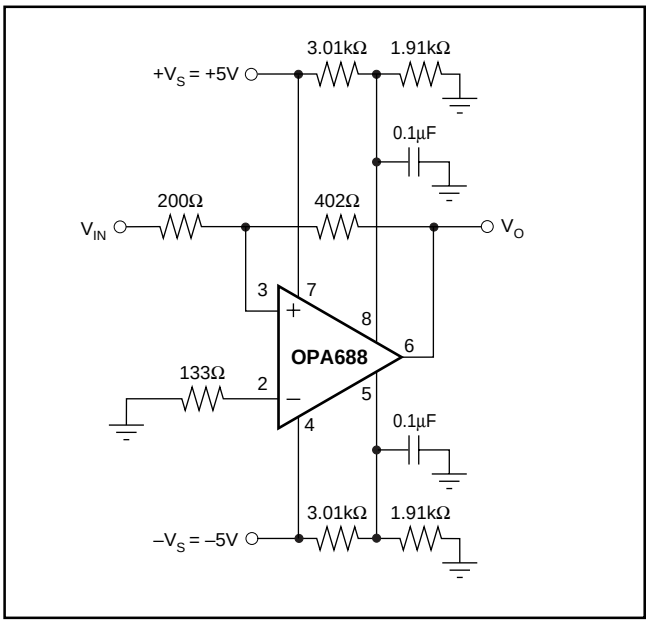


FIGURE 5. Very High Speed Schmitt Trigger.

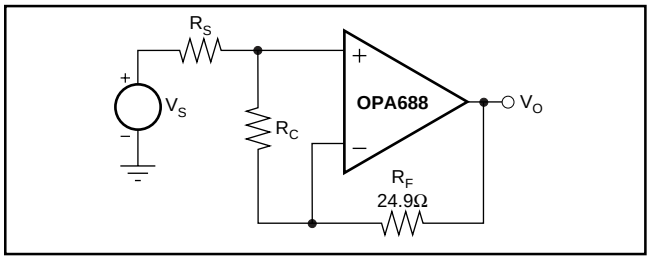


FIGURE 6. Unity-Gain Buffer.

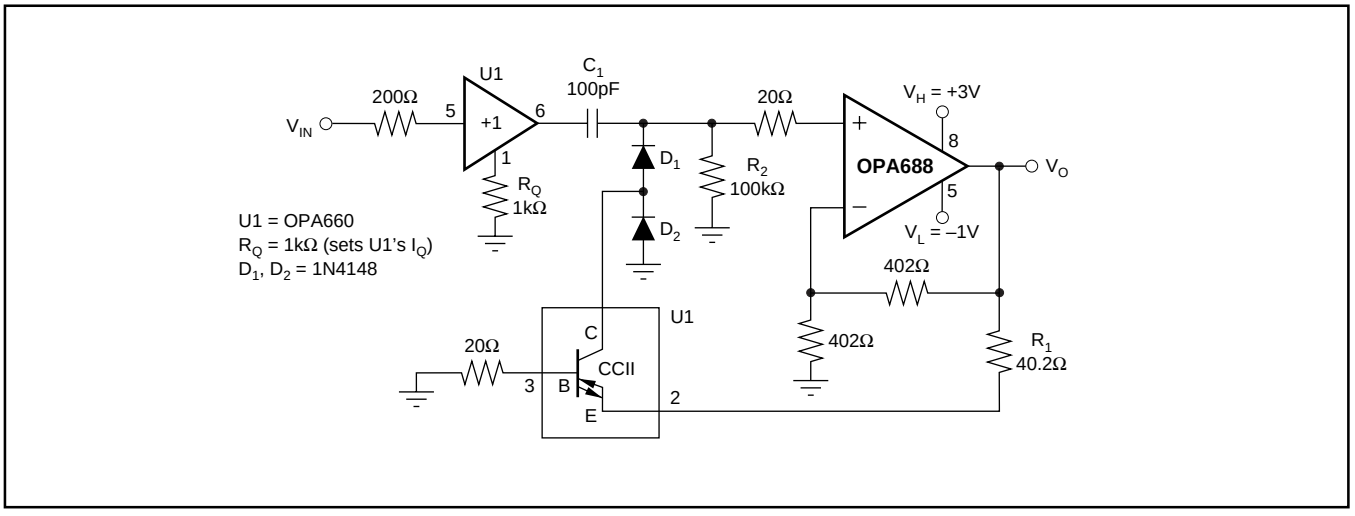


FIGURE 7. DC Restorer.

DESIGN-IN TOOLS

APPLICATIONS SUPPORT

The Texas Instruments Applications Department is available for design assistance at 1-972-644-5580. The Texas Instrments web site (http://www.ti.com) has the latest data sheets and other design aids.

DEMONSTRATION BOARDS

A PC board is available to assist in the initial evaluation of circuit performance of the OPA688U. It is available as an unpopulated PCB with descriptive documentation. See the demonstration board literature for more information. The summary information for this board is shown in Table I.

DEMONSTRATION BOARD	PACKAGE	PRODUCT	LITERATURE REQUEST NUMBER
DEM-OPA68xU	SO-8	OPA68xU	MKT-351

TABLE I. Demo Board Summary Information.

Contact the Texas Instruments Technical Applications Support Line at 1-972-644-5580 for availability of these boards.

OPERATING INFORMATION

THEORY OF OPERATION

The OPA688 is a voltage-feedback op amp that is unity-gain stable. The output voltage is limited to a range set by the voltage on the limiter pins (5 and 8). When the input tries to overdrive the output, the limiters take control of the output buffer. This avoids saturating any part of the signal path, giving quick overdrive recovery and excellent limiter accuracy at any signal gain.

The limiters have a very sharp transition from the linear region of operation to output limiting. This allows the limiter voltages to be set very near (< 100mV) the desired signal range. The distortion performance is also very good near the limiter voltages.

CIRCUIT LAYOUT

Achieving optimum performance with the high-frequency OPA688 requires careful attention to layout design and component selection. Recommended PCB layout techniques and component selection criteria are:

a) **Minimize parasitic capacitance to any AC ground** for all of the signal I/O pins. Open a window in the ground and power planes around the signal I/O pins, and leave the ground and power planes unbroken elsewhere.

b) **Provide a high quality power supply.** Use linear regulators, ground plane and power planes to provide power. Place high-frequency 0.1µF decoupling capacitors < 0.2" away from each power-supply pin. Use wide, short traces to connect to these capacitors to the ground and power planes. Also use larger (2.2µF to 6.8µF) high-frequency decoupling capacitors to bypass lower frequencies. They may be somewhat further from the device, and be shared among several adjacent devices.

c) **Place external components close** to the OPA688. This minimizes inductance, ground loops, transmission line effects and propagation delay problems. Be extra careful with the feedback (R_F), input and output resistors.

d) **Use high-frequency components** to minimize parasitic elements. Resistors should be a very low reactance type. Surface-mount resistors work best and allow a tighter layout. Metal film or carbon composition axially-leaded resistors can also provide good performance when their leads are as short as possible. Never use wirewound resistors for high-frequency applications. Remember that most potentiometers have large parasitic capacitances and inductances.

Multilayer ceramic chip capacitors work best and take up little space. Monolithic ceramic capacitors also work very well. Use RF type capacitors with low ESR and ESL. The large power pin bypass capacitors (2.2µF to 6.8µF) should be tantalum for better high-frequency and pulse performance.

e) **Choose low resistor values** to minimize the time constant set by the resistor and its parasitic parallel capacitance. Good metal film or surface mount resistors have approximately 0.2pF parasitic parallel capacitance. For resistors > 1.5kΩ, this adds a pole and/or zero below 500MHz.

Make sure that the output loading is not too heavy. The recommended 402Ω feedback resistor is a good starting point in your design.

f) **Use short direct traces to other wideband devices** on the board. Short traces act as a lumped capacitive load. Wide traces (50 to 100 mils) should be used. Estimate the total capacitive load at the output, and use the series isolation resistor recommended in the typical performance curve "R_S vs Capacitive Load". Parasitic loads < 2pF may not need the isolation resistor.

g) **When long traces are necessary,** use transmission line design techniques (consult an ECL design handbook for microstrip and stripline layout techniques). A 50Ω transmission line is not required on board—a higher characteristic impedance will help reduce output loading. Use a matching series resistor at the output of the op amp to drive a transmission line, and a matched load resistor at the other end to make the line appear as a resistor. If the 6dB of attenuation that the matched load produces is not acceptable, and the line is not too long, use the series resistor at the source only. This will isolate the source from the reactive load presented by the line, but the frequency response will be degraded.

Multiple destination devices are best handled as separate transmission lines, each with its own series source and shunt load terminations. Any parasitic impedances acting on the terminating resistors will alter the transmission line match, and can cause unwanted signal reflections and reactive loading.

h) **Do not use sockets** for high-speed parts like the OPA688. The additional lead length and pin-to-pin capacitance introduced by the socket creates an extremely troublesome parasitic network. Best results are obtained by soldering the part onto the board.

POWER SUPPLIES

The OPA688 is nominally specified for operation using either ±5V supplies or a single +5V supply. The maximum specified total supply voltage of 12V allows reasonable tolerances on the supplies. Higher supply voltages can break down internal junctions, possibly leading to catastrophic failure. Single-supply operation is possible as long as common mode voltage constraints are observed. The common mode input and output voltage specifications can be interpreted as a required headroom to the supply voltage. Observing this input and output headroom requirement will allow design of non-standard or single-supply operation circuits. Figure 2 shows one approach to single-supply operation.

ESD PROTECTION

ESD damage has been known to damage MOSFET devices, but any semiconductor device is vulnerable to ESD damage. This is particularly true for very high-speed, fine geometry processes.

ESD damage can cause subtle changes in amplifier input characteristics without necessarily destroying the device. In precision operational amplifiers, this may cause a noticeable degradation of offset voltage and drift. Therefore, ESD handling precautions are required when handling the OPA688.

OUTPUT LIMITERS

The output voltage is linearly dependent on the input(s) when it is between the limiter voltages V_H (pin 8) and V_L (pin 5). When the output tries to exceed V_H or V_L, the corresponding limiter buffer takes control of the output voltage and holds it at V_H or V_L.

Because the limiters act on the output, their accuracy does not change with gain. The transition from the linear region of operation to output limiting is very sharp—the desired output signal can safely come to within 30mV of V_H or V_L with no onset of non-linearity.

The limiter voltages can be set to within 0.7V of the supplies ($V_L \geq -V_S + 0.7V$, $V_H \leq +V_S - 0.7V$). They must also be at least 200mV apart ($V_H - V_L \geq 0.2V$).

When pins 5 and 8 are left open, V_H and V_L go to the Default Voltage Limit; the minimum values are in the Specifications. Looking at Figure 8 for the zero bias current case will show the expected range of (V_s – default limit voltages) = headroom.

When the limiter voltages are more than 2.1V from the supplies ($V_L \geq -V_S + 2.1V$ or $V_H \leq +V_S - 2.1V$), you can use simple resistor dividers to set V_H and V_L (see Figure 1). Make sure you include the Limiter Input Bias Currents (Figure 8) in the calculations (i.e., $I_{VL} \approx -50\mu A$ out of pin 5, and $I_{VH} \approx +50\mu A$ out of pin 8). For good limiter voltage accuracy, run at least 1mA quiescent bias current through these resistors.

When the limiter voltages need to be within 2.1V of the supplies ($V_L \leq -V_S + 2.1V$ or $V_H \geq +V_S - 2.1V$), consider using low impedance buffers to set V_H and V_L to minimize errors due to bias current uncertainty. This will typically be the case for single supply operation (V_S = +5V). Figure 2 runs 2.5mA through the resistive divider that sets V_H and V_L. This keeps errors due to I_{VH} and I_{VL} < ±1% of the target limit voltages.

The limiters' DC accuracy depends on attention to detail. The two dominant error sources can be improved as follows:

- Power supplies, when used to drive resistive dividers that set V_H and V_L, can contribute large errors (e.g., ±5%). Using a more accurate source, and bypassing pins 5 and 8 with good capacitors, will improve limiter PSRR.
- The resistor tolerances in the resistive divider can also dominate. Use 1% resistors.

Other error sources also contribute, but should have little impact on the limiters' DC accuracy:

- Reduce offsets caused by the Limiter Input Bias Currents. Select the resistors in the resistive divider(s) as described above.
- Consider the signal path DC errors as contributing to uncertainty in the useable output swing.
- The Limiter Offset Voltage only slightly degrades limiter accuracy.

Figure 9 shows how the limiters affect distortion performance. Virtually no degradation in linearity is observed for output voltage swinging right up to the limiter voltages.

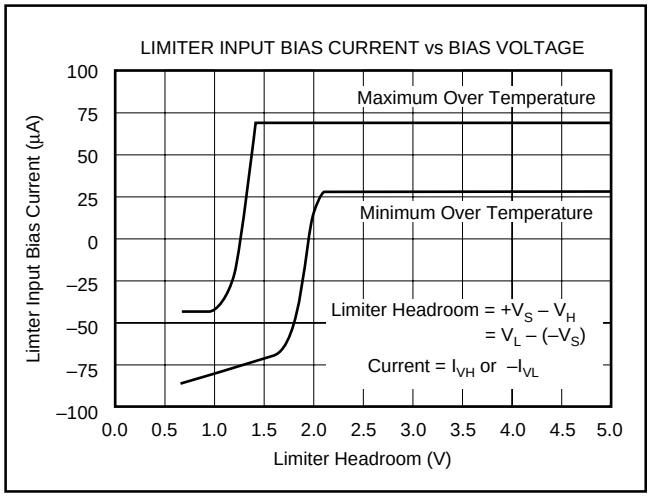


FIGURE 8. Limiter Bias Current vs Bias Voltage.

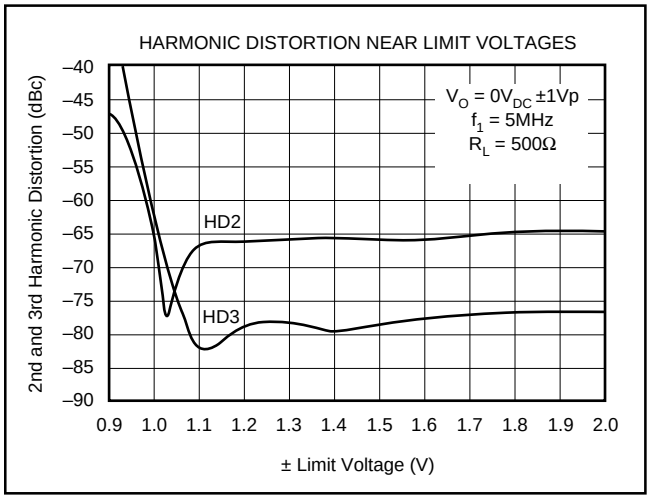


FIGURE 9. Harmonic Distortion Near Limit Voltages.

OFFSET VOLTAGE ADJUSTMENT

The circuit in Figure 10 allows offset adjustment without degrading offset drift with temperature. Use this circuit with caution since power supply noise can inadvertently couple into the op amp.

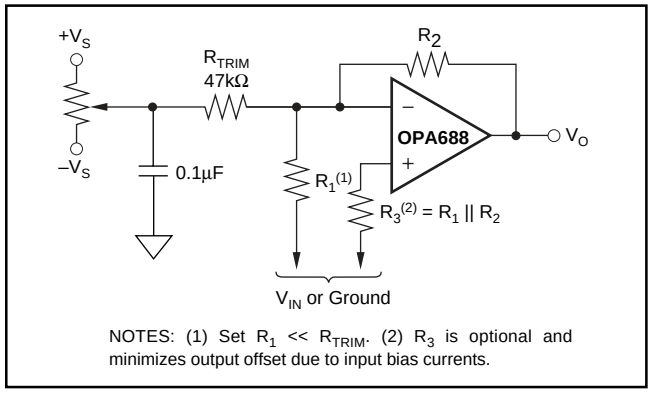


FIGURE 10. Offset Voltage Trim.

Remember that additional offset errors can be created by the amplifier's input bias currents. Whenever possible, match the impedance seen by both DC input bias currents using R_3. This minimizes the output offset voltage caused by the input bias currents.

OUTPUT DRIVE

The OPA688 has been optimized to drive 500Ω loads, such as ADCs. It still performs very well driving 100Ω loads; the specifications are shown for the 500Ω load. This makes the OPA688 an ideal choice for a wide range of high-frequency applications.

Many high-speed applications, such as driving ADCs, require op amps with low output impedance. As shown in the typical performance curve "Output Impedance vs Frequency", the OPA688 maintains very low closed-loop output impedance over frequency. Closed-loop output impedance increases with frequency, since loop gain decreases with frequency.

THERMAL CONSIDERATIONS

The OPA688 will not require heat-sinking under most operating conditions. Maximum desired junction temperature will set a maximum allowed internal power dissipation as described below. In no case should the maximum junction temperature be allowed to exceed 175°C.

The total internal power dissipation (P_D) is the sum of quiescent power (P_{DQ}) and the additional power dissipated in the output stage (P_{DL}) while delivering load power. P_{DQ} is simply the specified no-load supply current times the total supply voltage across the part. P_{DL} depends on the required output signals and loads. For a grounded resistive load, and equal bipolar supplies, it is at a maximum when the output is at 1/2 either supply voltage. In this condition, $P_{DL} = V_S^2/(4R_L)$ where R_L includes the feedback network loading. Note that it is the power in the output stage, and not in the load, that determines internal power dissipation.

The operating junction temperature is: $T_J = T_A + P_D \theta_{JA}$, where T_A is the ambient temperature.

For example, the maximum T_J for a OPA688U with G = +2, R_{FB} = 402Ω, R_L = 100Ω, and $\pm V_S = \pm 5V$ at the maximum T_A = +85°C is calculated as:

$$P_{DQ} = (10V \bullet 20mA) = 200mW$$

$$P_{DL} = \frac{(5V)^2}{4 \bullet (100\Omega \parallel 804\Omega)} = 70mW$$

$$P_D = 200mW + 70mW = 270mW$$

$$T_J = 85°C + 270mW \bullet 125°C/W = 119°C$$

CAPACITIVE LOADS

Capacitive loads, such as the input to ADCs, will decrease the amplifier's phase margin, which may cause high-frequency peaking or oscillations. Capacitive loads ≥ 2pF should be isolated by connecting a small resistor in series with the output as shown in Figure 11. Increasing the gain from +2 will improve the capacitive drive capabilities due to increased phase margin.

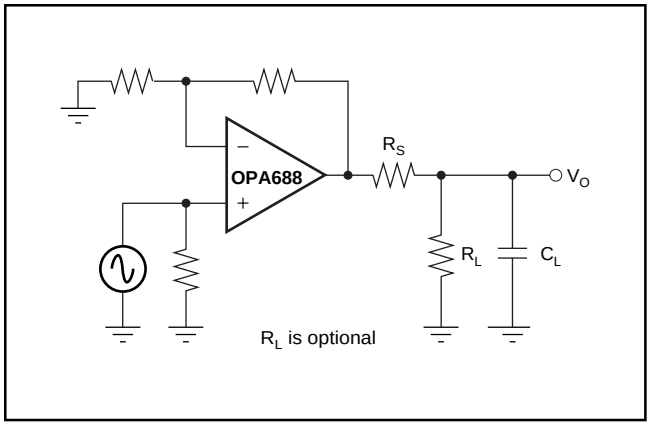


FIGURE 11. Driving Capacitive Loads.

In general, capacitive loads should be minimized for optimum high-frequency performance. The capacitance of coax cable (29pF/foot for RG-58) will not load the amplifier when the coaxial cable, or transmission line, is terminated in its characteristic impedance.

FREQUENCY RESPONSE COMPENSATION

The OPA688 is internally compensated to be unity-gain stable, and has a nominal phase margin of 60° at a gain of +2. Phase margin and peaking improve at higher gains. Recall that an inverting gain of –1 is equivalent to a gain of +2 for bandwidth purposes (i.e., noise gain = 2).

Standard external compensation techniques work with this device. For example, in the inverting configuration, the bandwidth may be limited without modifying the inverting gain by placing a series RC network to ground on the inverting node. This has the effect of increasing the noise gain at high frequencies, which limits the bandwidth.

To maintain a wide bandwidth at high gains, cascade several op amps, or use the high gain optimized OPA689.

In applications where a large feedback resistor is required, such as photodiode transimpedance amplifier, the parasitic capacitance from the inverting input to ground causes peaking or oscillations. To compensate for this effect, connect a small capacitor in parallel with the feedback resistor. The bandwidth will be limited by the pole that the feedback resistor and this capacitor create. In other high gain applications, use a three resistor "Tee" network to reduce the RC time constants set by the parasitic capacitances. Be careful to not increase the noise generated by this feedback network too much.

PULSE SETTLING TIME

The OPA688 is capable of an extremely fast settling time in response to a pulse input. Frequency response flatness and phase linearity are needed to obtain the best settling times. For capacitive loads, such as an ADC, use the recommended R_S in the typical performance curve "R_S vs Capacitive Load". Extremely fine-scale settling (0.01%) requires close attention to ground return current in the supply decoupling capacitors.

The pulse settling characteristics when recovering from overdrive are very good.

DISTORTION

The OPA688's distortion performance is specified for a 500Ω load, such as an ADC. Driving loads with smaller resistance will increase the distortion as illustrated in Figure 12. Remember to include the feedback network in the load resistance calculations.

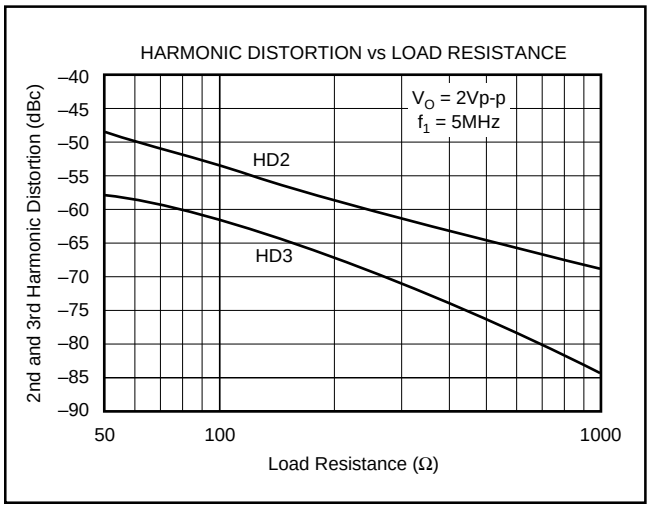


FIGURE 12. 5MHz Harmonic Distortion vs Load Resistance.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
OPA688P	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI
OPA688U	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI
OPA688U/2K5	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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- Military: OPA688M

NOTE: Qualified Version Definitions:
- Military - QML certified for Military and Defense Applications

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