'290, 'LS290 . . . DECADE COUNTERS
'293, 'LS293 . . . 4-BIT BINARY COUNTERS

 GND and V_{CC} on Corner Pins (Pins 7 and 14 Respectively)

description

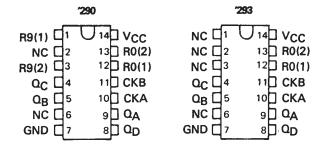
The SN54290/SN74290, SN54LS290/SN74LS290, SN54293/SN74293, and SN54LS293/SN74LS293 counters are electrically and functionally identical to the SN5490A/SN7490A, SN54LS90/SN74LS90, SN5493A/SN7493A, and SN54LS93/SN74LS93, respectively. Only the arrangement of the terminals has been changed for the '290, 'LS290, '293, and 'LS293.

Each of these monolithic counters contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three-stage binary counter for which the count cycle length is divide-by-five for the '290 and 'LS290 and divide-by-eight for the '293 and 'LS293.

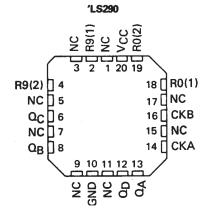
All of these counters have a gated zero reset and the '290 and 'LS290 also have gated set-to-nine inputs for use in BCD nine's complement applications.

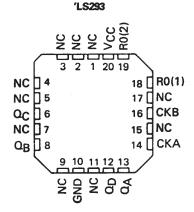
To use the maximum count length (decade or four-bit binary) of these counters, the B input is connected to the Ω_A output. The input count pulses are applied to input A and the outputs are as described in the appropriate function table. A symmetrical divide-byten count can be obtained from the '290 and 'LS290 counters by connecting the Ω_D output to the A input and applying the input count to the B input which gives a divide-by-ten square wave at output Ω_A .

SN54290, SN54LS290, SN54293, SN54LS293 . . . J OR W PACKAGE SN74290, SN74293 . . . N PACKAGE SN74LS290, SN74LS293 . . . D OR N PACKAGE (TOP VIEW)



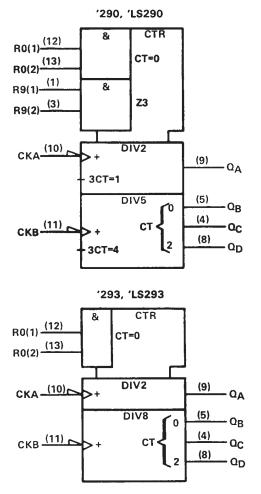
SN54LS290, SN54LS293 . . . FK PACKAGE (TOP VIEW)





NC - No internal connection

logic symbols†



 $^{^\}dagger$ These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for D, J, N, and W packages.



'290, 'LS290 BCD COUNT SEQUENCE (See Note A)

• • • • • • • • • • • • • • • • • • • •				
COUNT		OUT	PUT	
COONT	a_{D}	αç	αB	QA
0	L	L	L	L
1	L	L	L	н
2	L	L	н	L
3	Ł	L	н	н
4	L	Н	L	L
5	L	Н	L	н
6	L	Н	н	L
7	L	н	н	н
8	н	L	L	L
9	н	L	L	н

'290, 'LS290 BI-QUINARY (5-2) (See Note B)

(See Note B)												
COUNT		OUT	PUT									
COUNT	QA	σ_{D}	αc	σ_{B}								
0	L	L	L	L								
1	L	L	L	H								
2	L	L	Н	L								
3	L	L	Н	н								
4	L	н	L	L								
5	н	L	L	L								
6	н	L	L	н								
7	н	L	Н	L								
8	н	L	Н	Н								
9	н	н	L	L								

'290, 'LS290 RESET/COUNT FUNCTION TABLE

R _{O(1)} R _{O(2)} R ₉₍₁₎ R ₉₍₂₎ Q _D Q _C H H L X L L H H X L L L X X H H L L	OUTPUT							
H H X L L L	αB	QA						
	L	L						
· · · · · · · · · · · · · · · · · · ·	L	L						
~ ~ " " " " " " " " " " " " " " " " " "	L	н						
X L X L COL	UNT	•						
L X L X COL	UNT	-						
L X X L COL	UNT	•						
X L L X COL	UNT							

'293, 'L\$293
RESET/COUNT FUNCTION TABLE

RESET	INPUTS		OUT	PUT	
R ₀₍₁₎	R ₀₍₂₎	αp	QC	αB	QA
Н	Н	L	L	L.	L
L	×		CO	TNL	
×	L		COL	TNL	

'293, 'LS293 COUNT SEQUENCE (See Note C)

COUNT		TUO	PUT	
000111	α_{D}	α_{C}	α_{B}	Q_{A}
0	L	L	L	L
1	L	L	L	Н
2	L	Ł	Н	L
3	L	L	Н	Н
4	L	Н	L	L
5	L	Н	L	н
6	L	Н	Н	L
7	L	Н	Н	н
8	н	L	L	L
9	н	L	L	Н
10	н	L	Н	L
11	н	L	Н	Н
12	H	Н	L	L
13	н	н	L	Н
14	н	Н	н	L
15	н	н	н	Н

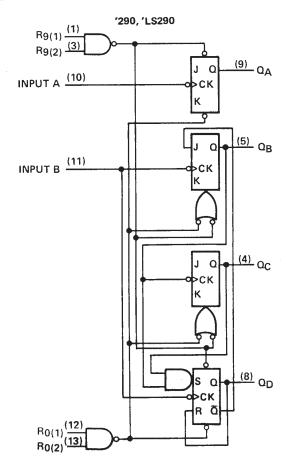
C. Output QA is connected to input B.

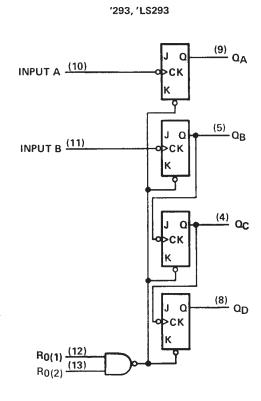
D. H = high level, L = low level, X = irrelevant

NOTES: A. Output Ω_A is connected to input B for BCD count.

B. Output QD is connected to input A for bi-quinary

logic diagrams (positive logic)



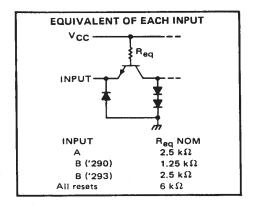


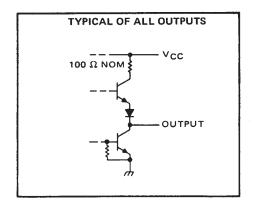
Pin numbers shown are for D, J, N, and W packages.

The J and K inputs shown without connection are for reference only and are functionally at a high level.



schematics of inputs and outputs





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC (see Note 1) .																					7 \	V
Input voltage																					5.5 \	/
Interemitter voltage (see Note 2) .																						
Operating free-air temperature range:	5	SN	54	′ (Cir	cui	its										-5	5°	C	to	125°(C
	5	SN	74	' (Cir	cui	ts											0)°C	C to	o 70° (С
Storage temperature range																	6	5°	C	to	150°	С

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.

2. This is the voltage between two emitters of a multiple-emitter transistor. For these circuits, this rating applies between the two R₀ inputs, and for the '290 circuit, it also applies between the two R9 inputs.

recommended operating conditions

			SN5	4'		SN74	,	
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Supply voltage, VCC		4.5	5	5.5	4.75	5	5.25	V
High-level output current, IOH				-800			-800	μА
Low-level output current, IOL				16			16	mA
	A input	0		32	0		32	MHz
Count frequency, f _{count}	B input	0		16	0		16	IVITIZ
	A input	15			15			
Pulse width, tw	B input	30			30			ns
	Reset inputs	15			15			
Reset inactive-state setup time, t _{su}	•	25			25			ns
Operating free-air temperature, TA		-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

				t		′290			'293		
	PARAMETER		TEST CONDITIO	INS	MIN	TYP‡	MAX	MIN	TYP‡	MAX	UNIT
VIH	High-level input voltage				2			2			V
VIL	Low-level input voltage						0.8			0.8	V
VIK	Input clamp voltage		V _{CC} = MIN, I ₁ = -1	2 mA			-1.5			-1.5	V
VOH	High-level output voltage		V _{CC} = MIN, V _{IH} = V _{IL} = 0.8 V, I _{OH} =		2.4	3.4		2.4	3.4	-	٧
VOL	Low-level output voltage		V _{CC} = MIN, V _{IH} = V _{IL} = 0.8 V, I _{OL} =	_		0.2	0.4		0.2	0.4	V
11	Input current at maximum inp	out voltage	V _{CC} = MAX, V _I = 5	.5 V			1			1	mA
,		Any reset					40			40]
Ιн	High-level input current	A input	$V_{CC} = MAX, V_1 = 2$.4 V			80			80	μΑ
		B input	1				120			80	
		Any reset					-1.6			-1.6	
I _I L	Low-level input current	A input	$V_{CC} = MAX, V_{I} = 0$.4 V			-3.2			-3.2	mA
		B input	1				-4.8			-3.2]
1	Ch : - : - : 8		V	SN54'	-20		-57	-20		-57	mA
los	Short-circuit output current §		V _{CC} = MAX	SN74'	-18		-57	-18		-57	1 ""
Icc	Supply current		V _{CC} = MAX, See No	te 3		29	42		26	39	mA

[†]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTE 3: I_{CC} is measured with all outputs open, both R₀ inputs grounded following momentary connection to 4.5 V, and all other inputs grounded.

switching characteristics, VCC = 5 V, TA = 25°C

	FROM	FROM TO TEST CONDITIONS			′290			'293		UNIT
PARAMETER#	(INPUT)	(OUTPUT)	1E21 CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	0.411
	Α	QΑ		32	42		32	42		MHz
f _{max}	В	QΒ		16			16			1411.12
t _{PLH}	Α	0.			10	16		10	16	ns
[‡] PHL	1 ^	·QΑ	C _L = 15 pF, R _L = 400 Ω, See Note 4		12	18		12	18	1
t _{PLH}	А	0-			32	48		46	70	70 ns
^t PHL	1 ^	σ_{D}			34	50		46	70	1.3
^t PLH	В	0-			10	16		10	16	ns
^t PHL	1 B	ΩB			14	21		14	21	1
^t PLH		0-	Jee Note 4		21	32		21	32	ns
^t PHL	В	σC			23	35		23	35	113
^t PLH			1		21	32		34	51	ns
^t PHL	В	σD			23	35		34	51	1113
tpHL	Set-to-0	Any			26	40		26	40	ns
tPLH	0-11-0	Q_A, Q_D			20	30				ns
tPHL.	Set-to-9	Q _B , Q _C	1		26	40				<u> </u>

 $^{\#}f_{max}$ = maximum count frequency



 $[\]ddagger$ All typical values are at $V_{CC} = 5 \text{ V}$, $T_{A} = 25^{\circ}\text{C}$.

Not more than one output should be shorted at a time.

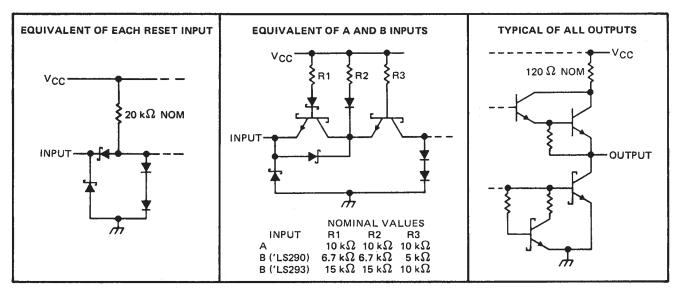
[¶]Q_A outputs are tested at I_{OL} = 16 mA plus the limit value of I_{IL} for the B input. This permits driving the B input while maintaining full fan-out capability.

tpLH = propagation delay time, low-to-high-level output

tPHL = propagation delay time, high-to-low-level output

NOTE 4: Load circuits and voltage waveforms are shown in Section 1.

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC (see Note 5)		,	٧
Input voltage: R inputs			V
Operating free-air temperature range: SN54LS29	0, SN54LS293	3 –55°C to 125°	С
SN74LS29	0, SN74LS293	3 0°C to 70°	С
Storage temperature range			C

NOTE 5: Voltage values are with respect to network ground terminal.

recommended operating conditions

		5	N54LS	,	:	SN74LS'		
		MIN	NOM	MAX	MIN	NOM	MAX	דומט
Supply voltage, VCC		4.5	5	5.5	4.75	5	5.25	V
High-level output current, IOH				-400			-400	μА
Low-level output current, IOL				4			8.	mA
	A input	0		32	0		32	MHz
Count frequency, f _{count}	B input	0		16	0		16 "	141112
	A input	15			15			
Pulse width, tw	B input	30			30			ns
	Reset inputs	30			30			
Reset inactive-state setup time, t _{Su}		25			25			ns
Operating free-air temperature, TA		-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

					+		SN54LS	•		SN74LS	.	
	PARAMET	ER	TES	ST CONDITIONS	51	MIN	TYP‡	MAX	MIN	TYP‡	MAX	UNIT
VIH	High-level inpu	t voltage				2			2			٧
VIL	Low-level input	voltage						0.7			0.8	V
VIK	Input clamp vo	Itage	V _{CC} = MIN,	I _I = -18 mA				-1.5			-1.5	V
	High-level outp	ut voltage	V _{CC} = MIN, V _{IL} = V _{IL} max,	V _{IH} = 2 V,		2.5	3.4		2.7	3.4		v
VOL	Low-level outp	ut voltage	VCC = MIN,	V _{1H} = 2 V,	1 _{OL} = 4 mA¶		0.25	0.4		0.25	0.4	v
		Any reset	V ₁ L = V ₁ L max V _{CC} = MAX,	V ₁ = 7 V	IOL = 8 mA¶			0.1		0.35	0.1	
	Input current	A input		· · · · · · · · · · · · · · · · · · ·				0.2			0.2	
Ч	at maximum	B of 'LS290	V _{CC} = MAX,	V _i = 5.5 V				0.4			0,4	mA
	input voltage	B of 'LS293		·				0.2			0.2	
		Any reset						20			20]
	High-level	A input		V = 0.7.V				40			40	
lіН	input current	B of 'LS290	V _{CC} = MAX,	V ₁ = 2.7 V				80			80	μΑ
		B of 'LS293						40			40	
		Any reset						-0.4			-0.4	
1	Low-level	A input	\\ \\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\	V ₁ = 0,4 V				-2.4			-2.4	mA
ИL	input current	B of 'LS290	V _{CC} = MAX,	V - 0.4 V				-3.2			-3.2	'''`
		B of 'LS293						-1.6			-1.6	
los	Short-circuit or	utput current §	V _{CC} = MAX			-20		-100	-20		-100	mA
laa	Supply current		V _{CC} = MAX,	See Note 3	'LS290		9	15		9	15	mA
1CC	Supply cultent		*CC - MAA,	003 14016 0	'LS293		9	15	l	9	15	

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

switching characteristics, VCC = 5 V, TA = 25°C

PARAMETER#	FROM	то	TEST COMPLETIONS	'LS290			'LS293			UNIT
	(INPUT)	(OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	CIAII
	Α	QA		32	42		32	42		MHz
^f max	В	QB		16			16			IVIII
^t PLH	A	0.	Ì		10	16		10	16	ns
tpHL	1 ^	QA	C _L = 15 pF, R _L = 2 kΩ, See Note 4		12	18		12	18	
t _{PLH}		0-			32	48		46	70	ns
tPHL	A	σ_{D}			34	50		46	70	
^t PLH	В	0-			10	16		10	16	ns ns
†PHL	1 6	QB			14	21		14	21	
tPLH		0 =			21	32		21	32	
^t PHL	В	αc			23	35		23	35	
^t PLH					21	32		34	51	ns
tPHL	В	σD			23	35		34	51	
t _{PHL}	Set-to-0	Any	1		26	40		26	40	ns
^t PLH	0 0	Q_A, Q_D	1		20	30				ns
†PHL	Set-to-9	Q _B , Q _C	1		26	40] '''

[#]fmax = maximum count frequency

NOTE 4: Load circuits and voltage waveforms are shown in Section 1.



 $^{^{\}ddagger}$ All typical values are at $V_{CC} = 5 \text{ V}$, $T_{\Delta} = 25^{\circ}\text{C}$.

Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

[¶]QA outputs are tested at specified IOL plus the limit value of IIL for the B input. This permits driving the B input while maintaining full fan-out capability.

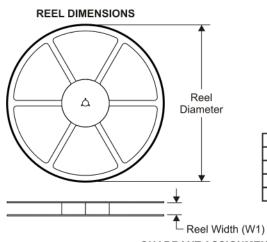
NOTE 3: I_{CC} is measured with all outputs open, both R₀ inputs grounded following momentary connection to 4.5 V, and all other inputs grounded.

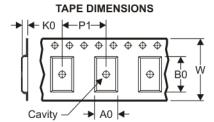
tpLH = propagation delay time, low-to-high-level output

tpHL = propagation delay time, high-to-low-level output



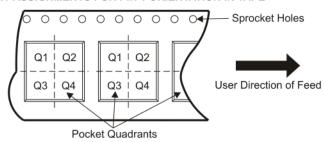
TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	_	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS293DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1





*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS293DR	SOIC	D	14	2500	346.0	346.0	33.0

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