19-4583; Rev 0; 4/09

MAXIM

Dual PCI Express Equalizer/Redriver

General Description

The MAX4950A dual PCI Express® (PCIe) equalizer/redriver operates from a single +3.3V supply. This device improves signal integrity at the receiver through programmable input equalization and redrive circuitry with output deemphasis to correct for high-frequency losses. This device permits optimal placement of key PCIe components and longer runs of stripline, microstrip, or cable.

The MAX4950A contains two identical channels capable of equalizing PCIe Gen I (2.5GT/s) and Gen II (5.0GT/s) signals. The MAX4950A features electrical idle and receiver detection on each channel and a power-saving mode.

The MAX4950A is available in a small 36-pin (6.0mm x 6.0mm) TQFN package with flowthrough traces for optimal layout and minimal space requirements. The MAX4950A is specified over the 0°C to +70°C commercial operating temperature range.

Applications

Servers

Industrial PCs

Test Equipment

Computers

External Graphics Applications

Communications Switchers

Storage Area Networks

PCI Express is a registered trademark of PCI-SIG Corp.

Features

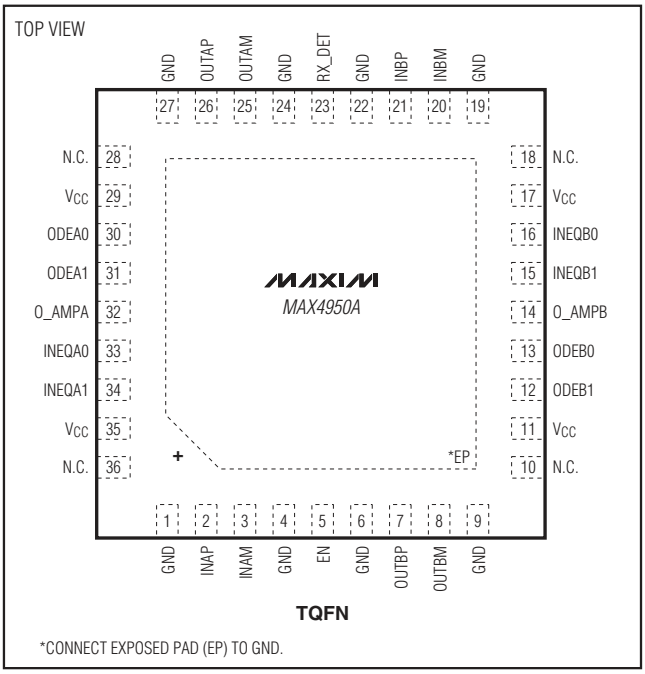
- **Single +3.3V Supply Operation**
- **PCIe Gen I (2.5GT/s) and Gen II (5.0GT/s) Capable**
  Excellent Differential Return Loss:
  ≥ 8dB (f = 1.25GHz to 2.5GHz)
- **Very Low Latency with 280ps (typ) Propagation Delay**
- **Individual Lane Detection**
- **Three-Level Programmable Input Equalization**
- **Three-Level Programmable Output Deemphasis**
- **Standard, -2.5dB Programmable Output Levels**
- **On-Chip 50Ω Input/Output Terminations**
- **Space-Saving, 6.0mm x 6.0mm TQFN Package**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX4950ACTX+T	0°C to +70°C	36 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*
T = Tape and reel.

Pin Configuration



Dual PCI Express Equalizer/Redriver

ABSOLUTE MAXIMUM RATINGS

(Voltages referenced to GND.)
V_{CC} .....-0.3V to +4.0V
All Other Pins (Note 1).....-0.3V to (V_{CC} + 0.3V)
Continuous Current IN_P, IN_M, OUT_P, OUT_M .....±30mA
Peak Current IN_P, IN_M, OUT_P, OUT_M
(pulsed for 1µs, 1% duty cycle).....±100mA
Continuous Power Dissipation (T_A = +70°C)
36-Pin TQFN (derate 35.7mW/°C above +70°C) 2857mW
Junction-to-Case Thermal Resistance (θ_{JC}) (Note 2)
36-Pin TQFN.....1°C/W
Junction-to-Ambient Thermal Resistance (θ_{JA}) (Note 2)
36-Pin TQFN.....28°C/W
Operating Temperature Range.....0°C to +70°C
Junction Temperature Range .....-40°C to +150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Note 1: All I/O pins are clamped by internal diodes.
Note 2: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +3.6V, C_{CL} = 75nF coupling capacitor on each output, R_L = 50Ω resistor on each output, T_A = 0°C to +70°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V and T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC PERFORMANCE						
Power-Supply Range	V_{CC}		3.0		3.6	V
Supply Current	I_{CC}	EN = V_{CC}, V_{O_AMPA} = V_{GND}, V_{O_AMPB} = V_{GND} (Note 4)		130	165	mA
Differential Input Impedance	$Z_{RX-DIFF-DC}$	DC	80	100	120	Ω
Differential Output Impedance	$Z_{TX-DIFF-DC}$	DC	80	100	120	Ω
Common-Mode Resistance to GND	$Z_{RX-HIGH-IMP-DC-POS}$	V_{IN_P} = V_{IN_M} = 0 to +200mV, input terminations not powered	50			kΩ
Common-Mode Resistance to GND	$Z_{RX-HIGH-IMP-DC-NEG}$	V_{IN_P} = V_{IN_M} = -150mV to 0, input terminations not powered	1			kΩ
Common-Mode Resistance to GND, Input Terminations Powered	Z_{RX-DC}		40	50	60	Ω
Output Short-Circuit Current	$I_{TX-SHORT}$	Single-ended			90	mA
Common-Mode Delta Between Active and Idle States	$V_{TX-CM-DC-ACTIVE-IDLE-DELTA}$	$V_{O\_AMP\_}$ = V_{GND}			100	mV
DC Output Offset During Active State	$V_{TX-CM-DC-LINE-DELTA}$	$\lvert V_{OUT\_P} - V_{OUT\_M} \rvert$			25	mV
DC Output Offset During Electrical Idle	$V_{TX-IDLE-DIFF-DC}$	$\lvert V_{OUT\_P} - V_{OUT\_M} \rvert$			10	mV
AC PERFORMANCE						
Differential Input Return Loss (Note 5)	$RL_{RX-DIFF}$	f = 0.05GHz to 1.25GHz	10			dB
		f = 1.25GHz to 2.5GHz	8			
Common-Mode Input Return Loss (Note 5)	RL_{RX-CM}	f = 0.05GHz to 2.5GHz	6			dB

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +3.0V to +3.6V, C_{CL} = 75nF coupling capacitor on each output, R_L = 50Ω resistor on each output, T_A = 0°C to +70°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V and T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Differential Output Return Loss (Note 5)	$RL_{TX-DIFF}$	f = 0.05GHz to 1.25GHz	10			dB
		f = 1.25GHz to 2.5GHz	8			
Common-Mode Output Return Loss (Note 5)	RL_{TX-CM}	f = 0.05GHz to 2.5GHz	6			dB
Redriver-Operation Differential Input Signal Range	$V_{RX-DIFF-PP}$	f = 0.05GHz to 2.5GHz	120		1200	mV_{P-P}
Full-Swing No-Deemphasis Differential Output Voltage	$V_{TX-DIFF-PP}$	$ABS\|V_{OUT\_P} - V_{OUT\_M}\|$; O_AMP_ = GND	800	1000	1200	mV_{P-P}
Low-Swing No-Deemphasis Differential Output Voltage	$V_{TX-DIFF-PP-LOW}$	$ABS\|V_{OUT\_P} - V_{OUT\_M}\|$; O_AMP_ = V_{CC}	600	750	900	mV_{P-P}
Output Deemphasis Ratio, 0dB	$V_{TX-DE-RATIO-0dB}$	f = 2.5GHz, ODE_1 = GND, ODE_0 = GND, Figure 1 (see Table 3)		0		dB
Output Deemphasis Ratio, 3.5dB	$V_{TX-DE-RATIO-3.5dB}$	f = 2.5GHz, ODE_1 = GND, ODE_0 = V_{CC}, Figure 1 (see Table 3)		3.5		dB
Output Deemphasis Ratio, 6dB	$V_{TX-DE-RATIO-6dB}$	f = 2.5GHz, ODE_1 = V_{CC}, ODE_0 = V_{CC} or GND, Figure 1 (see Table 3)		6		dB
Input Equalization, 0dB (Note 6)	$V_{RX-EQ-0dB}$	f = 2.5GHz, INEQ_1 = GND, INEQ_0 = GND (see Table 2)		0		dB
Input Equalization, 3.5dB (Note 6)	$V_{RX-EQ-3.5dB}$	f = 2.5GHz, INEQ_1 = GND, INEQ_0 = V_{CC} (see Table 2)		3.5		dB
Input Equalization, 6dB (Note 6)	$V_{RX-EQ-6dB}$	f = 2.5GHz, INEQ_1 = V_{CC}, INEQ_0 = V_{CC} or GND (see Table 2)		6		dB
Output Common-Mode Voltage	$V_{TX-CM-AC-PP}$	$MAX(V_{OUT\_P} + V_{OUT\_M})/2 - MIN(V_{OUT\_P} + V_{OUT\_M})/2$			100	mV_{P-P}
Propagation Delay (Note 5)	T_{PD}	f = 2.5GHz	160	280	400	ps
Rise/Fall Time	$T_{TX-RISE-FALL}$	(Note 7)	30			ps
Rise/Fall Time Mismatch	$T_{TX-RF-MIISMATCH}$	(Note 7)			20	ps
Same-Pair Output Skew (Note 5)	T_{SK}	f = 2.5GHz		10	15	ps
Lane-to-Lane Output Skew (Note 5)	T_{SKL}	f = 2.5GHz	-50		+50	ps
Deterministic Jitter (Note 5)	$T_{TX-DJ-DD}$	K28.5± pattern, 5.0GT/s, AC coupled, R_L = 50Ω, effects of deemphasis deembedded			15	ps_{P-P}
Random Jitter	$T_{TX-RJ-DD}$	DIO.2 pattern			1.4	ps_{RMS}
Electrical Idle Entry Delay	$T_{TX-IDLE-SET-TO-IDLE}$	From input to output		15		ns
Electrical Idle Exit Delay	$T_{TX-IDLE-TO-DIFF-DATA}$	From input to output		12		ns

Dual PCI Express Equalizer/Redriver

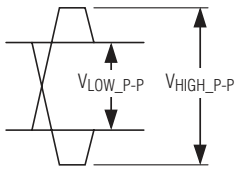
ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +3.0V to +3.6V, C_{CL} = 75nF coupling capacitor on each output, R_L = 50Ω resistor on each output, T_A = 0°C to +70°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V and T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Electrical Idle Detect Threshold	$V_{TX-IDLE-THRESH}$		65	95	120	mV_{P-P}
Output Voltage During Electrical Idle (AC)	$V_{TX-IDLE-DIFF-AC-P}$	$ABS\lvert V_{OUT\_P} - V_{OUT\_M}\rvert$, f = 500MHz			25	mV_{P-P}
Receiver Detect Pulse Amplitude (Note 5)	$V_{TX-RCV-DETECT}$	Voltage change in positive direction			600	mV
Receiver Detect Pulse Width				100		ns
Receiver Detect Retry Period				200		ns
CONTROL LOGIC (INEQ_1, INEQ_0, ODE_1, ODE_0, EN, RX_DET, O_AMP_)						
Input Logic-Level Low	V_{IL}				0.6	V
Input Logic-Level High	V_{IH}		1.4			V
Input Logic Hysteresis	V_{HYST}			130		mV
Input Leakage Current	I_{IN}	$V_{CONTROL\_LOGIC}$ = +0.5V or +1.5V	-50		+50	µA

Note 3: All devices are 100% production tested at T_A = +70°C. Specifications for all temperature limits are guaranteed by design.
Note 4: Currents are applicable for both PCIe Generation I and Generation II speeds. Table 5 summarizes the predicted power consumption.
Note 5: Guaranteed by design, unless otherwise noted.
Note 6: Equivalent to the same amount of deemphasis driving the output.
Note 7: Rise and fall times are measured using 20% and 80% levels.

Timing Diagram



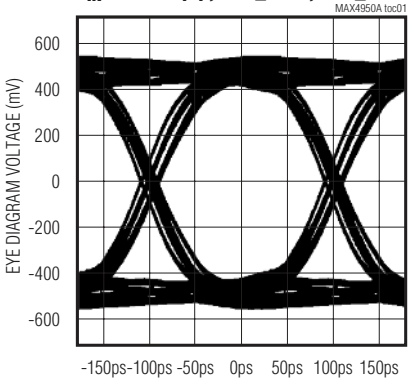
$$PE(dB) = 20\left[\log\left(\frac{V_{HIGH\_P-P}}{V_{LOW\_P-P}}\right)\right]$$

Figure 1. Illustration of Output Deemphasis

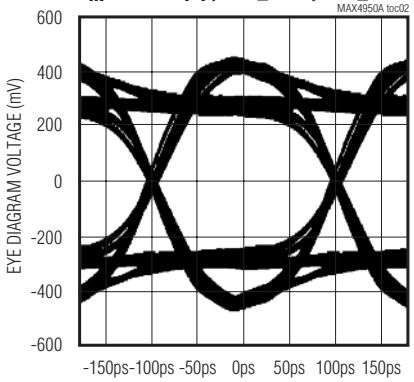
Typical Operating Characteristics

(V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.)

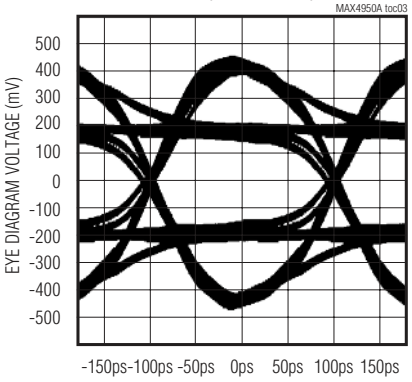
INEQ_0 = INEQ_1 = 0, O_AMP_ = 0, V_{IN} = 200mV_{P-P}, ODE_0 = 0, ODE_1 = 0



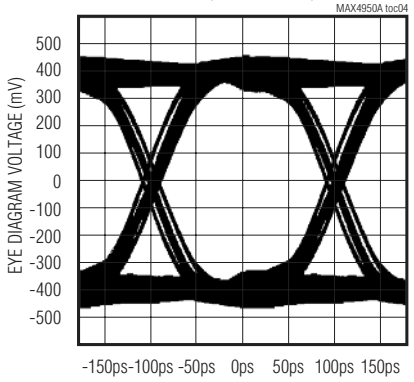
INEQ_0 = INEQ_1 = 0, O_AMP_ = 0, V_{IN} = 200mV_{P-P}, ODE_0 = 1, ODE_1 = 0



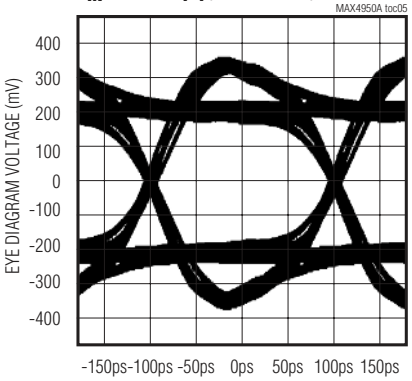
INEQ_0 = INEQ_1 = 0, O_AMP_ = 0, V_{IN} = 200mV_{P-P}, ODE_0 = 0, ODE_1 = 1



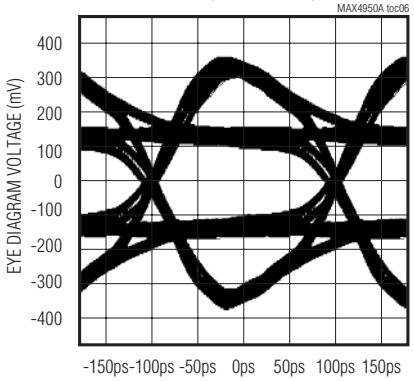
INEQ_0 = INEQ_1 = 0, O_AMP_ = 1, V_{IN} = 200mV_{P-P}, ODE_0 = 0, ODE_1 = 0



INEQ_0 = INEQ_1 = 0, O_AMP_ = 1, V_{IN} = 200mV_{P-P}, ODE_0 = 1, ODE_1 = 0



INEQ_0 = INEQ_1 = 0, O_AMP_ = 1, V_{IN} = 200mV_{P-P}, ODE_0 = 0, ODE_1 = 1

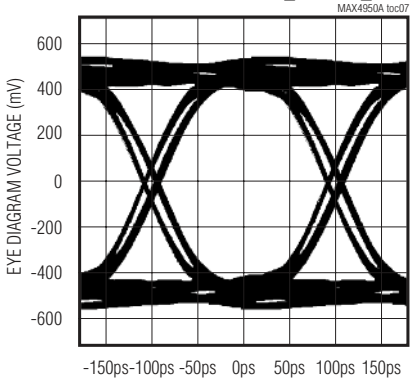


Dual PCI Express Equalizer/Redriver

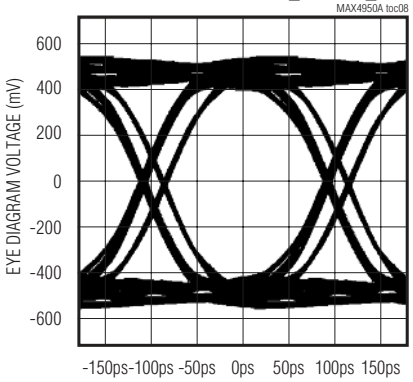
Typical Operating Characteristics (continued)

(V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.)

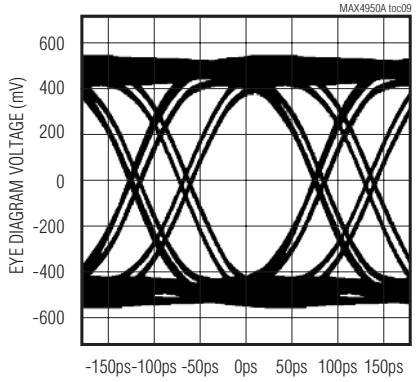
INEQ_0 = 1, INEQ_1 = 0, O_AMP_ = 0, V_{IN} = 500mV$_{P-P}$, WITH 6in STRIPLINE ODE_0 = ODE_1 = 0



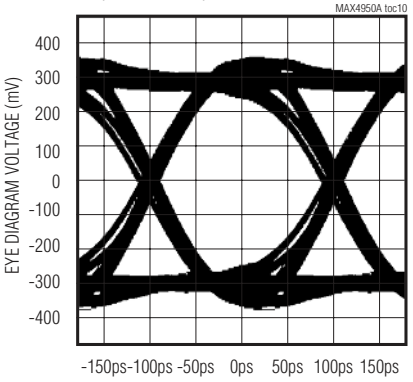
INEQ_0 = 0, INEQ_1 = 1, O_AMP_ = 0, V_{IN} = 500mV$_{P-P}$, WITH 19in STRIPLINE ODE_0 = ODE_1 = 0



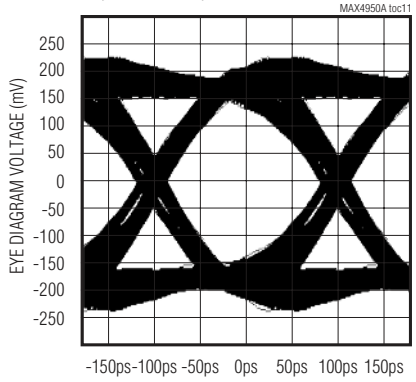
INEQ_0 = INEQ_1 = 0, O_AMP_ = 0, V_{IN} = 500mV$_{P-P}$, WITH 19in STRIPLINE ODE_0 = ODE_1 = 0



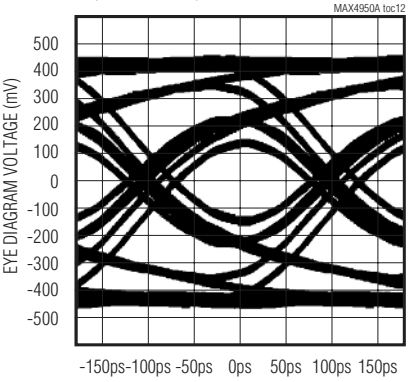
INEQ_0 = INEQ_1 = 0, O_AMP_ = 1, V_{IN} = 200mV$_{P-P}$, ODE_0 = 1, ODE_1 = 0, OUTPUT AFTER 6in STRIPLINE



INEQ_0 = INEQ_1 = 0, O_AMP_ = 0, V_{IN} = 200mV$_{P-P}$, ODE_0 = 0, ODE_1 = 1, OUTPUT AFTER 19in STRIPLINE



INEQ_0 = INEQ_1 = 0, O_AMP_ = 0, V_{IN} = 200mV$_{P-P}$, ODE_0 = 0, ODE_1 = 0, OUTPUT AFTER 19in STRIPLINE



Pin Description

PIN	NAME	FUNCTION
1, 4, 6, 9, 19, 22, 24, 27	GND	Ground
2	INAP	Noninverting Input A
3	INAM	Inverting Input A
5	EN	Enable Input. Drive EN low for standby mode. Drive EN high for normal mode. EN is internally pulled down by a 50kΩ (typ) resistor.
7	OUTBP	Noninverting Output B
8	OUTBM	Inverting Output B
10, 18, 28, 36	N.C.	No Connection. Not internally connected.
11, 17, 29, 35	V_{CC}	Power-Supply Input. Bypass V_{CC} to GND with 1µF and 0.01µF capacitors in parallel as close as possible to the device.
12	ODEB1	Output B Deemphasis Control MSB. ODEB1 is internally pulled down by a 50kΩ (typ) resistor. See Table 3.
13	ODEB0	Output B Deemphasis Control LSB. ODEB0 is internally pulled down by a 50kΩ (typ) resistor. See Table 3.
14	O_AMPB	Output B Amplitude Selection Input. O_AMPB is internally pulled down by a 50kΩ (typ) resistor.
15	INEQB1	Input B Equalization Control MSB. INEQB1 is internally pulled down by a 50kΩ (typ) resistor. See Table 2.
16	INEQB0	Input B Equalization Control LSB. INEQB0 is internally pulled down by a 50kΩ (typ) resistor. See Table 2.
20	INBM	Inverting Input B
21	INBP	Noninverting Input B
23	RX_DET	Receiver-Detection Control Bit. Toggle RX_DET to initiate receiver detection. RX_DET is internally pulled down by a 50kΩ (typ) resistor.
25	OUTAM	Inverting Output A
26	OUTAP	Noninverting Output A
30	ODEA0	Output A Deemphasis Control LSB. ODEA0 is internally pulled down by a 50kΩ (typ) resistor. See Table 3.
31	ODEA1	Output A Deemphasis Control MSB. ODEA1 is internally pulled down by a 50kΩ (typ) resistor. See Table 3.
32	O_AMPA	Output A Amplitude Selection Input. O_AMPA is internally pulled down by a 50kΩ (typ) resistor.
33	INEQA0	Input A Equalization Control LSB. INEQA0 is internally pulled down by a 50kΩ (typ) resistor. See Table 2.
34	INEQA1	Input A Equalization Control MSB. INEQA1 is internally pulled down by a 50kΩ (typ) resistor. See Table 2.
—	EP	Exposed Pad. Internally connected to GND. Connect EP to a large ground plane to maximize thermal performance. EP is not intended as an electrical connection point.

Dual PCI Express Equalizer/Redriver

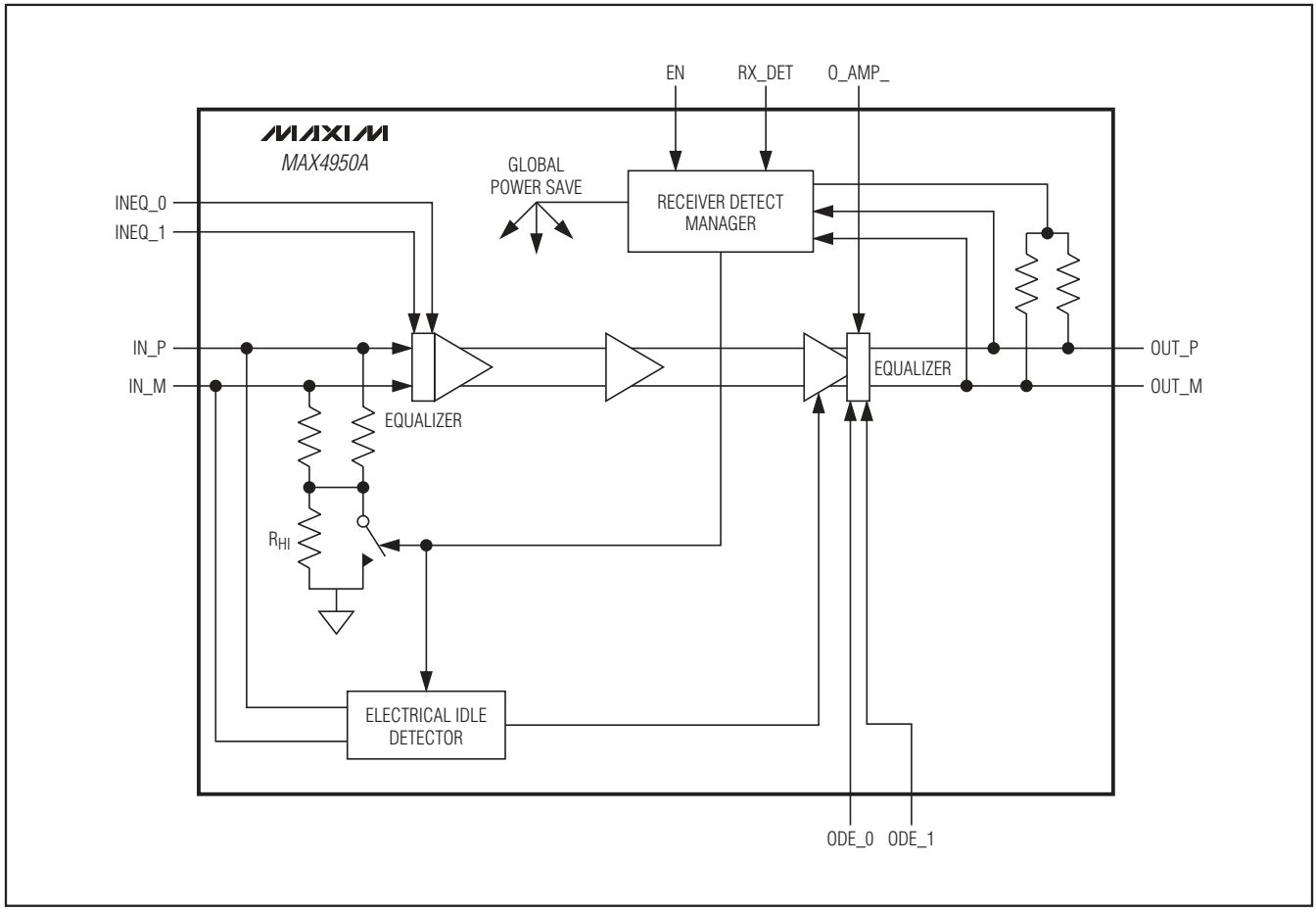


Figure 2. Block Diagram of Each Channel

Detailed Description

The MAX4950A dual equalizer/redriver is designed to support both Gen I (2.5GT/s) and Gen II (5.0GT/s) PCIe data rates. The device contains two identical drivers with idle/receive detect on each lane and equalization to compensate for circuit-board loss. Signal integrity at the receiver is improved by the use of programmable input equalization circuitry. The MAX4950A features individual channel output amplitude selection inputs, O_AMPA and O_AMPB (Table 1), and programmable output deemphasis, permitting optimal placement of key PCIe components and longer runs of stripline, microstrip, or cable.

Table 1. Output Amplitude Selection

O_AMPA/ O_AMPB	DIFFERENTIAL OUTPUT VOLTAGE (mV_{P-P})
0	1000 (typ)
1	750 (typ)

Programmable Input Equalization

The MAX4950A features programmable input equalizers capable of providing 0dB, 3.5dB, or 6dB of high-frequency boost on either channel (see Table 2).

Table 2. Input Equalization

INEQ_1	INEQ_0	INPUT EQUALIZATION (dB)
0	0	0
0	1	3.5 (typ)
1	X	6 (typ)

X = Don't care.

Programmable Output Deemphasis

The MAX4950A features programmable output deemphasis on either channel by setting two control bits, ODE_1 and ODE_0, for deemphasis ratios of 0dB, 3.5dB, and 6dB (see Table 3).

Table 3. Output Deemphasis

ODE_1	ODE_0	OUTPUT DEEMPHASIS RATIO (dB)
0	0	0
0	1	3.5 (typ)
1	X	6 (typ)

X = Don't care.

Receiver Detection

The MAX4950A features receiver detection on each channel. Upon initial power-up, if EN is high, receiver detection initializes. Receiver detection can also be initiated on a rising or falling edge of the RX_DET input when EN is high. During this time, the part remains in low-power standby mode and the outputs are squelched, despite the logic-high state of EN. Once started, receiver detection repeats indefinitely on each channel. Once a receiver is detected on one of the channels, up to three more attempts are made on the other channel. Upon receiver detection, channel output and electrical idle detection are enabled (see Table 4).

Table 4. Receiver-Detection Input Function

RX_DET	EN	DESCRIPTION
X	0	Receiver detection inactive
0	1	Following a rising or falling edge, indefinite retry until receiver detected
Rising or Falling Edge	1	Initiate receiver detection
1	1	Following a rising or falling edge, indefinite retry until receiver detected

X = Don't care.

Electrical Idle Detection

The MAX4950A features electrical idle detection to prevent unwanted noise from being redriven at the output. If the MAX4950A detects that the differential input has fallen below $V_{TX-IDLE-THRESH}$, the MAX4950A squelches the output. For differential input signals that are above $V_{TX-IDLE-THRESH}$, the MAX4950A turns on the output and redrives the signal.

Power-Saving Features

The MAX4950A features an enable input (EN) to shut down the device and reduce supply current. To place the device in shutdown mode, drive EN low. To enable the device, drive EN high. During normal operation, supply current can also be reduced by reducing the channel output amplitudes. Table 5 shows typical power consumption differences between shutdown mode and normal operation with different output redrive strengths.

Dual PCI Express Equalizer/Redriver

Table 5. Quiescent Power Dissipation with Equalization and Deemphasis

EN	O_AMPB	O_AMPA	QUIESCENT POWER SUPPLY CURRENT (typ) (mA)	QUIESCENT POWER SUPPLY CURRENT (max) (mA)	QUIESCENT POWER DISSIPATION (3.3V, typ) (mW)	QUIESCENT POWER DISSIPATION (3.6V, max) (mW)
0	0	0	60	75	198	270
0	0	1	55	68	182	243
0	1	0	55	68	182	243
0	1	1	50	60	165	216
1	0	0	130	165	429	594
1	0	1	125	157	413	565
1	1	0	125	157	413	565
1	1	1	120	150	396	540

Applications Information

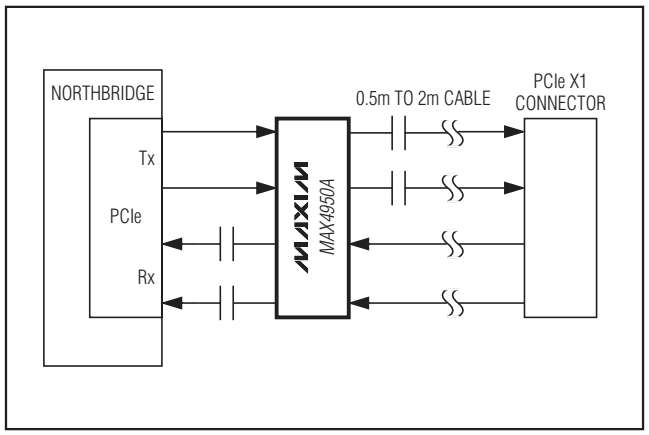


Figure 3. Typical Application Circuit—MAX4950A Used as X1 Lane Cable Driver

Layout

Circuit-board layout and design can significantly affect the performance of the MAX4950A. Use good high-frequency design techniques, including minimizing ground inductance and using controlled-impedance transmission lines on data signals. It is recommended to run receive and transmit on different layers to minimize crosstalk and to place power-supply decoupling capacitors as close as possible to V_{CC}. Always connect V_{CC} to a power plane.

Exposed Pad Package

The exposed-pad, 36-pin, TQFN package incorporates features that provide a very low thermal resistance path for heat removal from the IC. The exposed pad on the MAX4950A must be soldered to the circuit-board ground plane for proper thermal performance. For more information on exposed-pad packages, refer to Maxim Application Note HFAN-08.1: *Thermal Considerations of QFN and Other Exposed-Paddle Packages*.

Power-Supply Sequencing

Caution: Do not exceed the absolute maximum ratings because stresses beyond the listed ratings may cause permanent damage to the device.

Proper power-supply sequencing is recommended for all devices. Always apply GND then V_{CC} before applying signals, especially if the signal is not current limited.

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
36 TQFN	T3666+2	21-0141