HSP48901

3 x 3 Image Filter

FN2459
Rev 6.00
July 2004

The Intersil HSP48901 is a high speed 9-Tap FIR Filter which utilizes 8-bit wide data and coefficients. It can be configured as a one-dimensional (1-D) 9-Tap filter for a variety of signal processing applications, or as a two dimensional (2-D) filter for image processing. In the 2-D configuration, the device is ideally suited for implementing 3 x 3 kernel convolution. The 30MHz clock rate allows a large number of image sizes to be processed within the required frame time for real-time video.

Data is provided to the HSP48901 through the use of programmable data buffers such as the HSP9500 or any other Programmable Shift Register. Coefficient and pixel input data are 8-bit signed or unsigned integers, and the 20-bit extended output guarantees no overflow will occur during the filtering operation.

There are two internal register banks for storing independent 3 x 3 filter kernels, thus, facilitating the implementation of adaptive filters and multiple filter operations on the same data.

The configuration of the HSP48901 Image Filter is controlled through a standard microprocessor interface and all inputs and outputs are TTL compatible.

Features

- DC to 30MHz Clock Rate
- Configurable for 1-D and 2-D Correlation/Convolution
- Dual Coefficient Mask Registers, Switchable in a Single Clock Cycle
- Two's Complement or Unsigned 8-Bit Input Data and Coefficients
- 20-Bit Extended Precision Output
- Standard µP Interface

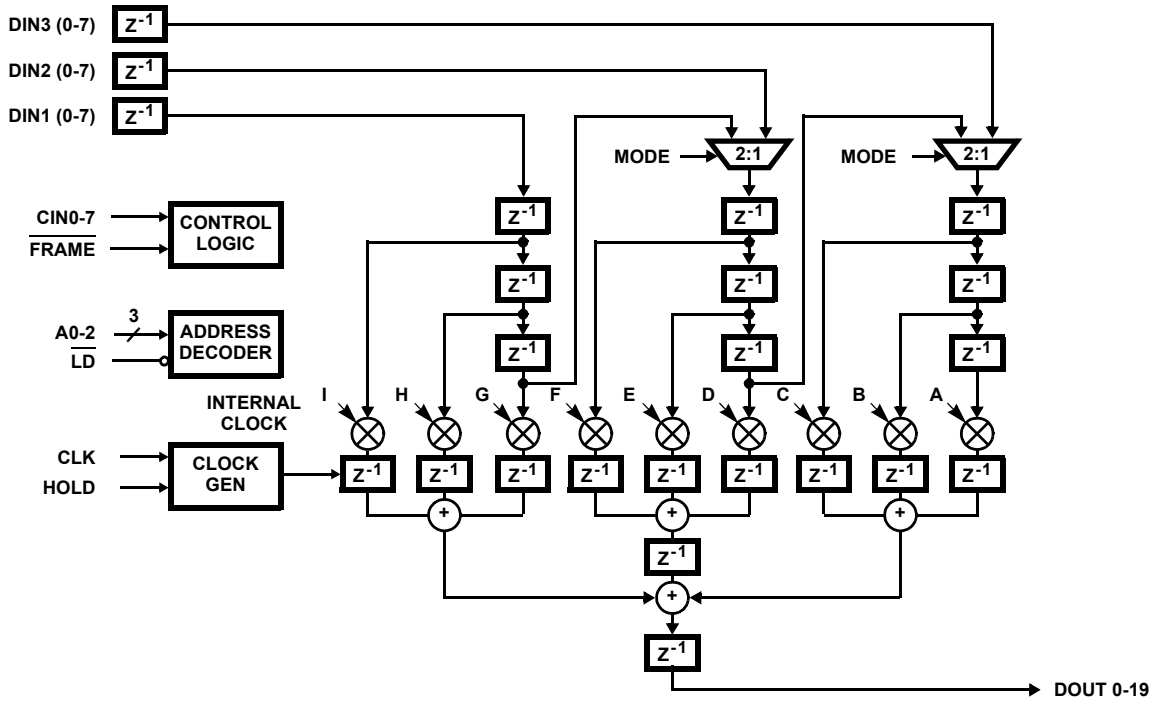
Applications

- Image Filtering
- Edge Detection/Enhancement
- Pattern Matching
- Real Time Video Filters

Ordering Information

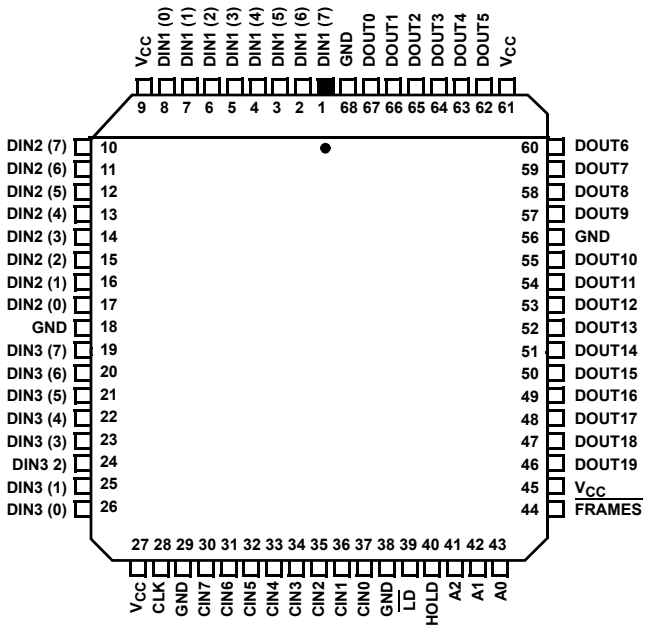
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
HSP48901JC-30	0 to 70	68 Ld PLCC	N68.95

Block Diagram



Pinouts

68 LEAD PLCC
TOP VIEW



Pin Descriptions

NAME	PLCC PIN	TYPE	DESCRIPTION
V_{CC}	9, 27, 45, 61		The +5V power supply pins. 0.1µF capacitors between the V_{CC} and GND pins are recommended.
GND	18, 29, 38, 56		The device ground.
CLK	28	I	Input and System clock. Operations are synchronous with the rising edge of this clock signal.
DIN1(7-0)	1-8	I	Pixel Data Input Bus #1. These inputs are used to provide 8-bit pixel data to the HSP48901. The data must be provided in a synchronous fashion, and is latched on the rising edge of the CLK signal. The DIN1(0-7) inputs are also used to input data when operating in the 9-Tap FIR mode.
DIN2(7-0)	10-17	I	Pixel Data Input Bus #2. Same as above. These inputs should be grounded when operating in the 1D mode.
DIN3(7-0)	19-26	I	Pixel Data Input Bus #3. Same as above. These inputs should be grounded when operating in the 1D mode.
CIN7-0	30-37	I	Coefficient Data Input Bus. This input bus is used to load the Coefficient Mask Register(s) and the Initialization Register. The register to be loaded is defined by the register address bits A0-2. The CIN0-7 data is loaded to the addressed register through the use of the $\overline{LD}$ input.
DOUT19-0	46-55, 57-60, 62-67	O	Output Data Bus. This 20-Bit output port is used to provide the convolution result. The result is the sum of products of the input data samples and their corresponding coefficients.
$\overline{FRAME}$	44	I	$\overline{FRAME}$ is an asynchronous new frame or vertical sync input. A low on this input resets all internal circuitry except for the Coefficient and INT Registers. Thus, after a $\overline{FRAME}$ reset has occurred, a new frame of pixels may be convolved without reloading these registers.
HOLD	40	I	The Hold Input is used to gate the clock from all of the internal circuitry of the HSP48901. This signal is synchronous, is sampled on the rising edge of CLK and takes effect on the following cycle. While this signal is active (high), the clock will have no effect on the HSP48901 and internal data will remain undisturbed.
A2-0	41-43	I	Control Register Address. These lines are decoded to determine which register in the control logic is the destination for the data on the CIN0-7 inputs. Register loading is controlled by the A0-2 and $\overline{LD}$ inputs.
$\overline{LD}$	39	I	Load Strobe. $\overline{LD}$ is used for loading the Internal Registers of the HSP48901. The rising edge of $\overline{LD}$ will latch the CIN0-7 data into the register specified by A0-2. The Address on A0-2 must be setup with respect to the falling edge of $\overline{LD}$ and must be held with respect to the rising edge of $\overline{LD}$.

Functional Description

The HSP48901 can perform convolution of a 3 x 3 filter kernel with 8-bit image data. It accepts the image data in a raster scan, non-interlaced format, convolves it with the filter kernel and outputs the filtered image. The input and filter kernel data are both 8-bits, while the output data is 20 bits to prevent overflow during the convolution operation. Image data is input via the DIN1, DIN2, and DIN3 busses. This data would normally be provided by programmable data buffer such as the HSP9501 as illustrated in the Operations Section of this specification. The data is then convolved with the 3 x 3 array of filter coefficients. The resultant output data is then stored in the Output Register. The HSP48901 may also be used in a one-dimensional mode. In this configuration, it functions as a 1-D 9-tap FIR filter. Data would be input via the DIN1(0-7) bus for operation in this mode.

Initialization of the convolver is done using the CIN0-7 bus to load configuration data and the filter kernel(s). The address lines A0-2 are used to address the Internal Registers for initialization. The configuration data is loaded using the A0-2, CIN0-7 and $\overline{LD}$ controls as address, data and write enable, respectively. This interface is compatible with standard microprocessors without the use of any additional glue logic.

Filtered image data is output from the convolver over the DOUT0-19 bus. This output bus is 20 bits wide to provide room for growth during the convolution operation.

8-Bit Multiplier Array

The multiplier array consists of nine 8 x 8 multipliers. Each multiplier forms the product of a filter coefficient with a corresponding pixel in the input image. Input and coefficient data may be in either two's complement or unsigned integer format. The nine coefficients form a 3 x 3 filter kernel which is multiplied by the input pixel data and summed to form a sum of products for implementation of the convolution operation as shown below:

FILTER KERNEL			INPUT DATA		
A	B	C	P1	P2	P3
D	E	F	P4	P5	P6
G	H	I	P7	P8	P9

OUTPUT = (A x P1) + (B x P2) + (C x P3)
+ (D x P4) + (E x P5) + (F x P6)
+ (G x P7) + (H x P8) + (I x P9)

Control Logic

The control logic (Figure 1) contains the Initialization Register and the Coefficient Registers. The control logic is updated by placing data on the CIN0-7 bus and using the A0-2 and $\overline{LD}$ control lines to write to the addressed register (see Address Decoder). All of the Control Logic Registers are unaffected by $\overline{FRAME}$.

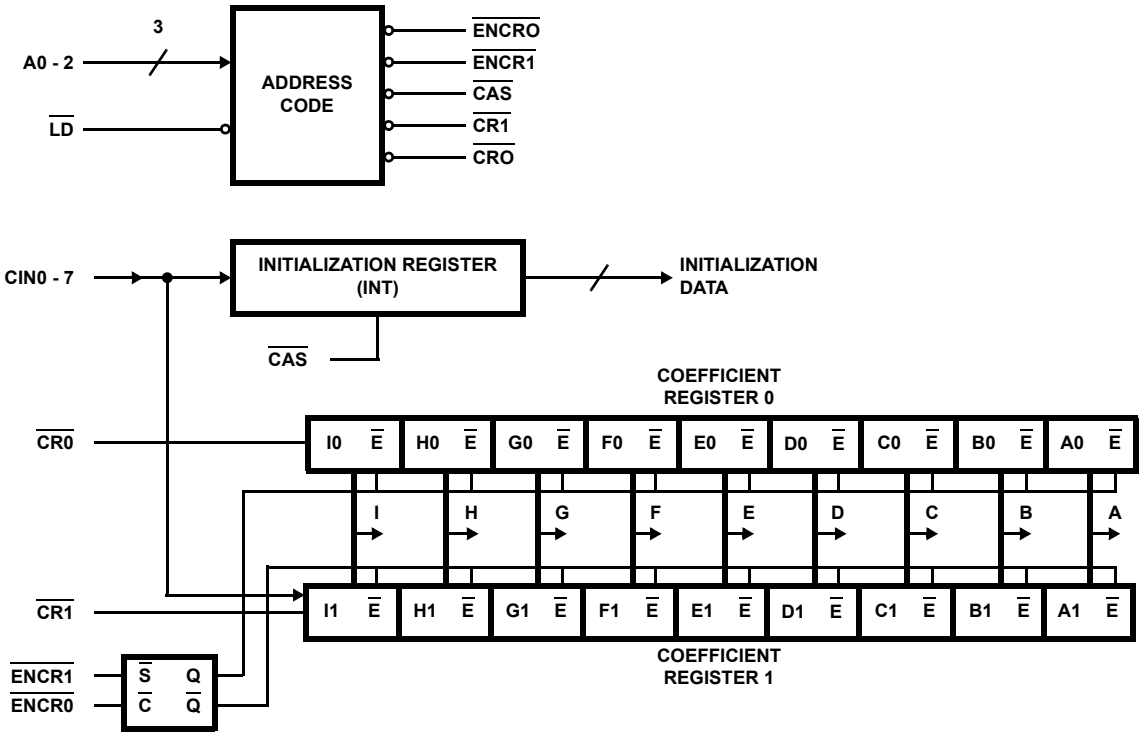


FIGURE 1. CONTROL LOGIC BLOCK DIAGRAM

Initialization Register

The Initialization Register is used to appropriately configure the convolver for a particular application. It is loaded through the use of the CIN0-7 bus along with the $\overline{LD}$ input. Bit-0 defines the input data and coefficients format (unsigned or two's complement); Bit-1 defines the mode of operation (1-D or 2-D); and Bit-2 and Bit-3 determine the type of rounding to occur on the DOUT0-19 bus; The complete definition of the Initialization Register bits is given in Table 1.

TABLE 1. INITIALIZATION REGISTER

INITIALIZATION REGISTER		
BIT 0		**FUNCTION = INPUT AND COEFFICIENT DATA FORMAT**
0		Unsigned Integer Format
1		Two's Complement Format
BIT 1		**FUNCTION = OPERATING MODE**
0		1-D 9-Tap Filter
1		2-D 3 x 3 Filter
3 BIT 2		**FUNCTION = OUTPUT ROUNDING**
0	0	No Rounding
0	1	Round to 16 Bits (i.e., DOUT19-4)
1	0	Round to 8 Bits (i.e., DOUT19-12)
1	1	Not Valid

Coefficient Registers (CREG0, CREG1)

The control logic contains two coefficient register banks, CREG0 and CREG1. Each of these register banks is capable of storing nine 8-bit filter coefficient values (3 x 3 Kernel). The output of the registers are connected to the coefficient input of the corresponding multiplier in the 3 x 3 multiplier array (designated A through I). The register bank to be used for the convolution is selectable by writing to the appropriate address (see address decoder). All registers in a given bank are enabled simultaneously, and one of the banks is always active.

For most applications, only one of the register banks is necessary. The user can simply load CREG0 after power up, and use it for the entire convolution operation. (CREG0 is the Default Register). The alternate register bank allows the user to maintain two sets of filter coefficients and switch between them in real time. The coefficient masks are loaded via the CIN0-7 bus by using A0-2 and $\overline{LD}$. The selection of the particular register bank to be used in processing is also done by writing to the appropriate address (See address decoder). For example, if CREG0 is being used to provide coefficients to the multipliers, CREG1 can be updated at a low rate by an external processor; then, at the proper time, CREG1 can be selected, so that the new coefficient mask is used to process the data. Thus, no clock cycles have been lost when changing between alternate 3 x 3 filter kernels.

The nine coefficients must be loaded sequentially over the CIN0-7 bus from A to I. The address of CREG0 or CREG1 is placed on A0-2, and then the coefficients are written to the corresponding Coefficient Register one at a time by using the $\overline{LD}$ input.

Address Decoder

The address decoder (see Figure 1) is used for writing to the control logic of the HSP48901. Loading an Internal Register is done by selecting the Destination Register with the A0-2 address lines, placing the data on CIN0-7, and asserting $\overline{LD}$ control line. When $\overline{LD}$ goes high, the data on CIN0-7 is latched into the addressed register. The address map for the A0-2 bus is shown in Table 2.

While loading of the control logic registers is asynchronous to CLK, the target register in the control logic is being read synchronous to the internal clock. Therefore, care must be taken when modifying the convolver setup parameters during processing to avoid changing the contents of the registers near a rising edge of CLK. The required setup time relative to CLK is given by the specification TLCS. For example, in order to change the active coefficient register from CREG0 to CREG1 during an active convolution operation, a write will be performed to the address for selecting CREG1 for internal processing (A0-2 = 110). In order to provide proper uninterrupted operation, $\overline{LD}$ should be deasserted at least TLCS prior to the next rising edge of CLK. Failure to meet this setup time may result in unpredictable results on the output of the convolver. Keep in mind that this requirement applies only to the case where changes are being made in the control logic during an active convolution operation. In a typical convolver configuration routine, where the configuration data is loaded prior to the actual convolution operation, this specification would not apply.

TABLE 2. ADDRESS MAPS

CONTROL LOGIC ADDRESS MAP			
A2-0			**FUNCTION**
0	0	0	Reserved for Future Use.
0	0	1	Reserved for Future Use.
0	1	0	Load Coefficient Register 0 (CREG0).
0	1	1	Load Coefficient Register 1 (CREG1).
1	0	0	Load Initialization Register (INT).
1	0	1	Select CREG0 for Internal Processing.
1	1	0	Select CREG1 for Internal Processing.
1	1	1	No Operation.

Control Signals

HOLD

The HOLD control input provides the ability to disable internal clock and stop all operations temporarily. HOLD is sampled on the rising edge of CLK and takes effect during the following clock cycle (refer to Figure 2). This signal can be used to momentarily ignore data at the input of the convolver while maintaining its current output data and operational state.

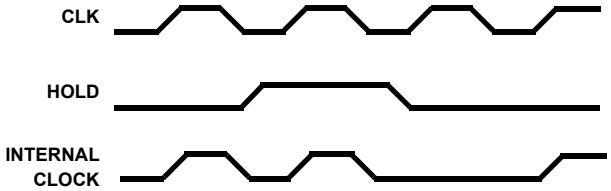


FIGURE 2. HOLD OPERATION

FRAME

The $\overline{\text{FRAME}}$ input initializes all internal flip flops and registers except for the coefficient and Initialization Registers. It is used as a reset between video frames and eliminates the need to reinitialize the entire HSP48901 or reload the coefficients. The registers and flip flops will remain in a reset state as long as $\overline{\text{FRAME}}$ is active. $\overline{\text{FRAME}}$ is an asynchronous input and may occur at any time. However, it must be deasserted at least t_{FS} ns prior to the rising clock edge that is to begin operation for the next frame in order to ensure the new pixel data is properly loaded.

Operation

A single HSP48901 can be used to perform 3 x 3 convolution on 8-bit image data. A Block Diagram of this configuration is shown in Figure 3. The inputs of an external data buffer (such as the HSP9501) are connected to the input data in parallel with the DIN1(0-7) lines; the outputs of the data buffer are connected to the DIN2(0-7) bus. A second external data buffer is connected between the outputs of the first buffer and the DIN3(0-7) inputs. To perform the convolution operation, a group of nine image pixels is multiplied by the 3 x 3 array of filter coefficients and their products are summed and sent to the output. For the example in Figure 3, the pixel value in the output image at location m, n is given by:

$$\begin{aligned} DOUT(m,n) = {} & A \times Pm\text{-}1,\ n\text{-}1 + B \times Pm\text{-}1,n + C \times Pm\text{-}1,\ n+1 \\ & + D \times Pm,\ n\text{-}1 + E \times Pm,\ n + F \times Pm,\ n+1 \\ & + G \times Pm+1,n\text{-}1 + H \times Pm+1,n + I \times Pm+1,\ n+1 \end{aligned}$$

This process is continually repeated until the last pixel of the last row of the image has been input. It can then start again with the first row of the next frame. The $\overline{\text{FRAME}}$ pin is used to clear the Internal Multiplier Registers and DOUT0-19 Registers between frames. The row length of the image to be convolved is limited only by the maximum length of the external data buffers.

The setup is straightforward. The user must first setup the HSP48901 by loading a new value into the Initialization Register. The coefficients can now be loaded one at a time from A to I via the CIN0-7 coefficient bus, and the A0-2 and $\overline{\text{LD}}$ control lines.

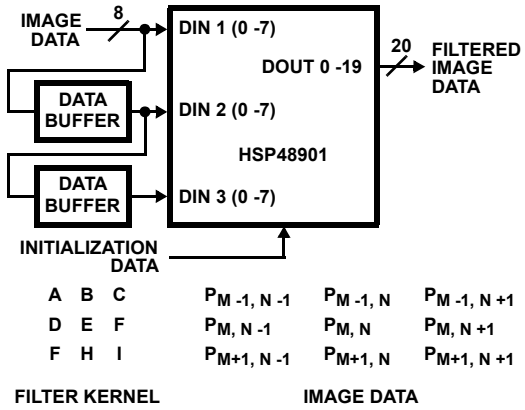


FIGURE 3. 3 x 3 KERNEL ON AN 8-BIT IMAGE

Multiple filter kernels can also be used on the same image data using the dual Coefficient Registers CREG0 and CREG1. This type of filtering is used when the characteristics of the input pixel data change over the image in such a way that no one filter produces satisfactory results for the entire image. In order to filter such an image, the characteristics of the filter itself must change while the image is being processed. The HSP48901 can perform this function with the use of an external processor. The processor is used to calculate the required new filter coefficients, loads them into the Coefficient Register not in use, and selects the newly loaded Coefficient Register at the proper time. The first Coefficient Register can then be loaded with new coefficients in preparation for the next change. This can be carried out with no interruption in processing, provided that the new register is selected synchronous to the convolver CLK signal.

The HSP48901 can also operate as a one dimensional 9-tap FIR filter by programming the Initialization Register to 1-D mode (i.e., INT bit-1 = 0). This configuration will provide for nine sequential input values to be multiplied by the coefficient values in the selected Coefficient Register and provide the proper filtered output. The input bus to be used when operating in this mode is the DIN1(0-7) inputs.

The equation for the output in the 1-D 9-tap FIR case becomes:

$$\begin{aligned} D0UTn = {} & A \times Dn\text{-}8 + B \times Dn\text{-}7 + C \times Dn\text{-}6 + D \times Dn\text{-}5 \\ & + E \times Dn\text{-}4 + F \times Dn\text{-}3 + G \times Dn\text{-}2 + H \times Dn\text{-}1 \\ & + I \times Dn \end{aligned}$$

Frame Rate

The total time to process an image is given by the formula: T = R x C/F, where:

T = Time to process a frame

R = Number of rows in the image

C = Number of pixels in a row

F = Clock rate of the HSP48901

Absolute Maximum Ratings

Supply Voltage . . . . . +6.0V
Input, Output or I/O Voltage Applied . . . . . GND -0.5V to V_{CC} +0.5V
ESD Classification . . . . . Class 1

Operating Conditions

Voltage Range . . . . . 4.75V to 5.25V
Temperature Range . . . . . 0°C to 70°C

Thermal Information

Thermal Resistance (Typical, Note 1) θ_{JA} (°C/W)
PLCC Package. 43
Maximum Junction Temperature
PLCC Package. . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(PLCC - Lead Tips Only)

Die Characteristics

Number of Transistors or Gates . . . . . 13,594 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

DC Electrical Specifications V_{CC} = 5.0V ±5%, T_A = 0°C to 70°C

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
Logical One Input Voltage	V_{IH}	V_{CC} = 5.25V	2.0	-	V
Logical Zero Input Voltage	V_{IL}	V_{CC} = 4.75V	-	0.8	V
High Level Clock Input	V_{IHC}	V_{CC} = 5.25V	3.0	-	V
Low Level Clock Input	V_{ILC}	V_{CC} = 4.75V	-	0.8	V
Output HIGH Voltage	V_{OH}	I_{OH} = 400µA, V_{CC} = 4.75V	2.6	-	V
Output LOW Voltage	V_{OL}	I_{OL} = +2.0mA, V_{CC} = 4.75V	-	0.4	V
Input Leakage Current	I_I	V_{IN} = V_{CC} or GND, V_{CC} = 5.25V	-10	10	µA
Standby Power Supply Current	I_{CCSB}	V_{IN} = V_{CC} or GND, V_{CC} = 5.25V, Outputs Open	-	500	µA
Operating Power Supply Current	I_{CCOP}	f = 20MHz, V_{IN} = V_{CC} or GND, V_{CC} = 5.25V (Note 2)	-	120	mA
Input Capacitance	C_{IN}	f = 1MHz, V_{CC} = Open, All Measurements are referenced to device GND (Note 3).	-	10	pF
Output Capacitance	C_O		-	15	pF

NOTES:

2. Power supply current is proportional to operating frequency. Typical rating for I_{CCOP} is 6mA/MHz.
3. Not tested, but characterized at initial design and at major process/design changes.

AC Electrical Specifications V_{CC} = 5.0V ±5%, T_A = 0°C to 70°C

PARAMETER	SYMBOL	NOTES	TEST CONDITIONS	-30		-40		UNITS
				MIN	MAX	MIN	MAX	
Clock Period	t_{CYCLE}			33	-	50	-	ns
Clock Pulse Width High	t_{PWH}			13	-	20	-	ns
Clock Pulse Width Low	t_{PWL}			13	-	20	-	ns
Data Input Setup Time	t_{DS}			14	-	16	-	ns
Data Input Hold Time	t_{DH}			0	-	0	-	ns
Clock to Data Out	t_{OUT}			-	21	-	30	ns
Address Setup Time	t_{AS}			5	-	5	-	ns
Address Hold Time	t_{AH}			2	-	2	-	ns

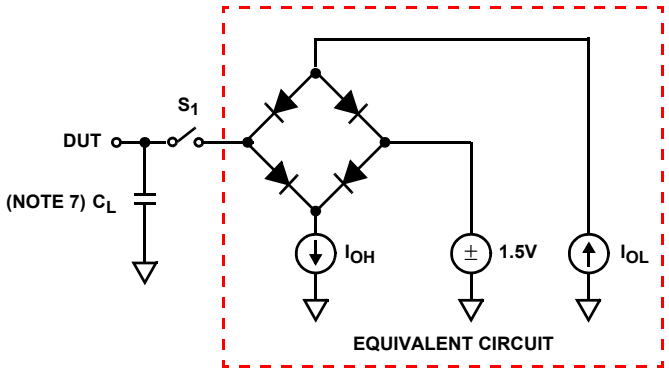
AC Electrical Specifications V_{CC} = 5.0V ±5%, T_A = 0°C to 70°C

PARAMETER	SYMBOL	NOTES	TEST CONDITIONS	-30		-40		UNITS
				MIN	MAX	MIN	MAX	
Configuration Data Setup Time	t_{CS}			10	-	12	-	ns
Configuration Data Hold Time	t_{CH}			0	-	0	-	ns
$\overline{LD}$ Pulse Width	t_{LPH}			13	-	20	-	ns
$\overline{LD}$ Setup Time	t_{LCS}	Note 4		31	t_{CYCLE}+2	40	t_{CYCLE}+2	ns
HOLD Setup Time	t_{HS}			10	-	12	-	ns
HOLD Hold Time	t_{HH}			0	-	0	-	ns
$\overline{FRAME}$ Pulse Width	t_{FPW}			t_{CYCLE}	-	t_{CYCLE}	-	ns
$\overline{FRAME}$ Setup Time	t_{FS}	Note 5		28	-	40	-	ns
Output Rise	t_R		From 0.8V to 2.0V	-	8	-	8	ns
Output Fall Time	t_F		From 2.0V to 0.8V	-	8	-	8	ns

NOTES:

4. This specification applies only to the case where a change in the active Coefficient Register is being selected during a convolution operation. It must be met in order to achieve predictable results at the next rising clock edge. In most applications, this selection will be made asynchronously, and the t_{LCS} Specification may be disregarded.
5. While $\overline{FRAME}$ is asynchronous with respect to CLK, it must be deasserted a minimum of t_{FS} ns prior to the rising clock edge which is to begin loading new pixel data for the next frame.
6. AC Testing is performed as follows: Input levels (CLK Input) = 4.0V and 0V; input levels (all other inputs) = 0V to 3.0V; input timing reference levels: (CLK) = 2.0V, (others) = 1.5V; other timing references: $V_{OH} \geq 1.5V$, $V_{OL} \leq 1.5V$; output load test load circuit with C_L = 40pF.

Test Load Circuit



NOTES:

7. Includes stray and jig capacitance.
8. Switch S_1 Open for I_{CCSB} and I_{CCOP} Tests.

Timing Waveforms

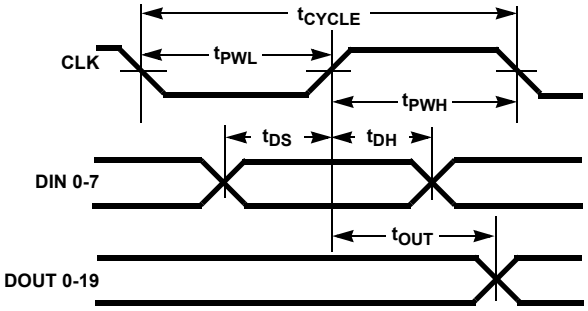


FIGURE 4. FUNCTIONAL TIMING

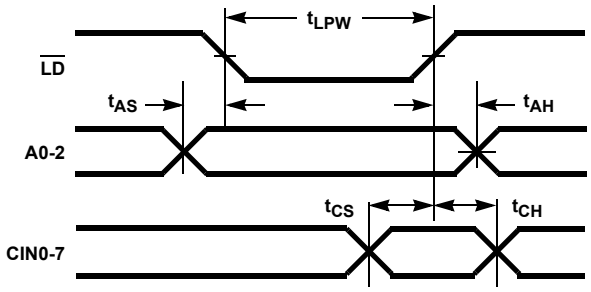


FIGURE 5. CONFIGURATION TIMING

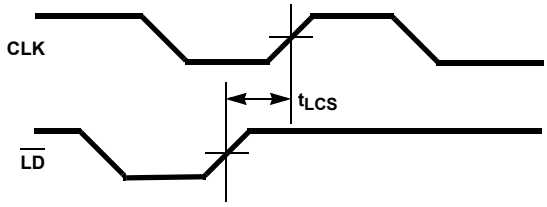


FIGURE 6. SYNCHRONOUS LOAD TIMING

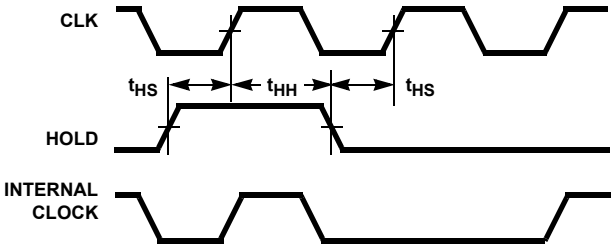


FIGURE 7. HOLD TIMING

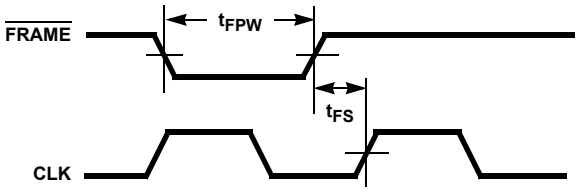


FIGURE 8. $\overline{\text{FRAME}}$ TIMING