

# ISO-CMOS MT8814 8 x 12 Analog Switch Array

Data Sheet

**Features** 

Internal control latches and address decoder

· Short set-up and hold times

Wide operating voltage: 4.5 V to 13.2 V

· 12Vpp analog signal capability

•  $R_{ON}$  65  $\Omega$  max. @  $V_{DD}$ =12 V, 25°C

•  $\Delta R_{ON} \le 10 \Omega @ V_{DD} = 12 V, 25^{\circ}C$ 

· Full CMOS switch for low distortion

· Minimum feedthrough and crosstalk

Separate analog and digital reference supplies

Low power consumption ISO-CMOS technology

# **Applications**

- Key systems
- PBX systems
- · Mobile radio
- Test equipment /instrumentation
- · Analog/digital multiplexers
- · Audio/Video switching

September 2011

#### **Ordering Information**

-40°C to +85°C

### **Description**

The Zarlink MT8814 is fabricated in Zarlink's ISO-CMOS technology providing low power dissipation and high reliability. The device contains a 8 x 12 array of crosspoint switches along with a 7 to 96 line decoder and latch circuits. Any one of the 96 switches can be addressed by selecting the appropriate seven address bits. The selected switch can be turned on or off by applying a logical one or zero to the DATA input.  $V_{SS}$  is the ground reference of the digital inputs. The range of the analog signal is from  $V_{DD}$  to  $V_{EE}$ . Chip Select (CS) allows the crosspoint array to be cascaded for matrix expansion.

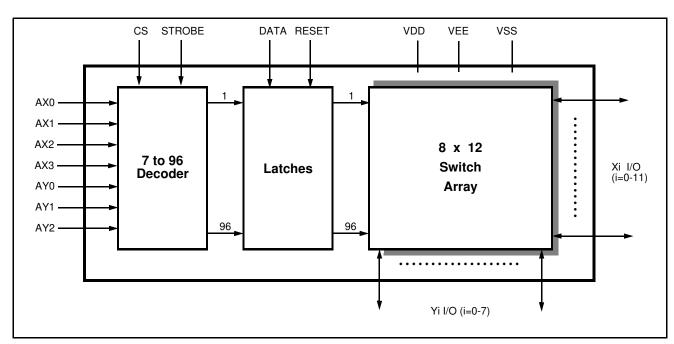


Figure 1 - Functional Block Diagram

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# **Change Summary**

Changes from the May 2005 issue to the September 2011 issue.

Page	Item	Change
1	Ordering Information	Removed leaded packages as per PCN notice.

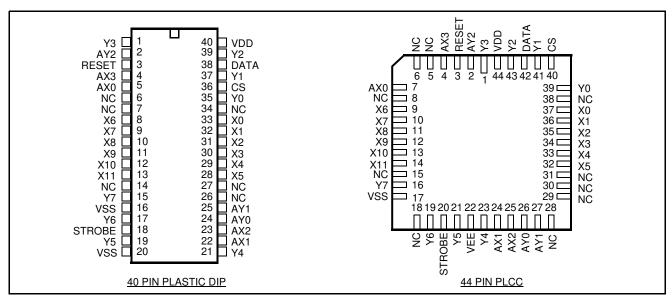


Figure 2 - Pin Connections

#### **Pin Description**

Piı	n #	Name	Description						
PDIP	PLCC	Name	Description						
1	1	Y3	Y3 Analog (Input/Output): this is connected to the Y3 column of the switch array.						
2	2	AY2	Y2 Address Line (Input).						
3	3	RESET	Master RESET (Input): this is used to turn off all switches regardless of the condition of CS. Active High.						
4,5	4,7	AX3,AX0	X3 and X0 Address Lines (Inputs).						
6,7	5,6,8	NC	No Connection.						
8-13	9-14	X6-X11	<b>X6-X11 Analog (Inputs/Outputs):</b> these are connected to the X6-X11 rows of the switch array.						
14	15,18	NC	No Connection						
15	16	Y7	Y7 Analog (Input/Output): this is connected to the Y7 column of the switch array.						
16	17	$V_{SS}$	Digital Ground Reference.						
17	19	Y6	Y6 Analog (Input/Output): this is connected to the Y6 column of the switch array.						
18	20	STROBE	STROBE (Input): enables function selected by address and data. Address must be stable before STROBE goes high and DATA must be stable on the falling edge of the STROBE. Active High.						

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#### **Pin Description**

Pir	1 #	Name	Description					
PDIP	PLCC	Name	Description					
19	21	Y5	Y5 Analog (Input/Output): this is connected to the Y5 column of the switch array.					
20	22	V <sub>EE</sub>	Negative Power Supply.					
21	23	Y4	Y4 Analog (Input/Output): this is connected to the Y4 column of the switch array.					
22, 23	24,25	AX1,AX2	X1 and X2 Address Lines (Inputs).					
24, 25	26,27	AY0,AY1	Y0 and Y1 Address Lines (Inputs).					
26, 27	28-31	NC	No Connection.					
28 - 33	32-37	X5-X0	X5-X0 Analog (Inputs/Outputs): these are connected to the X5-X0 rows of the switch array.					
34	38	NC	No Connection.					
35	39	Y0	Y0 Analog (Input/Output): this is connected to the Y0 column of the switch array.					
36	40	CS	Chip Select (Input): this is used to select the device. Active High.					
37	41	Y1	Y1 Analog (Input/Output): this is connected to the Y1 column of the switch array.					
38	42	DATA	<b>DATA (Input)</b> : a logic high input will turn on the selected switch and a logic low will turn off the selected switch. Active High.					
39	43	Y2	Y2 Analog (Input/Output): this is connected to the Y2 column of the switch array.					
40	44	$V_{DD}$	Positive Power Supply.					

## **Functional Description**

The MT8814 is an analog switch matrix with an array size of 8 x 12. The switch array is arranged such that there are 8 columns by 12 rows. The columns are referred to as the Y inputs/outputs and the rows are the X inputs/outputs. The crosspoint analog switch array will interconnect any X I/O with any Y I/O when turned on and provide a high degree of isolation when turned off. The control memory consists of a 96 bit write only RAM in which the bits are selected by the address inputs (AY0-AY2, AX0-AX3). Data is presented to the memory on the DATA input. Data is asynchronously written into memory whenever both the CS (Chip Select) and STROBE inputs are high and are latched on the falling edge of STROBE. A logical "1" written into a memory cell turns the corresponding crosspoint switch on and a logical "0" turns the crosspoint off. Only the crosspoint switches corresponding to the addressed memory location are altered when data is written into memory. The remaining switches retain their previous states. Any combination of X and Y inputs/outputs can be interconnected by establishing appropriate patterns in the control memory. A logical "1" on the RESET input will asynchronously return all memory locations to logical "0" turning off all crosspoint switches regardless of whether CS is high or low. Two voltage reference pins ( $V_{SS}$  and  $V_{EE}$ ) are provided for the MT8814 to enable switching of negative analog signals. The range for digital signals is from  $V_{DD}$  to  $V_{SS}$  while the range for analog signals is from  $V_{DD}$  to  $V_{EE}$ .  $V_{SS}$  and  $V_{EE}$  pins can be tied together if a single voltage reference is needed.

#### **Address Decode**

The seven address inputs along with the STROBE and CS (Chip Select) are logically ANDed to form an enable signal for the resettable transparent latches. The DATA input is buffered and is used as the input to all latches. To write to a location, RESET must be low and CS must go high while the address and data are set up. Then the STROBE input is set high and then low causing the data to be latched. The data can be changed while STROBE is high, however, the corresponding switch will turn on and off in accordance with the DATA input. DATA must be stable on the falling edge of STROBE in order for correct data to be written to the latch.

#### $\textbf{Absolute Maximum Ratings*} \textbf{-} \ \text{Voltages are with respect to V}_{\text{EE}} \ \text{unless otherwise stated}.$

	Parameter	Symbol	Min.	Max.	Units
1	Supply Voltage	$V_{DD}$ $V_{SS}$	-0.3 -0.3	16.0 V <sub>DD</sub> +0.3	V V
2	Analog Input Voltage	V <sub>INA</sub>	-0.3	V <sub>DD</sub> +0.3	V
3	Digital Input Voltage	V <sub>IN</sub>	V <sub>SS</sub> -0.3	V <sub>DD</sub> +0.3	V
4	Current on any I/O Pin	I		±15	mA
5	Storage Temperature	T <sub>S</sub>	-65	+150	°C
6	Package Power Dissipation PLASTIC DIP	$P_{D}$		0.6	W

<sup>\*</sup> Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

# $\textbf{Recommended Operating Conditions} \text{ - Voltages are with respect to V}_{\text{EE}} \text{ unless otherwise stated}.$

	Characteristics	Sym.	Min.	Тур.	Max.	Units	Test Conditions
1	Operating Temperature	T <sub>O</sub>	-40	25	85	°C	
2	Supply Voltage	$V_{DD}$ $V_{SS}$	4.5 V <sub>EE</sub>		13.2 V <sub>DD</sub> -4.5	V V	
3	Analog Input Voltage	$V_{INA}$	$V_{EE}$		$V_{DD}$	V	
4	Digital Input Voltage	V <sub>IN</sub>	$V_{SS}$		$V_{DD}$	V	

# **DC Electrical Characteristics**<sup>†</sup>- Voltages are with respect to $V_{EE} = V_{SS} = 0V$ , $V_{DD} = 12V$ unless otherwise stated.

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	Quiescent Supply Current	I <sub>DD</sub>		1	100	μА	All digital inputs at $V_{IN}$ = $V_{SS}$ or $V_{DD}$
				0.4	1.5	mA	All digital inputs at $V_{IN}$ =2.4V + $V_{SS}$ ; $V_{SS}$ =7.0V
				5	15	mA	All digital inputs at V <sub>IN</sub> =3.4V
2	Off-state Leakage Current (See G.9 in Appendix)	I <sub>OFF</sub>		±1	±500	nA	$IV_{Xi}$ - $V_{Yj}I = V_{DD}$ - $V_{EE}$ See Appendix, Fig. A.1
3	Input Logic "0" level	V <sub>IL</sub>			0.8+V <sub>S</sub> S	V	V <sub>SS</sub> =7.5V; V <sub>EE</sub> =0V
4	Input Logic "1" level	$V_{IH}$	2.0+V <sub>SS</sub>			V	$V_{SS}$ =6.5V; $V_{EE}$ =0V
5	Input Logic "1" level	V <sub>IH</sub>	3.3			V	
6	Input Leakage (digital pins)	I <sub>LEAK</sub>		0.1	10	μΑ	All digital inputs at $V_{IN} = V_{SS}$ or $V_{DD}$

<sup>†</sup> DC Electrical Characteristics are over recommended temperature range. ‡ Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

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#### DC Electrical Characteristics- Switch Resistance - V<sub>DC</sub> is the external DC offset applied at the analog I/O pins.

Characteristics	Sym.	25	5°C	70	)°C	85°C		Units	Test Conditions
		Тур.	Max.	Тур.	Max.	Тур.	Max.		
$ \begin{array}{lll} \text{On-state} & \text{V}_{\text{DD}}\text{=}12\text{V} \\ \text{Resistance} & \text{V}_{\text{DD}}\text{=}10\text{V} \\ \text{V}_{\text{DD}}\text{=}5\text{V} \\ \text{(See G.1, G.2, G.3 in} \\ \text{Appendix)} \end{array} $	R <sub>ON</sub>	45 55 120	65 75 185		75 85 215		80 90 225	Ω Ω Ω	$V_{SS}=V_{EE}=0V, V_{DC}=V_{DD}/2,$ $IV_{Xi}-V_{Yj}I=0.4V$ See Appendix, Fig. A.2
Difference in on-state resistance between two switches (See G.4 in Appendix)	ΔR <sub>ON</sub>	5	10		10		10	Ω	$\begin{split} &V_{DD}{=}12\text{V, }V_{SS}{=}V_{EE}{=}0,\\ &V_{DC}{=}V_{DD}/2,\\ &IV_{Xi}{-}V_{Yj}I=0.4\text{V}\\ &\text{See Appendix, Fig. A.2} \end{split}$

# AC Electrical Characteristics $^{\dagger}$ - Crosspoint Performance-Voltages are with respect to V<sub>DD</sub>=5V, V<sub>SS</sub>=0V, V<sub>EE</sub>=-7V, unless otherwise stated.

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	Switch I/O Capacitance	C <sub>S</sub>		20		рF	f=1 MHz
2	Feedthrough Capacitance	C <sub>F</sub>		0.2		pF	f=1 MHz
3	Frequency Response Channel "ON" 20LOG(V <sub>OUT</sub> /V <sub>Xi</sub> )=-3dB	F <sub>3dB</sub>		45		MHz	Switch is "ON"; $V_{INA}$ = 2Vpp sinewave; $R_L$ = 1k $\Omega$ See Appendix, Fig. A.3
4	Total Harmonic Distortion (See G.5, G.6 in Appendix)	THD		0.01		%	Switch is "ON"; $V_{INA} = 2Vpp$ sinewave f= 1kHz; $R_L$ =1k $\Omega$
5	Feedthrough Channel "OFF" Feed.=20LOG (V <sub>OUT</sub> /V <sub>Xi</sub> ) (See G.8 in Appendix)	FDT		-95		dB	All Switches "OFF"; $V_{INA}$ = 2Vpp sinewave f= 1kHz; $R_L$ = 1k $\Omega$ . See Appendix, Fig. A.4
6	Crosstalk between any two channels for switches Xi-Yi and	X <sub>talk</sub>		-45		dB	$V_{INA}$ =2Vpp sinewave f= 10MHz; R <sub>L</sub> = 75 $\Omega$ .
	Xj-Yj.			-90		dB	$V_{INA}$ =2Vpp sinewave f= 10kHz; R <sub>L</sub> = 600 $\Omega$ .
	Xtalk=20LOG ( $V_{Yj}/V_{Xi}$ ). (See G.7 in Appendix).			-85		dB	$V_{INA}$ =2Vpp sinewave f= 10kHz; R <sub>L</sub> = 1k $\Omega$ .
	(222 22 pp 22).			-80		dB	$V_{INA}$ =2Vpp sinewave f= 1kHz; R <sub>L</sub> = 10k $\Omega$ . Refer to Appendix, Fig. A.5 for test circuit.
7	Propagation delay through switch	t <sub>PS</sub>			30	ns	$R_L=1k\Omega; C_L=50pF$

<sup>†</sup> Timing is over recommended temperature range. See Fig. 3 for control and I/O timing details.
‡ Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.
Crosstalk measurements are for Plastic DIPS only, crosstalk values for PLCC packages are approximately 5dB better.

#### AC Electrical Characteristics $^{\dagger}$ - Control and I/O Timings- Voltages are with respect to $V_{DD}$ =5V, $V_{SS}$ =0V, $V_{\text{EE}}$ =-7V, unless otherwise stated.

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	Control Input crosstalk to switch (for CS, DATA, STROBE, Address)	CX <sub>talk</sub>		30		mVpp	$V_{IN}$ =3V square wave; $R_{IN}$ =1k $\Omega$ , $R_L$ =10k $\Omega$ . See Appendix, Fig. A.6
2	Digital Input Capacitance	C <sub>DI</sub>		10		pF	f=1MHz
3	Switching Frequency	F <sub>O</sub>			20	MHz	
4	Setup Time DATA to STROBE	t <sub>DS</sub>	10			ns	$R_L = 1 k\Omega$ , $C_L = 50 pF^{-1}$
5	Hold Time DATA to STROBE	t <sub>DH</sub>	10			ns	$R_L = 1 k\Omega$ , $C_L = 50 pF^{-1}$
6	Setup Time Address to STROBE	t <sub>AS</sub>	10			ns	$R_L = 1k\Omega$ , $C_L = 50pF^{-1}$
7	Hold Time Address to STROBE	t <sub>AH</sub>	10			ns	$R_L = 1k\Omega$ , $C_L = 50pF^1$
8	Setup Time CS to STROBE	t <sub>CSS</sub>	10			ns	$R_L = 1k\Omega$ , $C_L = 50pF^1$
9	Hold Time CS to STROBE	t <sub>CSH</sub>	10			ns	$R_L = 1k\Omega$ , $C_L = 50pF^{-1}$
10	STROBE Pulse Width	t <sub>SPW</sub>	20			ns	$R_L = 1k\Omega$ , $C_L = 50pF^{-1}$
11	RESET Pulse Width	t <sub>RPW</sub>	40			ns	$R_L = 1k\Omega$ , $C_L = 50pF^{-1}$
12	STROBE to Switch Status Delay	t <sub>S</sub>		40	100	ns	$R_L=1k\Omega$ , $C_L=50pF^{-1}$
13	DATA to Switch Status Delay	t <sub>D</sub>		50	100	ns	$R_L = 1 k\Omega$ , $C_L = 50 pF^{-1}$
14	RESET to Switch Status Delay	t <sub>R</sub>		35	100	ns	$R_L = 1 k\Omega$ , $C_L = 50 pF^{-1}$

<sup>†</sup> Timing is over recommended temperature range. See Fig. 3 for control and I/O timing details.

Digital Input rise time (tr) and fall time (tf) = 5ns.

‡ Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing. Note 1: Refer to Appendix, Fig. A.7 for test circuit.

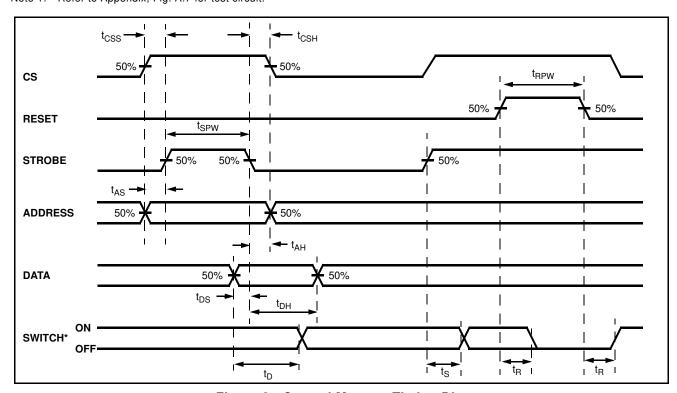


Figure 3 - Control Memory Timing Diagram

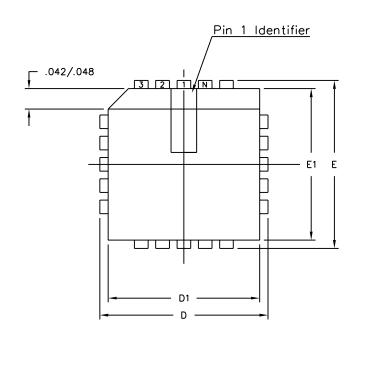
<sup>\*</sup> See Appendix, Fig. A.7 for switching waveform

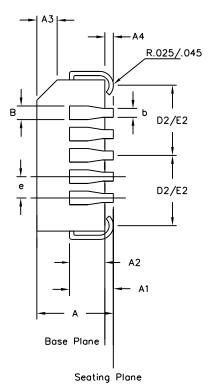
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AX0	AX1	AX2	AX3	AY0	AY1	AY2	Connection
0	0	0	0	0	0	0	X0-Y0
1	0	0	0	0	0	0	X1-Y0
0	1	0	0	0	0	0	X2-Y0
1	1	0	0	0	0	0	X3-Y0
0	0	1	0	0	0	0	X4-Y0
1	0	1	0	0	0	0	X5-Y0
0	1	1	0	0	0	0	No Connection <sup>1</sup>
1	1	1	0	0	0	0	No Connection <sup>1</sup>
0	0	0	1	0	0	0	X6-Y0
1	0	0	1	0	0	0	X7-Y0
0	1	0	1	0	0	0	X8-Y0
1	1	0	1	0	0	0	X9-Y0
0	0	1	1	0	0	0	X10-Y0
1	0	1	1	0	0	0	X11-Y0
0	1	1	1	0	0	0	No Connection <sup>1</sup>
1	1	1	1	0	0	0	No Connection <sup>1</sup>
Q	Q	Q	Q	1	Q	Q	X0-Y1
$\downarrow$	<b>\</b>	↓	↓	<b>↓</b>	<b>\</b>	<b>↓</b>	$\downarrow \downarrow$
1	0	1	1	1	0	0	X11-Y1
Q	0	Q	Q	Q	1	Q	X0-Y2
<b>\</b>	<b>↓</b>	<b>↓</b>	<b>↓</b>	<b>\</b>	<b>↓</b>	<b>\</b>	$\downarrow \downarrow$
1	0	1	1	0	1	0	X11-Y2
Q	0	Q	Q	1	1	0	X0-Y3
<b>*</b>		<b>*</b>	<b>*</b>	<b>V</b>	<b>*</b>	i i	$\downarrow \downarrow$
1	0	1	1	1	1	0	X11-Y3
Q	Q	Q	Q	Q	Q	1	X0-Y4
<b>↓</b>	↓	<b>\</b>	<b>↓</b>	<b>↓</b>	<b>↓</b>	<b>\</b>	$\downarrow \downarrow$
1	0	1	1	0	0	1	X11-Y4
Q	Q	Q	Q	1	Q	1	X0-Y5
<b>\</b>	<b>+</b>	<b>\</b>	<b>↓</b>	<b>\</b>	<b>\</b>	<b>\</b>	$\downarrow \downarrow$
1	0	1	1	1	0	1	X11-Y5
Q	Q	Q	Q	Q	1	1 1	X0-Y6
<b>¥</b>	*	<b>*</b>	*	<b>*</b>	<b>*</b>	*	$\downarrow \downarrow$
1	0	1	1	0	1	1	X11-Y6
Q	Q	Q	Q	1	1 1	1 1	X0-Y7
<b>\</b>	<b>*</b>	<b>*</b>	<b>*</b>	<b>.</b>	<b>*</b>	<b>*</b>	<b>↓</b> ↓
1	0	1	1	1	11	1	X11-Y7

Table 1 - Address Decode Truth Table

Note 1: This address has no effect on device status.



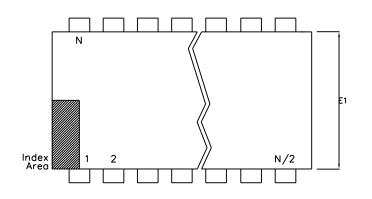


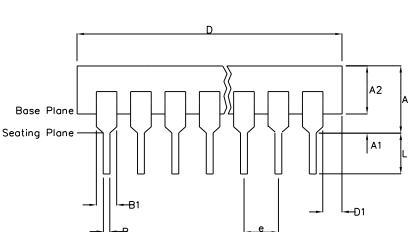
	Control Di	imensions	Altern. Di	mensions			
Symbol	in inc	hes	in milli	metres			
	MIN	MAX	MIN	MAX			
Α	0.165	0.180	4.19	4.57			
A1	0.090	0.120	2.29	3.05			
Α2	0.062	0.083	1.57	2.11			
А3	0.042	0.056	1.07	1.42			
Α4	0.020	_	0.51	_			
D	0.685	0.695	17.40	17.65			
D1	0.650	0.656	16.51	16.66			
D2	0.291	0.319	7.39	8.10			
Ε	0.685	0.695	17.40	17.65			
E1	0.650	0.656	16.51	16.66			
E2	0.291	0.319	7.39	8.10			
В	0.026	0.032	0.66	0.81			
b	0.013	0.021	0.33	0.53			
е	0.050	BSC	1.27	BSC			
		Pin fee	atures				
ND		11					
NE	11						
Ν	44						
Note	Note Square						
Confor	ms to J	EDEC MS	-018AC	Iss. A			

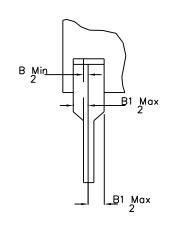
#### Notes:

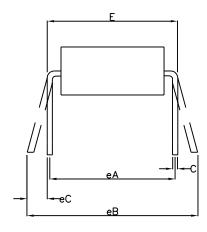
- 1. All dimensions and tolerances conform to ANSI Y14.5M-1982
- 2. Dimensions D1 and E1 do not include mould protrusions. Allowable mould protrusion is 0.010" per side. Dimensions D1 and E1 include mould protrusion mismatch and are determined at the parting line, that is D1 and E1 are measured at the extreme material condition at the upper or lower parting line.
- 3. Controlling dimensions in Inches.
- 4. "N" is the number of terminals.
- 5. Not To Scale
- 6. Dimension R required for 120° minimum bend.

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ISSUE	1	2	3		Previous package codes	Package Outline for
ACN	5958	207470	213094	ZARLINK SEMICONDUCTOR	HP / P	44 lead PLCC
DATE	15Aug94	10Sep99	15Jul02	Jamies Nyselisk	,	
APPRD.						GPD00003









	Min	Max	Min	Max
	mm	mm	<u>Inches</u>	<u>Inches</u>
Α		6.35		0.250
A1	0.38		0.015	
A2	3.18	4.95	0.125	0.195
В	0.36	0.56	0.014	0.022
B1	0.76	1.78	0.030	0.070
C	0.20	0.38	0.008	0.015
D	50.29	53.21	1.980	2.095
D1	0.13		0.005	
E	15.24	15.88	0.600	0.625
E1	12.32	14.73	0.485	0.580
е	2.54 BSC		0.100 BSC	
eА	15.24 BSC		0.600 BSC	
eВ		17.78		0.700
١	2.92	5.08	0.115	0.200
Ν	40		40	
Conforms to Jedec MS-011AC ISS.B				

#### Notes:

1. Controlling Dimensions are in inches
2. Dimension A, A1 and L are measured with the package seated in the Seating Plane
3. Dimensions D & E1 do not include mould flash or protrusions. Mould flash or protrusion shall not exceed 0.010 inch.
4. Dimensions E & eA are measured with leads constrained to be perpendicular to plane T.
5. Dimensions eB & eC are measured at the lead tips with the leads unconstrained; eC must be zero or greater.

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ISSUE	1	2	3			
ACN	7010	203533	213103			
DATE	20Apr95	25Nov97	15Jul02			
APPRD.						



	Package Code DA	
Previous package codes	Daalaaa Oodiaa faa	
DP / E	Package Outline for 40 lead PDIP	
	GPD00073	



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