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FAIRCHILD SEMICONDUCTOR®

October 2013

# FDME410NZT

## N-Channel PowerTrench® MOSFET

**20 V, 7 A, 26 mΩ**

### Features

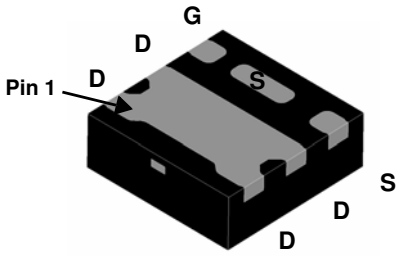
- Max $r_{DS(on)}$ = 26 mΩ at $V_{GS}$ = 4.5 V, $I_D$ = 7 A
- Max $r_{DS(on)}$ = 31 mΩ at $V_{GS}$ = 2.5 V, $I_D$ = 6 A
- Max $r_{DS(on)}$ = 39 mΩ at $V_{GS}$ = 1.8 V, $I_D$ = 5 A
- Max $r_{DS(on)}$ = 53 mΩ at $V_{GS}$ = 1.5 V, $I_D$ = 4 A
- Low profile: 0.55 mm maximum in the new package MicroFET 1.6x1.6 **Thin**
- Free from halogenated compounds and antimony oxides
- HBM ESD protection level > 1800V (Note3)
- RoHS Compliant

### General Description

This Single N-Channel MOSFET has been designed using Fairchild Semiconductor's advanced Power Trench process to optimize the $r_{DS(ON)}$ @ VGS = 1.5 V on special MicroFET leadframe.

### Applications

- Li-Ion Battery Pack
- Baseband Switch
- Load Switch
- DC-DC Conversion

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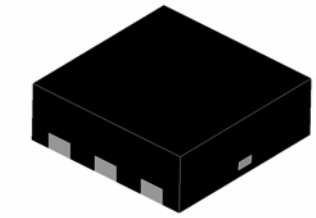

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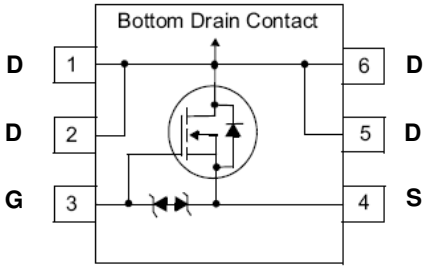



**MicroFET 1.6x1.6 Thin**

## MOSFET Maximum Ratings $T_A$ = 25 °C unless otherwise noted

| Symbol | Parameter | | | Ratings | Units |
|---|---|---|---|---|---|
| $V_{DS}$ | Drain to Source Voltage | | | 20 | V |
| $V_{GS}$ | Gate to Source Voltage | | | ±8 | V |
| $I_D$ | Drain Current -Continuous | $T_A$ = 25 °C | (Note 1a) | 7 | A |
| | -Pulsed | | | 15 | |
| $P_D$ | Power Dissipation for Single Operation | $T_A$ = 25 °C | (Note 1a) | 2.1 | W |
| | Power Dissipation for Single Operation | $T_A$ = 25 °C | (Note 1b) | 0.7 | |
| $T_J$, $T_{STG}$ | Operating and Storage Junction Temperature Range | | | -55 to +150 | °C |

### Thermal Characteristics

| | | | | |
|---|---|---|---|---|
| $R_{\theta JA}$ | Thermal Resistance, Junction to Ambient | (Note 1a) | 60 | °C/W |
| $R_{\theta JA}$ | Thermal Resistance, Junction to Ambient | (Note 1b) | 175 | |

### Package Marking and Ordering Information

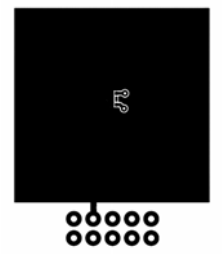
| Device Marking | Device | Package | Reel Size | Tape Width | Quantity |
|---|---|---|---|---|---|
| 6T | FDME410NZT | MicroFET 1.6x1.6 **Thin** | 7 ” | 8 mm | 5000 units |

## Electrical Characteristics $T_J$ = 25 °C unless otherwise noted

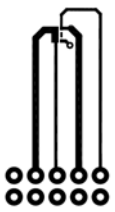
| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Off Characteristics** | | | | | | |
| $BV_{DSS}$ | Drain to Source Breakdown Voltage | $I_D$ = 250 μA, $V_{GS}$ = 0 V | 20 | | | V |
| $\frac{\Delta BV_{DSS}}{\Delta T_J}$ | Breakdown Voltage Temperature Coefficient | $I_D$ = 250 μA, referenced to 25 °C | | 18 | | mV/°C |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = 16 V, $V_{GS}$ = 0 V | | | 1 | μA |
| $I_{GSS}$ | Gate to Source Leakage Current | $V_{GS}$ = ±8 V, $V_{DS}$ = 0 V | | | ±10 | μA |
| **On Characteristics** | | | | | | |
| $V_{GS(th)}$ | Gate to Source Threshold Voltage | $V_{GS}$ = $V_{DS}$, $I_D$ = 250 μA | 0.4 | 0.7 | 1.0 | V |
| $\frac{\Delta V_{GS(th)}}{\Delta T_J}$ | Gate to Source Threshold Voltage Temperature Coefficient | $I_D$ = 250 μA, referenced to 25 °C | | -3 | | mV/°C |
| $r_{DS(on)}$ | Drain to Source On Resistance | $V_{GS}$ = 4.5 V, $I_D$ = 7 A | | 19 | 26 | mΩ |
| | | $V_{GS}$ = 2.5 V, $I_D$ = 6 A | | 20 | 31 | |
| | | $V_{GS}$ = 1.8 V, $I_D$ = 5 A | | 24 | 39 | |
| | | $V_{GS}$ = 1.5 V, $I_D$ = 4 A | | 31 | 53 | |
| | | $V_{GS}$ = 4.5 V, $I_D$ = 7 A , $T_J$ = 125 °C | | 24 | 36 | |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$ = 5 V, $I_D$ = 7 A | | 35 | | S |
| **Dynamic Characteristics** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{DS}$ = 10 V, $V_{GS}$ = 0 V, f = 1 MHz | | 770 | 1025 | pF |
| $C_{oss}$ | Output Capacitance | | | 115 | 155 | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | | 75 | 115 | pF |
| $R_g$ | Gate Resistance | | | 1.9 | | Ω |
| **Switching Characteristics** | | | | | | |
| $t_{d(on)}$ | Turn-On Delay Time | $V_{DD}$ = 10 V, $I_D$ = 7 A, $V_{GS}$ = 4.5 V, $R_{GEN}$ = 6 Ω | | 7.3 | 15 | ns |
| $t_r$ | Rise Time | | | 3.4 | 10 | ns |
| $t_{d(off)}$ | Turn-Off Delay Time | | | 27 | 43 | ns |
| $t_f$ | Fall Time | | | 3.2 | 10 | ns |
| $Q_g$ | Total Gate Charge | $V_{DD}$ = 10 V, $I_D$ = 7 A, $V_{GS}$ = 4.5 V | | 9.2 | 13 | nC |
| $Q_{gs}$ | Gate to Source Gate Charge | | | 1.1 | | nC |
| $Q_{gd}$ | Gate to Drain “Miller” Charge | | | 1.6 | | nC |
| **Drain-Source Diode Characteristics** | | | | | | |
| $V_{SD}$ | Source to Drain Diode Forward Voltage | $V_{GS}$ = 0 V, $I_S$ = 1.6 A (Note 2) | | 0.7 | 1.2 | V |
| $t_{rr}$ | Reverse Recovery Time | $I_F$ = 7 A, di/dt = 100 A/μs | | 15 | 27 | ns |
| $Q_{rr}$ | Reverse Recovery Charge | | | 3.5 | 10 | nC |

**Notes:**

1. $R_{\theta JA}$ is determined with the device mounted on a 1 $in^2$ pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 60 °C/W when mounted on a 1 $in^2$ pad of 2 oz copper.



b. 175 °C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300μs, Duty cycle < 2.0%.

3. The diode connected between the gate and source serves only as protection ESD. No gate overvoltage rating is implied.

## Typical Characteristics $T_J$ = 25 °C unless otherwise noted

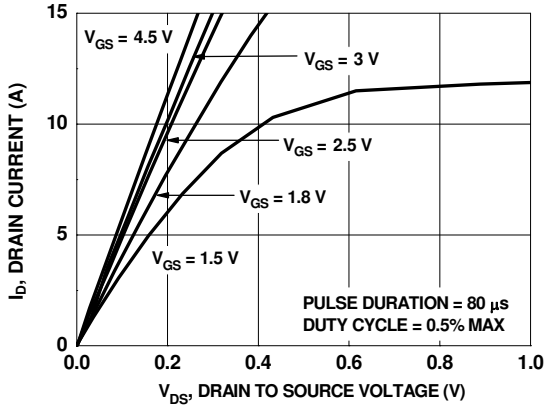



**Figure 1. On-Region Characteristics**

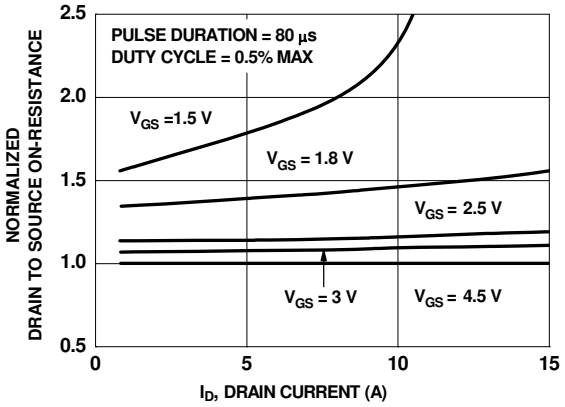



**Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage**

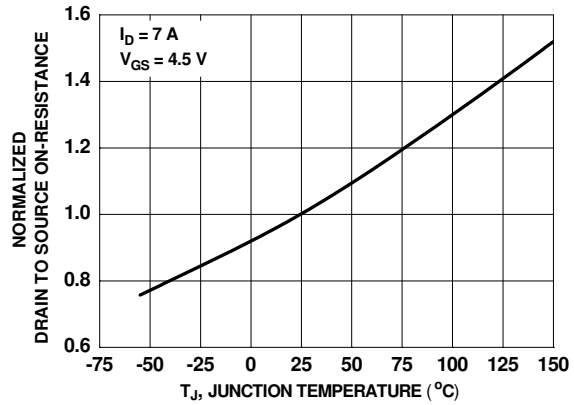



**Figure 3. Normalized On- Resistance vs Junction Temperature**

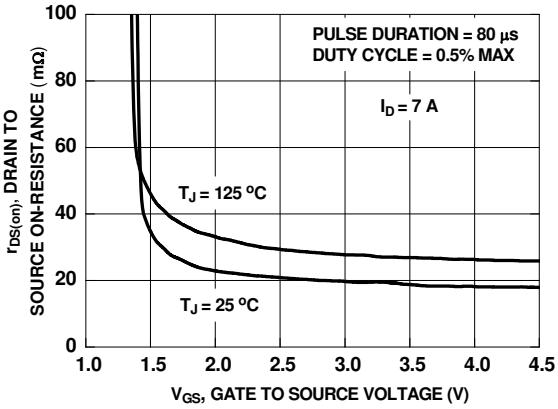



**Figure 4. On-Resistance vs Gate to Source Voltage**

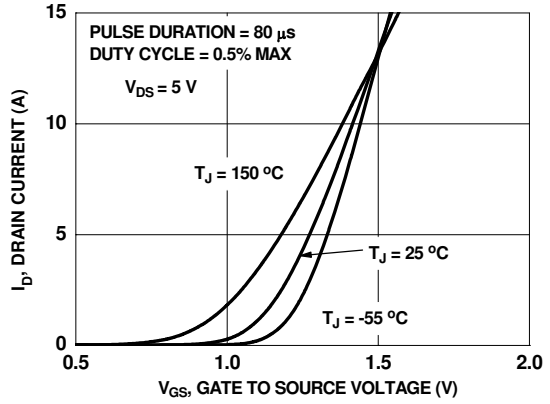



**Figure 5. Transfer Characteristics**

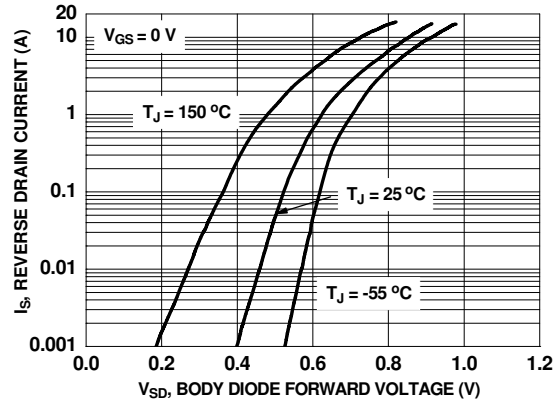



**Figure 6. Source to Drain Diode Forward Voltage vs Source Current**

## Typical Characteristics $T_J$ = 25 °C unless otherwise noted

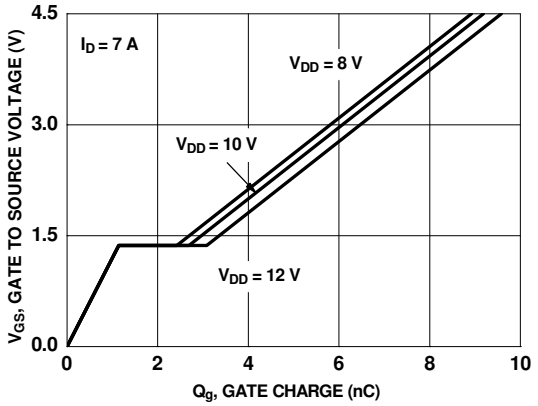



**Figure 7. Gate Charge Characteristics**

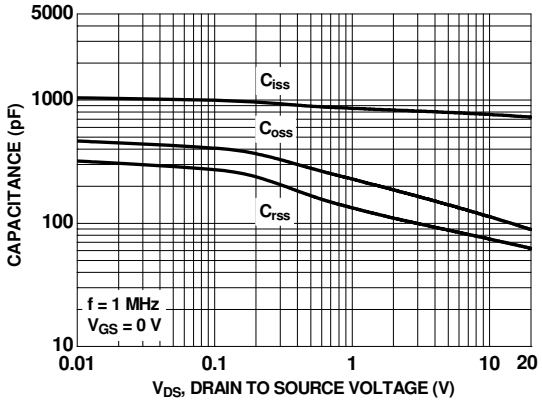



**Figure 8. Capacitance vs Drain to Source Voltage**

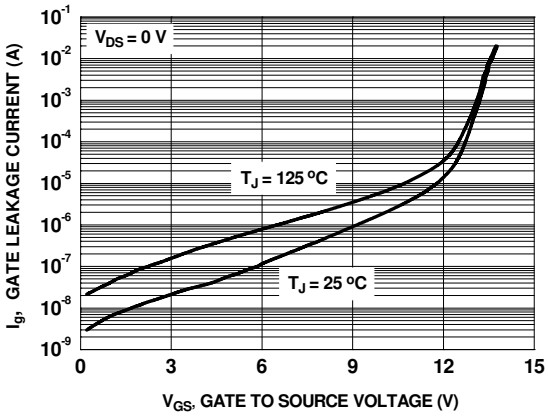



**Figure 9. Gate Leakage Current vs Gate to Source Voltage**

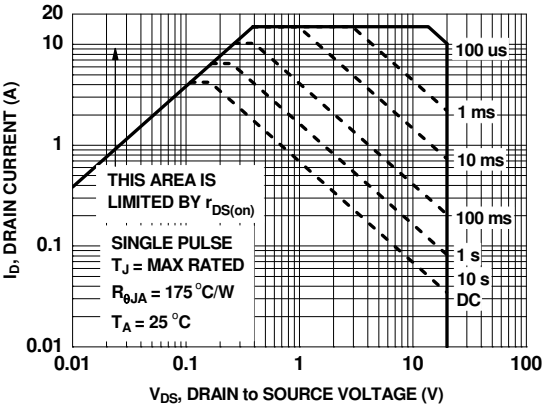



**Figure 10. Forward Bias Safe Operating Area**

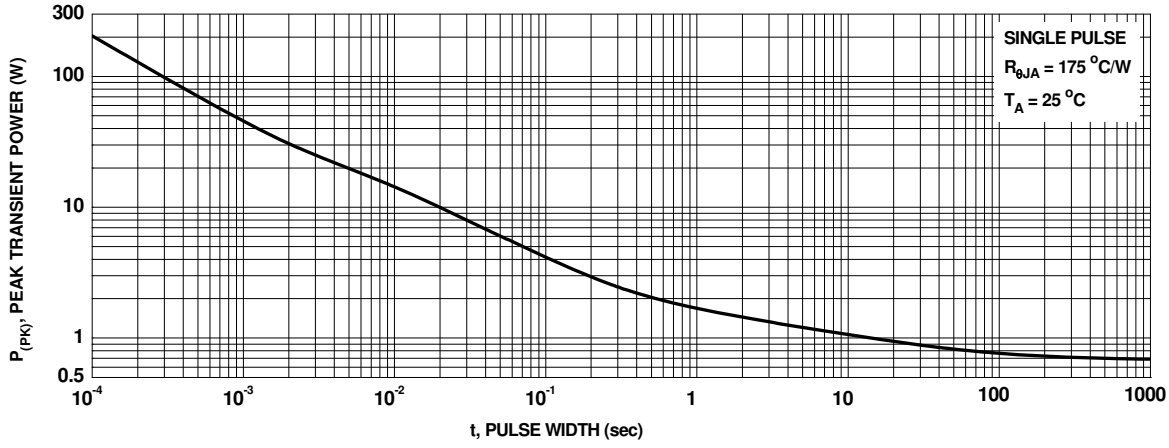



**Figure 11. Single Pulse Maximum Power Dissipation**

## Typical Characteristics $T_J$ = 25 °C unless otherwise noted

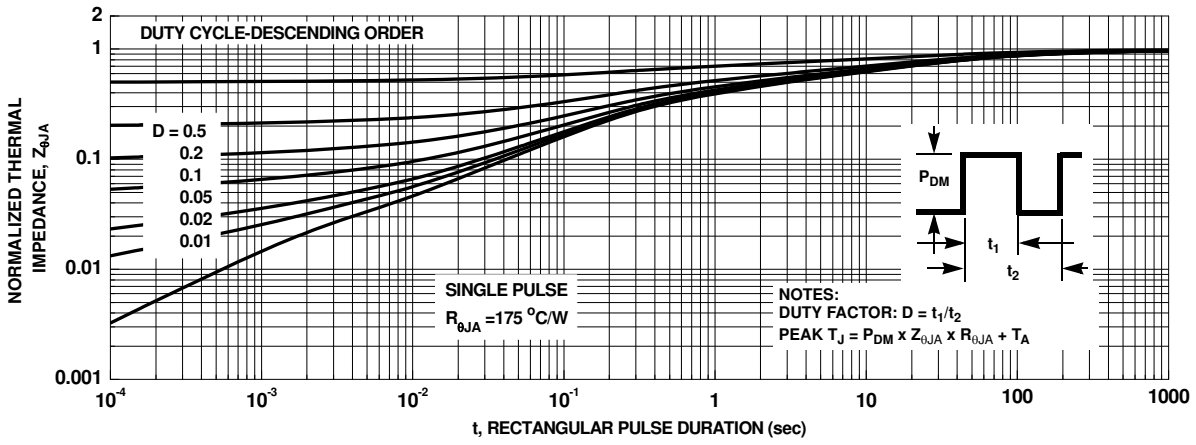
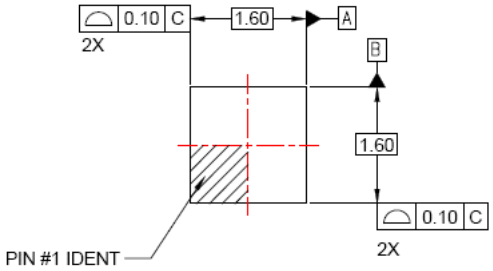
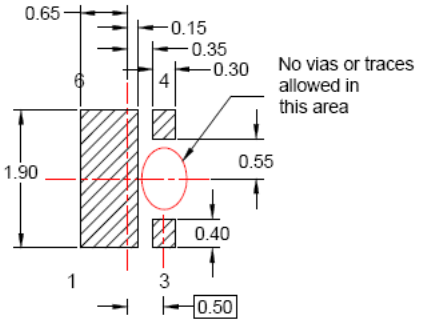



**Figure 12. Junction-to-Ambient Transient Thermal Response Curve**

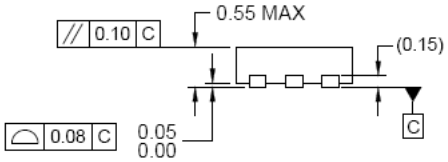
## Dimensional Outline and Pad Layout



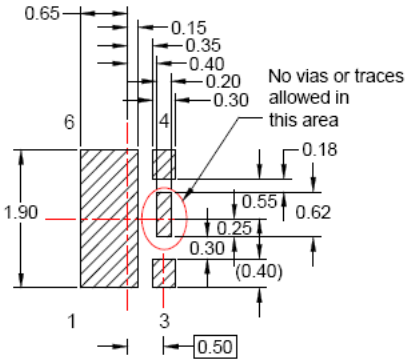

TOP VIEW



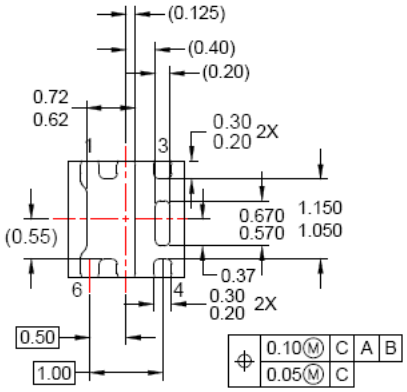

RECOMMENDED LAND PATTERN OPT 1




SIDE VIEW




RECOMMENDED LAND PATTERN OPT 2

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Rev. I66

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