

## 100336 Low Power 4-Stage Counter/Shift Register

### General Description

The 100336 operates as either a modulo-16 up/down counter or as a 4-bit bidirectional shift register. Three Select ( $S_n$ ) inputs determine the mode of operation, as shown in the Function Select table. Two Count Enable ( $\overline{CEP}$ ,  $\overline{CET}$ ) inputs are provided for ease of cascading in multistage counters. One Count Enable ( $\overline{CET}$ ) input also doubles as a Serial Data ( $D_0$ ) input for shift-up operation. For shift-down operation,  $D_3$  is the Serial Data input. In counting operations the Terminal Count ( $\overline{TC}$ ) output goes LOW when the counter reaches 15 in the count/up mode or 0 (zero) in the count/down mode. In the shift modes, the  $\overline{TC}$  output repeats the  $Q_3$  output. The dual nature of this  $\overline{TC}/Q_3$  output and the  $D_0/\overline{CET}$  input means that one interconnection from one stage to the next higher stage serves as the link for multistage counting or shift-up operation. The individual Preset ( $P_n$ ) inputs are used

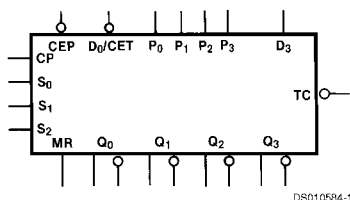
to enter data in parallel or to preset the counter in programmable counter applications. A HIGH signal on the Master Reset ( $\overline{MR}$ ) input overrides all other inputs and asynchronously clears the flip-flops. In addition, a synchronous clear is provided, as well as a complement function which synchronously inverts the contents of the flip-flops. All inputs have 50 k $\Omega$  pull-down resistors.

### Features

- 40% power reduction of the 100136
- 2000V ESD protection
- Pin/function compatible with 100136
- Voltage compensated operating range = -4.2V to -5.7V
- Available to industrial grade temperature range
- Available to MIL-STD-883

### Ordering Code:

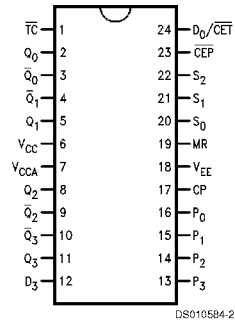
### Logic Symbol



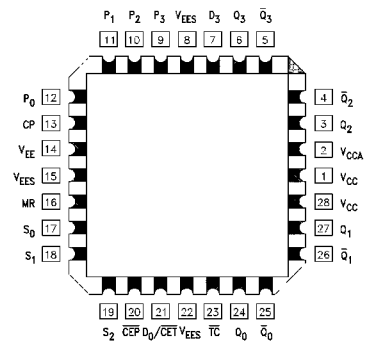
Pin Names	Description
CP	Clock Pulse Input
$\overline{CEP}$	Count Enable Parallel Input (Active LOW)
$D_0/\overline{CET}$	Serial Data Input/Count Enable Trickle Input (Active LOW)
$S_0$ - $S_2$	Select Inputs
MR	Master Reset Input
$P_0$ - $P_3$	Preset Inputs
$D_3$	Serial Data Input
$\overline{TC}$	Terminal Count Output
$Q_0$ - $Q_3$	Data Outputs
$\overline{Q_0}$ - $\overline{Q_3}$	Complementary Data Outputs

## Connection Diagrams

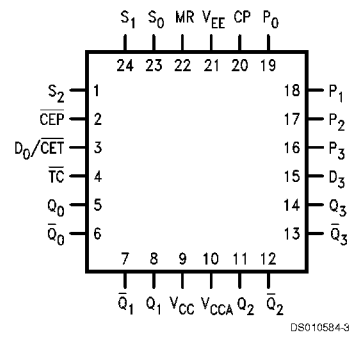
24-Pin DIP/SOIC



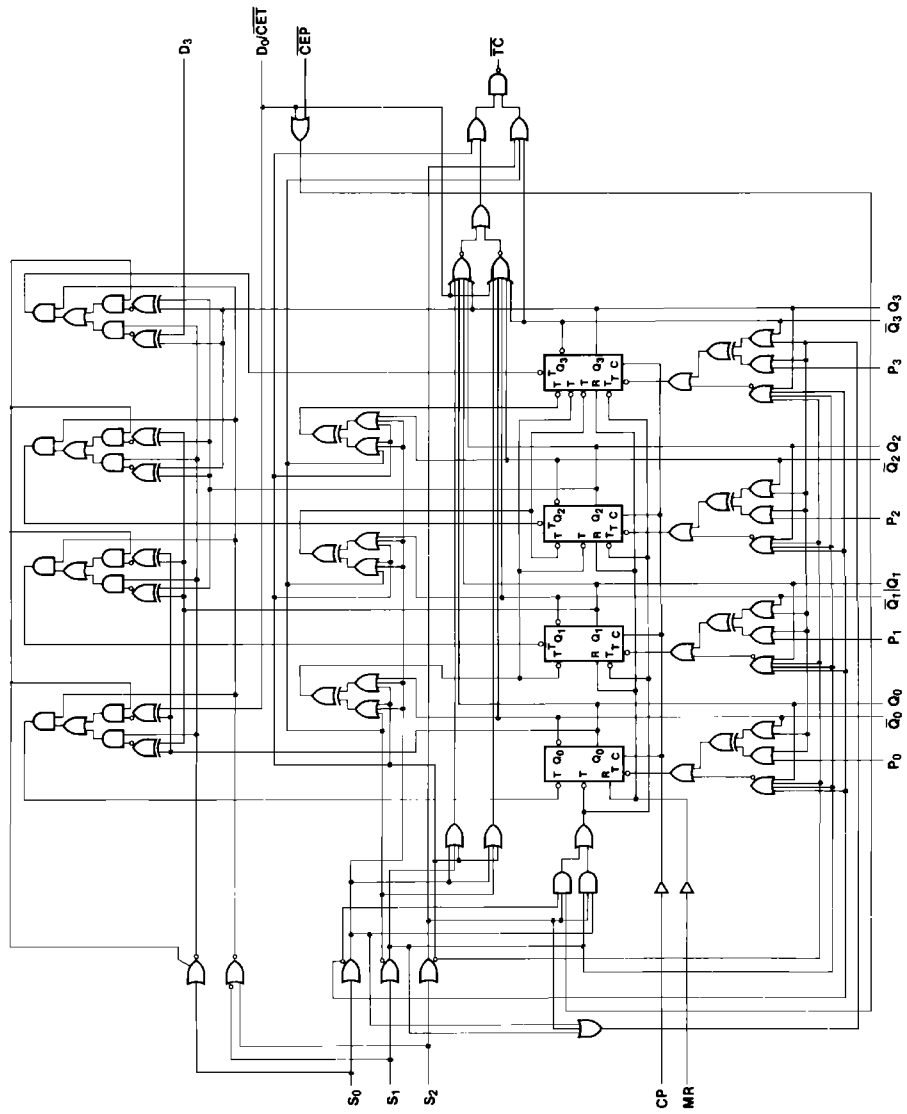
28-Pin PCC



24-Pin Quad Cerpak



# Logic Diagram



DS010584-5

## Function Select Table

S <sub>2</sub>	S <sub>1</sub>	S <sub>0</sub>	Function
L	L	L	Parallel Load
L	L	H	Complement
L	H	L	Shift Left
L	H	H	Shift Right
H	L	L	Count Down
H	L	H	Clear
H	H	L	Count Up
H	H	H	Hold

## Truth Table

Q<sub>0</sub> = LSB

Inputs								Outputs				TC	Mode
MR	S <sub>2</sub>	S <sub>1</sub>	S <sub>0</sub>	CEP	D <sub>0</sub> /CET	D <sub>3</sub>	CP	Q <sub>3</sub>	Q <sub>2</sub>	Q <sub>1</sub>	Q <sub>0</sub>		
L	L	L	L	X	X	X	↗	P <sub>3</sub>	P <sub>2</sub>	P <sub>1</sub>	P <sub>0</sub>	L	Preset (Parallel Load)
L	L	L	H	X	X	X	↗	$\overline{Q}_3$	$\overline{Q}_2$	$\overline{Q}_1$	$\overline{Q}_0$	L	Invert
L	L	H	L	X	X	X	↗	D <sub>3</sub>	Q <sub>3</sub>	Q <sub>2</sub>	Q <sub>1</sub>	D <sub>3</sub>	Shift to LSB
L	L	H	H	X	X	X	↗	Q <sub>2</sub>	Q <sub>1</sub>	Q <sub>0</sub>	D <sub>0</sub>	Q <sub>3</sub> (Note 1)	Shift to MSB
L	H	L	L	L	L	X	↗	(Q <sub>0-3</sub> ) minus 1				1	Count Down
L	H	L	L	H	L	X	X	Q <sub>3</sub>	Q <sub>2</sub>	Q <sub>1</sub>	Q <sub>0</sub>	1	Count Down with CEP not active
L	H	L	L	X	H	X	X	Q <sub>3</sub>	Q <sub>2</sub>	Q <sub>1</sub>	Q <sub>0</sub>	H	Count Down with CET not active
L	H	L	H	X	X	X	↗	L	L	L	L	H	Clear
L	H	H	L	L	L	X	↗	(Q <sub>0-3</sub> ) plus 1				2	Count Up
L	H	H	L	H	L	X	X	Q <sub>3</sub>	Q <sub>2</sub>	Q <sub>1</sub>	Q <sub>0</sub>	2	Count Up with CEP not active
L	H	H	L	X	H	X	X	Q <sub>3</sub>	Q <sub>2</sub>	Q <sub>1</sub>	Q <sub>0</sub>	H	Count Up with CET not active
L	H	H	H	X	X	X	X	Q <sub>3</sub>	Q <sub>2</sub>	Q <sub>1</sub>	Q <sub>0</sub>	H	Hold
H	L	L	L	X	X	X	X	L	L	L	L	L	Asynchronous Master Reset
H	L	L	H	X	X	X	X	L	L	L	L	L	
H	L	H	L	X	X	X	X	L	L	L	L	L	
H	L	H	H	X	X	X	X	L	L	L	L	L	
H	H	L	L	X	L	X	X	L	L	L	L	L	
H	H	L	H	X	X	X	X	L	L	L	L	L	
H	H	H	L	X	X	X	X	L	L	L	L	L	
H	H	H	H	X	X	X	X	L	L	L	L	L	
H	H	H	H	X	X	X	X	L	L	L	L	L	
H	H	H	H	X	X	X	X	L	L	L	L	L	

1 = L if Q<sub>0</sub>-Q<sub>3</sub> = LLLL

H if Q<sub>0</sub>-Q<sub>3</sub> ≠ LLLL

2 = L if Q<sub>0</sub>-Q<sub>3</sub> = HHHH

H if Q<sub>0</sub>-Q<sub>3</sub> ≠ HHHH

H = HIGH Voltage Level

L = LOW Voltage Level

X = Don't Care

↗ = LOW-to-HIGH Transition

**Note 1:** Before the clock, TC is Q<sub>3</sub>

After the clock, TC is Q<sub>2</sub>

## Absolute Maximum Ratings (Note 2)

Storage Temperature ( $T_{STG}$ )	-65°C to +150°C
Maximum Junction Temperature ( $T_J$ )	
Ceramic	+175°C
Plastic	+150°C
$V_{EE}$ Pin Potential to Ground Pin	-7.0V to +0.5V
Input Voltage (DC)	$V_{EE}$ to +0.5V
Output Current (DC Output HIGH)	-50 mA
ESD (Note 3)	$\geq 2000V$

## Recommended Operating Conditions

Case Temperature ( $T_C$ )	
Commercial	0°C to +85°C
Industrial	-40°C to +85°C
Military	-55°C to +125°C
Supply Voltage ( $V_{EE}$ )	-5.7V to -4.2V

**Note 2:** Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 3:** ESD testing conforms to MIL-STD-883, Method 3015.

## Commercial Version DC Electrical Characteristics

$V_{EE} = -4.2V$  to  $-5.7V$ ,  $V_{CC} = V_{CCA} = GND$ ,  $T_C = 0^\circ C$  to  $+85^\circ C$  (Note 4)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
$V_{OH}$	Output HIGH Voltage	-1025	-955	-870	mV	$V_{IN} = V_{IH (Max)}$ or $V_{IL (Min)}$
$V_{OL}$	Output LOW Voltage	-1830	-1705	-1620	mV	
$V_{OHC}$	Output HIGH Voltage	-1035			mV	$V_{IN} = V_{IH (Min)}$ or $V_{IL (Max)}$
$V_{OLC}$	Output LOW Voltage			-1610	mV	
$V_{IH}$	Input HIGH Voltage	-1165		-870	mV	Guaranteed HIGH Signal for All Inputs
$V_{IL}$	Input LOW Voltage	-1830		-1475	mV	Guaranteed LOW Signal for All Inputs
$I_{IL}$	Input LOW Current	0.50			$\mu A$	$V_{IN} = V_{IL (Min)}$
$I_{IH}$	Input HIGH Current			240	$\mu A$	$V_{IN} = V_{IH (Max)}$
$I_{EE}$	Power Supply Current	-165		-80		Inputs Open

**Note 4:** The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

## Commercial Version DIP AC Characteristics

$V_{EE} = -4.2V$  to  $-5.7V$ ,  $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_C = 0^\circ C$		$T_C = +25^\circ C$		$T_C = +85^\circ C$		Units	Conditions
		Min	Max	Min	Max	Min	Max		
$f_{shift}$	Shift Frequency	300		300		300		MHz	Figures 2, 3
$t_{PLH}$ $t_{PHL}$	Propagation Delay CP to $Q_n$ , $\overline{Q}_n$	1.00	2.00	1.00	2.00	1.00	2.00	ns	Figures 1, 3 (Note 5)
$t_{PLH}$ $t_{PHL}$	Propagation Delay CP to $\overline{TC}$ (Shift)	2.10	3.50	2.10	3.50	2.10	3.70	ns	Figures 1, 7, 8 (Note 5)
$t_{PLH}$ $t_{PHL}$	Propagation Delay CP to $\overline{TC}$ (Count)	2.40	4.40	2.40	4.40	2.60	4.70	ns	Figures 1, 9 (Note 5)
$t_{PLH}$ $t_{PHL}$	Propagation Delay MR to $Q_n$ , $\overline{Q}_n$	1.40	2.50	1.40	2.50	1.50	2.60	ns	Figures 1, 4 (Note 5)
$t_{PLH}$ $t_{PHL}$	Propagation Delay MR to $\overline{TC}$ (Count)	2.80	5.10	2.90	5.20	3.10	5.50	ns	Figures 1, 12 (Note 5)
$t_{PHL}$	Propagation Delay MR to $\overline{TC}$ (Shift)	2.40	4.00	2.40	4.00	2.50	4.10	ns	Figures 1, 10, 11 (Note 5)
$t_{PLH}$ $t_{PHL}$	Propagation Delay $D_0/\overline{CET}$ to $\overline{TC}$	1.80	3.10	1.80	3.10	1.90	3.30	ns	Figures 1, 5 (Note 5)
$t_{PLH}$ $t_{PHL}$	Propagation Delay $S_n$ to $\overline{TC}$	1.90	4.10	1.90	4.10	2.10	4.40	ns	
$t_{TLH}$ $t_{THL}$	Transition Time 20% to 80%, 80% to 20%	0.35	1.20	0.35	1.20	0.35	1.20	ns	Figures 1, 3
$t_s$	Setup Time $D_3$ $P_n$ $D_0/\overline{CET}$ $\overline{CEP}$ $S_n$ MR (Release Time)	1.00 1.50 1.30 1.40 3.40 2.60		1.00 1.50 1.30 1.40 3.40 2.60		1.00 1.50 1.30 1.40 3.40 2.60		ns	Figures 6, 4
$t_H$	Hold Time $D_3$ $P_n$ $D_0/\overline{CET}$ $\overline{CEP}$ $S_n$	0.40 0.30 0.30 0.20 0.10		0.40 0.30 0.30 0.20 0.10		0.40 0.30 0.30 0.20 0.10		ns	Figure 6
$t_{pw(H)}$	Pulse Width HIGH CP, MR	2.00		2.00		2.00		ns	Figures 3, 4

**Note 5:** The propagation delay specified is for single output switching. Delays may vary up to 250 ps with multiple outputs switching.

## Commercial Version SOIC, PCC and Cerpak AC Electrical Characteristics

$V_{EE} = -4.2V$  to  $-5.7V$ ,  $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_C = 0^\circ C$		$T_C = +25^\circ C$		$T_C = +85^\circ C$		Units	Conditions
		Min	Max	Min	Max	Min	Max		
$f_{shift}$	Shift Frequency	350		350		350		MHz	Figures 2, 3
$t_{PLH}$ $t_{PHL}$	Propagation Delay CP to $Q_n, \bar{Q}_n$	1.00	1.80	1.00	1.80	1.00	1.80	ns	Figures 1, 2 (Note 7)
$t_{PLH}$ $t_{PHL}$	Propagation Delay CP to $\bar{TC}$ (Shift)	2.10	3.30	2.10	3.30	2.10	3.50	ns	Figures 1, 7, 8 (Note 7)
$t_{PLH}$ $t_{PHL}$	Propagation Delay CP to $\bar{TC}$ (Count)	2.40	4.20	2.40	4.20	2.60	4.50	ns	Figures 1, 9 (Note 7)
$t_{PLH}$ $t_{PHL}$	Propagation Delay MR to $Q_n, \bar{Q}_n$	1.40	2.30	1.40	2.30	1.50	2.40	ns	Figures 1, 4 (Note 7)
$t_{PLH}$ $t_{PHL}$	Propagation Delay MR to $\bar{TC}$ (Count)	2.80	4.90	2.90	5.00	3.10	5.30	ns	Figures 1, 12 (Note 7)
$t_{PHL}$	Propagation Delay MR to $\bar{TC}$ (Shift)	2.40	3.80	2.40	3.80	2.50	3.90	ns	Figures 1, 10, 11 (Note 7)
$t_{PLH}$ $t_{PHL}$	Propagation Delay $D_0/\overline{CET}$ to $\bar{TC}$	1.80	2.90	1.80	2.90	1.90	3.10	ns	Figures 1, 5 (Note 7)
$t_{PLH}$ $t_{PHL}$	Propagation Delay $S_n$ to $\bar{TC}$	1.90	3.90	1.90	3.90	2.10	4.20	ns	
$t_{TLH}$ $t_{THL}$	Transition Time 20% to 80%, 80% to 20%	0.35	1.10	0.35	1.10	0.35	1.10	ns	Figures 1, 3
$t_s$	Setup Time $D_3$ $P_n$ $D_0/\overline{CET}$ $\overline{CEP}$ $S_n$ MR (Release Time)	0.90 1.40 1.20 1.30 3.30 2.50		0.90 1.40 1.20 1.30 3.30 2.50		0.90 1.40 1.20 1.30 3.30 2.50		ns	Figures 4, 6
$t_H$	Hold Time $D_3$ $P_n$ $D_0/\overline{CET}$ $\overline{CEP}$ $S_n$	0.30 0.20 0.20 0.10 0.00		0.30 0.20 0.20 0.10 0.00		0.30 0.20 0.20 0.10 0.00		ns	Figure 6
$t_{pw(H)}$	Pulse Width HIGH CP, MR	2.00		2.00		2.00		ns	Figures 3, 4
$t_{OSHL}$	Maximum Skew Common Edge Output-to-Output Variation Clock to Output Path		200		200		200	ps	PCC Only (Note 6)
$t_{OSLH}$	Maximum Skew Common Edge Output-to-Output Variation Clock to Output Path		200		200		200	ps	PCC Only (Note 6)
$t_{OST}$	Maximum Skew Opposite Edge Output-to-Output Variation Clock to Output Path		230		230		230	ps	PCC Only (Note 6)
$t_{ps}$	Maximum Skew Pin (Signal) Transition Variation Clock to Output Path		245		245		245	ps	PCC Only (Note 6)

## Commercial Version SOIC, PCC and Cerpak AC Electrical Characteristics (Continued)

**Note 6:** Output-to-Output Skew is defined as the absolute value of the difference between the actual propagation delay for any outputs within the same packaged device. The specifications apply to any outputs switching in the same direction either HIGH to LOW ( $t_{OSHL}$ ), or LOW to HIGH ( $t_{OSLH}$ ), or in opposite directions both HL and LH ( $t_{OST}$ ). Parameters  $t_{OST}$  and  $t_{ps}$  guaranteed by design

**Note 7:** The propagation delay specified is for single output switching. Delays may vary up to 250 ps with multiple outputs switching.

## Industrial Version PCC DC Electrical Characteristics

$V_{EE} = -4.2V$  to  $-5.7V$ ,  $V_{CC} = V_{CCA} = GND$ ,  $T_C = -40^\circ C$  to  $+85^\circ C$  (Note 8)

Symbol	Parameter	$T_C = -40^\circ C$		$T_C = 0^\circ C$ to $+85^\circ C$		Units	Conditions	
		Min	Max	Min	Max			
$V_{OH}$	Output HIGH Voltage	-1085	-870	-1025	-870	mV	$V_{IN} = V_{IH (Max)}$ or $V_{IL (Min)}$	Loading with 50Ω to -2.0V
$V_{OL}$	Output LOW Voltage	-1830	-1575	-1830	-1620	mV		
$V_{OHC}$	Output HIGH Voltage	-1095		-1035		mV	$V_{IN} = V_{IH (Min)}$ or $V_{IL (Max)}$	Loading with 50Ω to -2.0V
$V_{OLC}$	Output LOW Voltage		-1565		-1610	mV		
$V_{IH}$	Input HIGH Voltage	-1170	-870	-1165	-870	mV	Guaranteed HIGH Signal for All Inputs	
$V_{IL}$	Input LOW Voltage	-1830	-1480	-1830	-1475	mV	Guaranteed LOW Signal for All Inputs	
$I_{IL}$	Input LOW Current	0.50		0.50		μA	$V_{IN} = V_{IL (Min)}$	
$I_{IH}$	Input HIGH Current		240		240	μA	$V_{IN} = V_{IH (Max)}$	
$I_{EE}$	Power Supply Current	-165	-75	-165	-80	mA	Inputs Open	

**Note 8:** The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.



## Industrial Version PCC AC Electrical Characteristics

$V_{EE} = -4.2V$  to  $-5.7V$ ,  $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_C = -40^\circ C$		$T_C = +25^\circ C$		$T_C = +85^\circ C$		Units	Conditions
		Min	Max	Min	Max	Min	Max		
$f_{shift}$	Shift Frequency	325		350		350		MHz	Figures 2, 3
$t_{PLH}$ $t_{PHL}$	Propagation Delay CP to $Q_n$ , $\overline{Q}_n$	1.00	1.80	1.00	1.80	1.00	1.80	ns	Figures 1, 3 (Note 9)
$t_{PLH}$ $t_{PHL}$	Propagation Delay CP to $\overline{TC}$ (Shift)	2.00	3.30	2.10	3.30	2.10	3.50	ns	Figures 1, 7, 8 (Note 9)
$t_{PLH}$ $t_{PHL}$	Propagation Delay CP to $\overline{TC}$ (Count)	2.40	4.20	2.40	4.20	2.60	4.50	ns	Figures 1, 9 (Note 9)
$t_{PLH}$ $t_{PHL}$	Propagation Delay MR to $Q_n$ , $\overline{Q}_n$	1.40	2.30	1.40	2.30	1.50	2.40	ns	Figures 1, 4 (Note 9)
$t_{PLH}$ $t_{PHL}$	Propagation Delay MR to $\overline{TC}$ (Count)	2.80	4.90	2.90	5.00	3.10	5.30	ns	Figures 1, 12 (Note 9)
$t_{PHL}$	Propagation Delay MR to $\overline{TC}$ (Shift)	2.40	3.80	2.40	3.80	2.50	3.90	ns	Figures 1, 10, 11 (Note 9)
$t_{PLH}$ $t_{PHL}$	Propagation Delay $D_0/\overline{CET}$ to $\overline{TC}$	1.70	2.90	1.80	2.90	1.90	3.10	ns	Figures 1, 5 (Note 9)
$t_{PLH}$ $t_{PHL}$	Propagation Delay $S_n$ to $\overline{TC}$	1.80	3.90	1.90	3.90	2.10	4.20	ns	
$t_{TLH}$ $t_{THL}$	Transition Time 20% to 80%, 80% to 20%	0.20	1.90	0.35	1.10	0.35	1.10	ns	Figures 1, 3
$t_s$	Setup Time $D_3$ $P_n$ $D_0/\overline{CET}$ $\overline{CEP}$ $S_n$ MR (Release Time)	1.40 1.70 1.80 1.80 3.30 2.60		0.90 1.40 1.20 1.30 3.30 2.50		0.90 1.40 1.20 1.30 3.30 2.50		ns	Figure 6
$t_h$	Hold Time $D_3$ $P_n$ $D_0/\overline{CET}$ $\overline{CEP}$ $S_n$	0.90 1.00 0.70 0.60 0.00		0.30 0.20 0.20 0.10 0.00		0.30 0.20 0.20 0.10 0.00		ns	Figure 6
$t_{pw(H)}$	Pulse Width HIGH CP, MR	2.20		2.00		2.00		ns	Figures 3, 4

**Note 9:** The propagation delay specified is for single output switching. Delays may vary up to 250 ps with multiple outputs switching.

## Military Version DC Electrical Characteristics

$V_{EE} = -4.2V$  to  $-5.7V$ ,  $V_{CC} = V_{CCA} = GND$ ,  $T_C = -55^\circ C$  to  $+125^\circ C$

Symbol	Parameter	Min	Max	Units	$T_C$	Conditions	Notes	
$V_{OH}$	Output HIGH Voltage	-1025	-870	mV	$0^\circ C$ to $+125^\circ C$	$V_{IN} = V_{IH (Max)}$ or $V_{IL (Min)}$	Loading with $50\Omega$ to $-2.0V$	(Notes 10, 11, 12)
		-1085	-870	mV	$-55^\circ C$			
$V_{OL}$	Output LOW Voltage	-1830	-1620	mV	$0^\circ C$ to $+125^\circ C$	$V_{IN} = V_{IH (Min)}$ or $V_{IL (Max)}$	Loading with $50\Omega$ to $-2.0V$	(Notes 10, 11, 12)
		-1830	-1555	mV	$-55^\circ C$			
$V_{OHC}$	Output HIGH Voltage	-1035		mV	$0^\circ C$ to $+125^\circ C$	$V_{IN} = V_{IH (Min)}$ or $V_{IL (Max)}$	Loading with $50\Omega$ to $-2.0V$	(Notes 10, 11, 12)
		-1085		mV	$-55^\circ C$			
$V_{OLC}$	Output LOW Voltage		-1610	mV	$0^\circ C$ to $+125^\circ C$	$V_{IN} = V_{IH (Min)}$ or $V_{IL (Max)}$	Loading with $50\Omega$ to $-2.0V$	(Notes 10, 11, 12)
			-1555	mV	$-55^\circ C$			
$V_{IH}$	Input HIGH Voltage	-1165	-870	mV	$-55^\circ C$ to $+125^\circ C$	Guaranteed HIGH Signal for All Inputs	(Notes 10, 11, 12, 13)	
$V_{IL}$	Input LOW Voltage	-1830	-1475	mV	$-55^\circ C$ to $+125^\circ C$	Guaranteed LOW Signal for All Inputs	(Notes 10, 11, 12, 13)	
$I_{IL}$	Input LOW Current	0.50		$\mu A$	$-55^\circ C$ to $+125^\circ C$	$V_{EE} = -4.2V$ $V_{IN} = V_{IL (Min)}$	(Notes 10, 11, 12)	
$I_{IH}$	Input HIGH Current		240	$\mu A$	$0^\circ C$ to $+125^\circ C$	$V_{EE} = -5.7V$ $V_{IN} = V_{IH (Max)}$	(Notes 10, 11, 12)	
			340	$\mu A$	$-55^\circ C$			
$I_{EE}$	Power Supply Current			mA	$-55^\circ C$	Inputs Open $V_{EE} = -4.2V$ to $-4.8V$ $V_{EE} = -4.2V$ to $-5.7V$	(Notes 10, 11, 12)	
		-185	-70		to			
		-195	-70		$+125^\circ C$			

**Note 10:** F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals  $-55^\circ C$ ), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

**Note 11:** Screen tested 100% on each device at  $-55^\circ C$ ,  $+25^\circ C$ , and  $+125^\circ C$ , Subgroups 1, 2, 3, 7, and 8.

**Note 12:** Sample tested (Method 5005, Table I) on each manufactured lot at  $-55^\circ C$ ,  $+25^\circ C$ ,  $+125^\circ C$ , Subgroups A1, 2, 3, 7, and 8.

**Note 13:** Guaranteed by applying specified input condition and testing  $V_{OH}/V_{OL}$ .

## Military Version AC Characteristics

$$V_{EE} = -4.2V \text{ to } -5.7V, V_{CC} = V_{CCA} = GND$$

Symbol	Parameter	T <sub>C</sub> = -55°C		T <sub>C</sub> = +25°C		T <sub>C</sub> = +125°C		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
f <sub>shift</sub>	Shift Frequency	325		325		325		MHz	Figures 2, 3	(Note 17)
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay CP to Q <sub>n</sub> , $\overline{Q}_n$	0.40	2.30	0.50	2.20	0.40	2.50	ns	Figures 1, 3	(Notes 14, 15, 16, 18)
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay CP to $\overline{TC}$ (Shift)	1.30	3.90	1.70	3.80	1.70	4.20	ns	Figures 1, 7, 8	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay CP to $\overline{TC}$ (Count)	1.20	4.60	1.50	4.60	1.60	5.20	ns	Figures 1, 9	(Notes 14, 15, 16, 18)
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay MR to Q <sub>n</sub> , $\overline{Q}_n$	0.60	2.90	0.80	2.80	0.90	3.20	ns	Figures 1, 4	(Notes 14, 15, 16, 18)
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay MR to $\overline{TC}$ (Count)	2.30	5.20	2.70	5.20	2.90	5.90	ns	Figures 1, 12	
t <sub>PHL</sub>	Propagation Delay MR to $\overline{TC}$ (Shift)	2.10	4.30	2.20	4.10	2.40	4.70	ns	Figures 1, 10, 11	(Notes 14, 15, 16, 18)
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay D <sub>0</sub> / $\overline{CET}$ to $\overline{TC}$	0.70	3.20	1.00	3.20	1.30	4.10	ns	Figures 1, 5	(Notes 14, 15, 16, 18)
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay S <sub>n</sub> to $\overline{TC}$	1.30	4.10	1.50	4.20	1.70	4.90	ns		
t <sub>TLH</sub> t <sub>THL</sub>	Transition Time 20% to 80%, 80% to 20%	0.20	1.90	0.20	1.80	0.20	2.00	ns	Figures 1, 3	(Note 17)
t <sub>s</sub>	Setup Time D <sub>3</sub> P <sub>n</sub> D <sub>0</sub> / $\overline{CET}$ $\overline{CEP}$ S <sub>n</sub> MR (Release Time)	1.40 1.70 1.80 1.80 3.30 2.60		1.40 1.70 1.80 1.80 3.30 2.60		1.40 1.70 1.80 1.80 3.30 2.60		ns	Figure 6	(Note 17)
t <sub>h</sub>	Hold Time D <sub>3</sub> P <sub>n</sub> D <sub>0</sub> / $\overline{CET}$ $\overline{CEP}$ S <sub>n</sub>	0.90 1.00 0.70 0.60 0.00		0.90 1.00 0.70 0.60 0.00		0.90 1.00 0.70 0.60 0.00		ns	Figure 6	(Note 17)
t <sub>pw(H)</sub>	Pulse Width HIGH: CP MR	1.60 2.00		1.60 2.00		1.60 2.00		ns	Figures 3, 4	(Note 17)

**Note 14:** F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals -55°C), then testing immediately after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

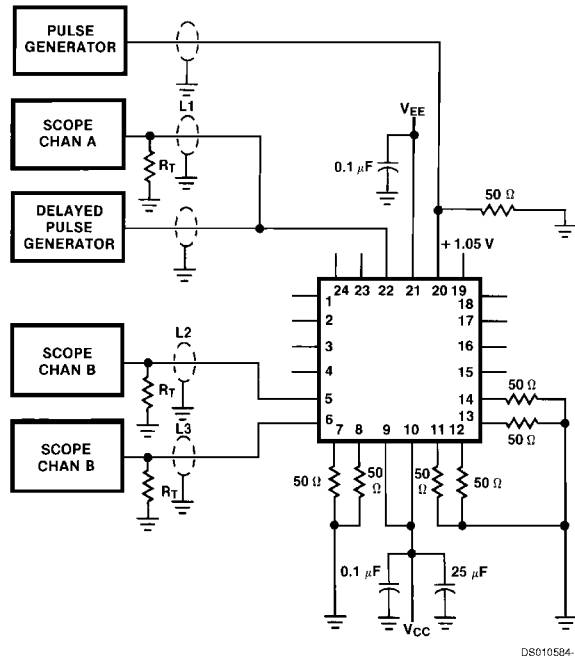
**Note 15:** Screen tested 100% on each device at +25°C temperature only, Subgroups A9.

**Note 16:** Sample tested (Method 5005, Table I) on each manufactured lot at +25°C, Subgroups A9, and at +125°C and -55°C temperatures, Subgroups A10 and A11.

**Note 17:** Not tested at +25°C, +125°C, and -55°C temperature (design characterization data).

**Note 18:** The propagation delay specified is for single output switching. Delays may vary up to 250 ps with multiple outputs switching.

## Test Circuitry



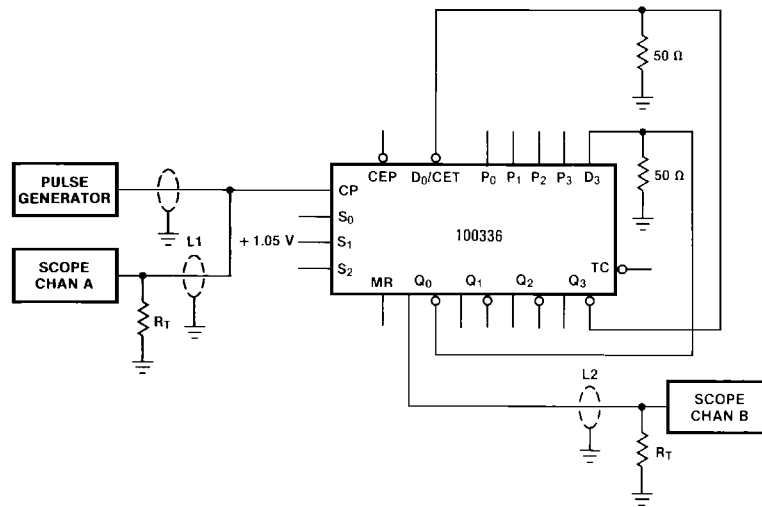
DS010584-6

### Notes:

$V_{CC}$ ,  $V_{CCA} = +2V$ ,  $V_{EE} = -2.5V$   
 $L1$ ,  $L2$  and  $L3$  = equal length  $50\Omega$  impedance lines  
 $R_T$  =  $50\Omega$  terminator internal to scope  
 Decoupling  $0.1\mu F$  from GND to  $V_{CC}$  and  $V_{EE}$   
 All unused outputs are loaded with  $50\Omega$  to GND  
 $C_L$  = Fixture and stray capacitance  $\leq 3\text{ pF}$   
 Pin numbers shown are for flatpak;  
 for DIP see logic symbol

FIGURE 1. AC Test Circuit

## Test Circuitry (Continued)



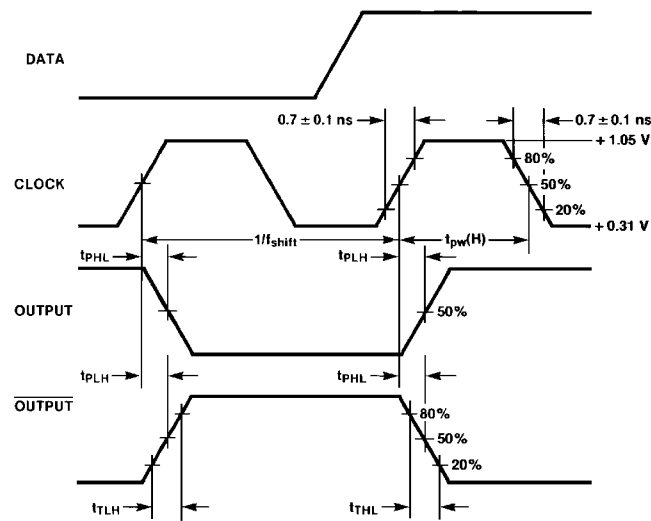
DS010584-7

### Notes:

For shift right mode, +1.05V is applied at  $S_0$ .  
The feedback path from output to input should be as short as possible.

FIGURE 2. Shift Frequency Test Circuit (Shift Left)

## Switching Waveforms



DS010584-8

FIGURE 3. Propagation Delay (Clock) and Transition Times

## Switching Waveforms (Continued)

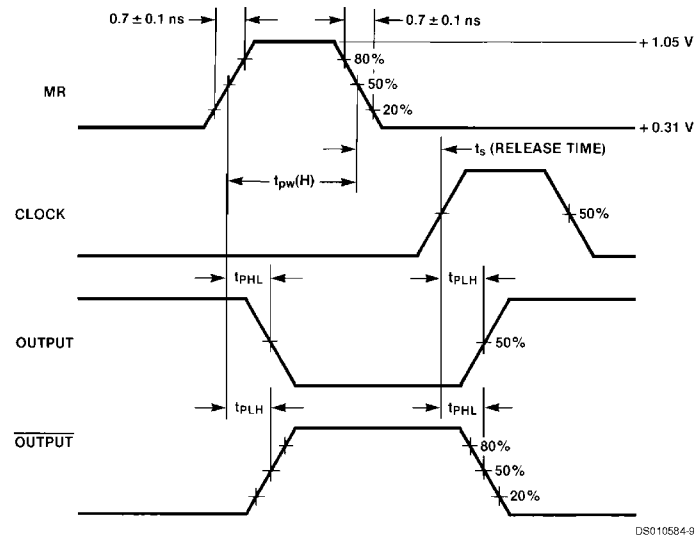


FIGURE 4. Propagation Delay (Reset)

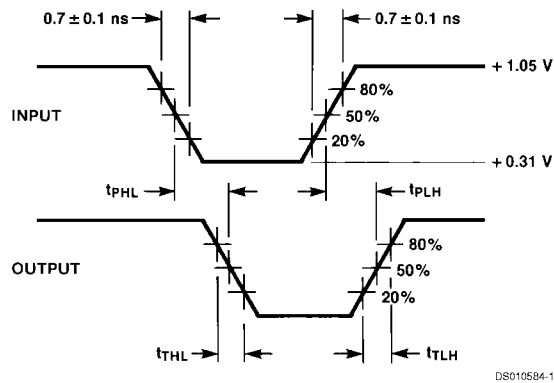
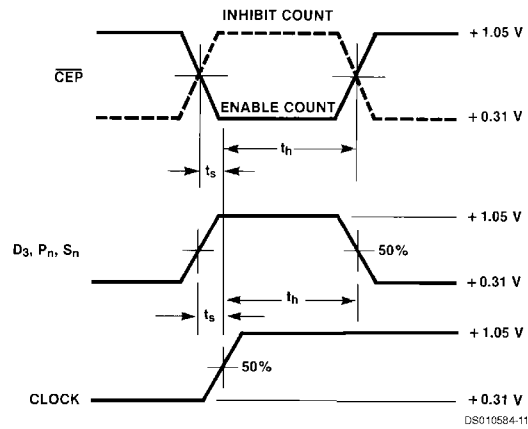


FIGURE 5. Propagation Delay (Serial Data, Selects)

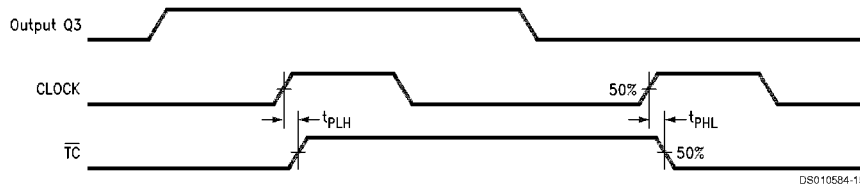
## Switching Waveforms (Continued)



**Notes:**

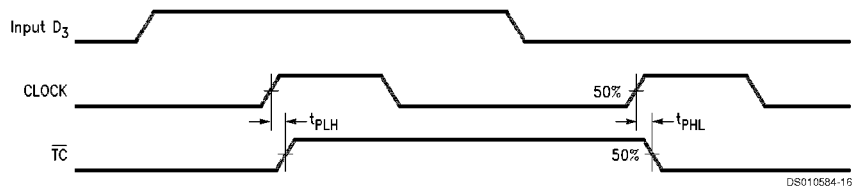
$t_s$  is the minimum time before the transition of the clock that information must be present at the data input.  
 $t_h$  is the minimum time after the transition of the clock that information must remain unchanged at the data input.

**FIGURE 6. Setup and Hold Time**



**Note:** Shift Right Mode;  $S_0 = H$ ,  $S_1 = H$ ,  $S_2 = L$ .

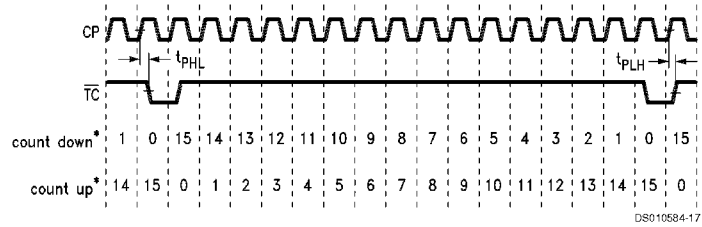
**FIGURE 7. Propagation Delay, Clock to Terminal Count (Shift Right Mode)**



**Note:** Shift Left Mode;  $S_0 = L$ ,  $S_1 = H$ ,  $S_2 = L$ .

**FIGURE 8. Propagation Delay, Clock to Terminal Count (Shift Left Mode)**

## Switching Waveforms (Continued)



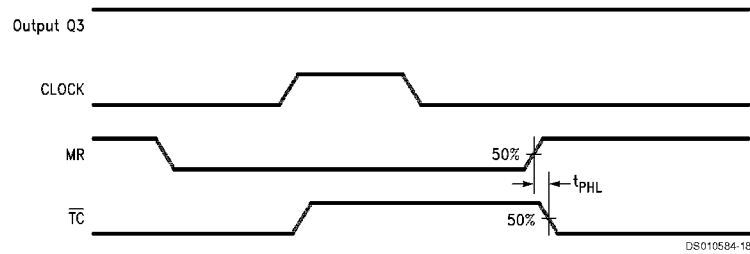
**Note:**

\*Decimal representation of binary outputs.

Count Up:  $S_0 = L, S_1 = H, S_2 = H$ ; Count Down:  $S_0 = L, S_1 = L, S_2 = H$ .

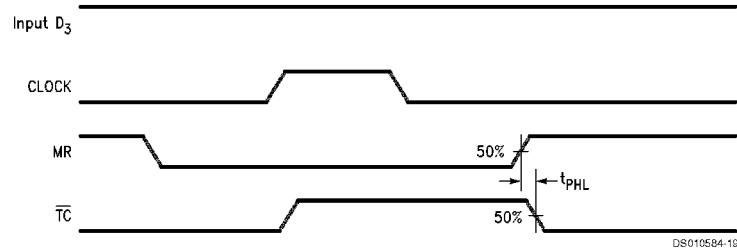
Measurement taken at 50% point of waveform.

**FIGURE 9. Propagation Delay, Clock to Terminal Count (Count Up and Count Down Modes)**



**Note:** Shift Right Mode;  $S_0 = H, S_1 = H, S_2 = L$ .

**FIGURE 10. Propagation Delay, Master Reset to Terminal Count (Shift Right Mode)**

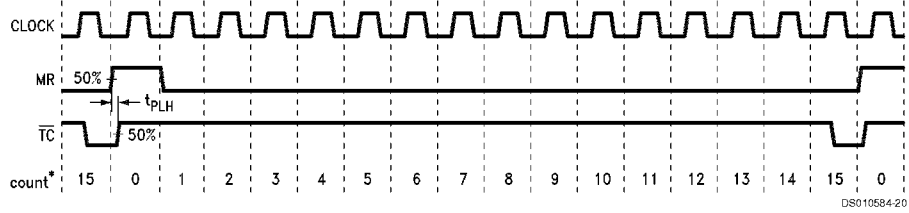


**Note:** Shift Left Mode;  $S_0 = L, S_1 = H, S_2 = L$ .

**FIGURE 11. Propagation Delay, Master Reset to Terminal Count (Shift Left Mode)**

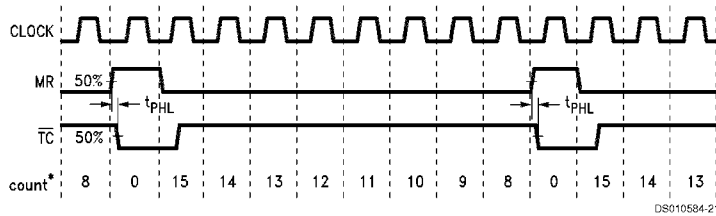


## Switching Waveforms (Continued)



**Note:**

\*Decimal representation of binary outputs. Count Up Mode:  $S_0 = L, S_1 = H, S_2 = H$ .

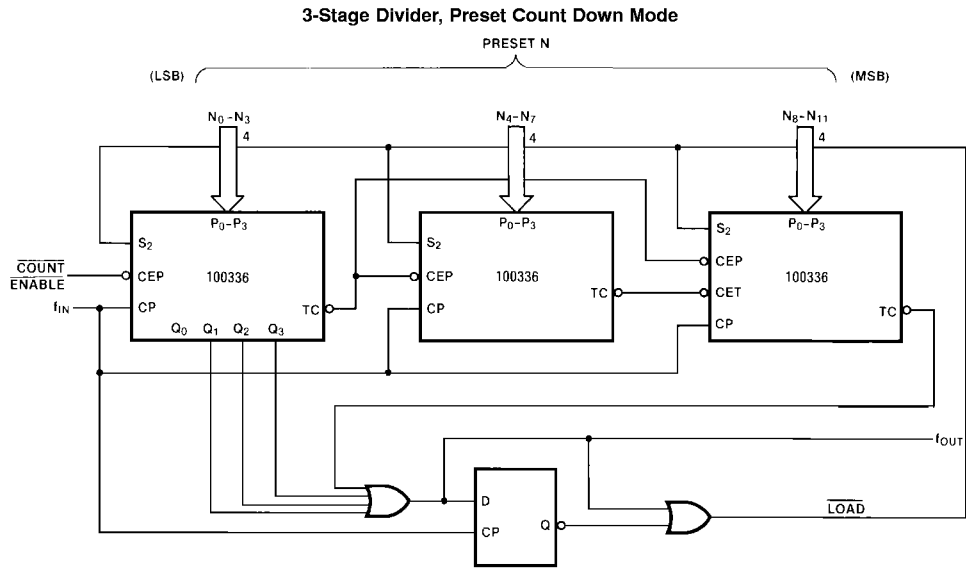


**Note:**

\*Decimal representation of binary outputs. Count Down Mode:  $S_0 = L, S_1 = L, S_2 = H$ .

**FIGURE 12. Propagation Delay, Master Reset to Terminal Count (Count Up and Count Down Modes)**

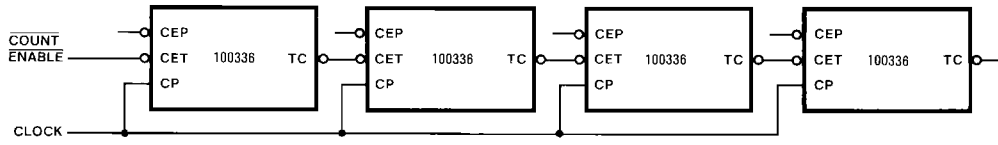
## Applications



**Note:** If  $S_0 = S_1 = S_2 = LOW$ , then  $T_C = LOW$

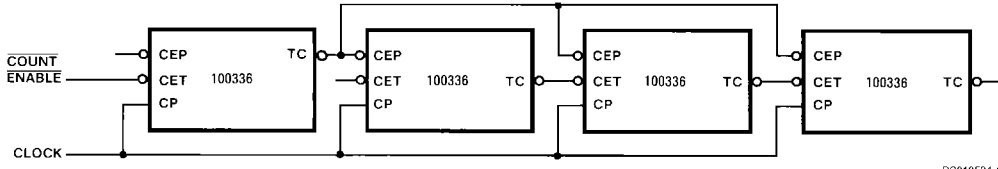
## Applications (Continued)

### Slow Expansion Scheme



DS010584-13

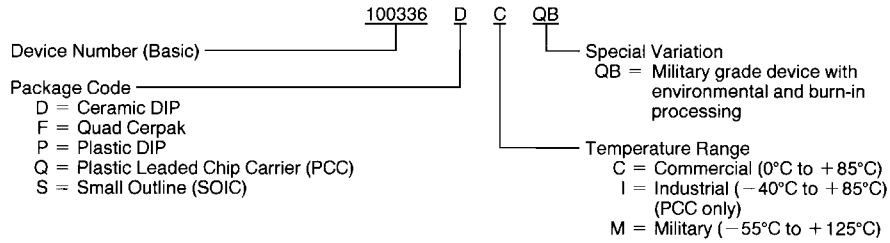
### Fast Expansion Scheme



DS010584-14

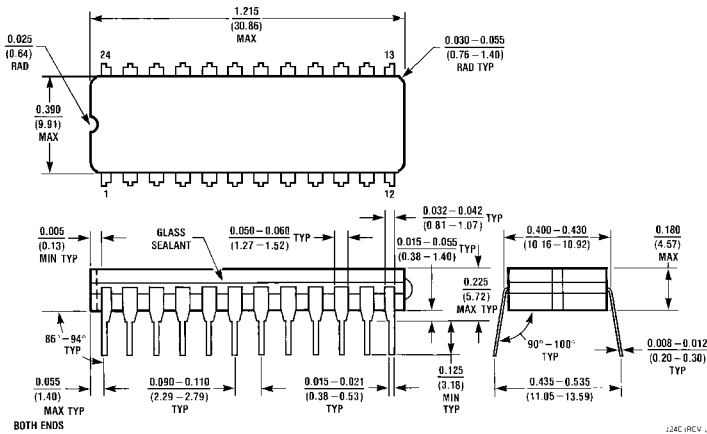
## Ordering Information

The device number is used to form part of a simplified purchasing code where a package type and temperature range are defined as follows:



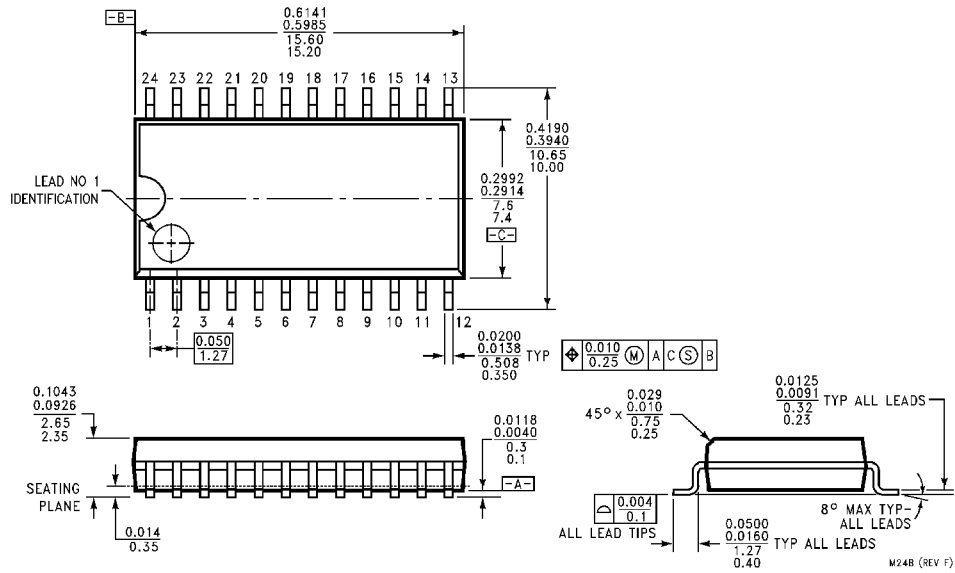
DS010584-22

## Physical Dimensions inches (millimeters) unless otherwise noted

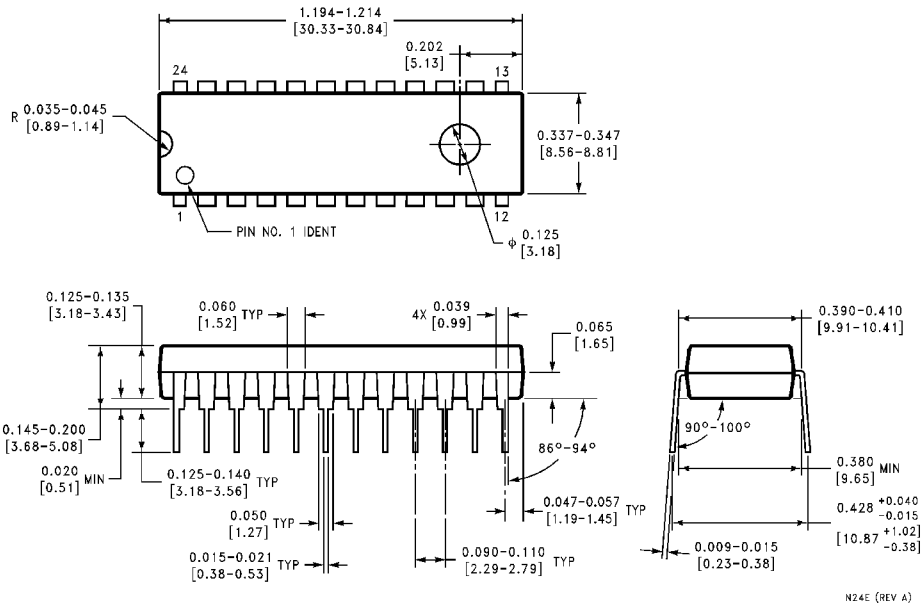


24-Lead Ceramic Dual-In-Line Package (0.400" Wide) (D)  
 Package Number J24E

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)

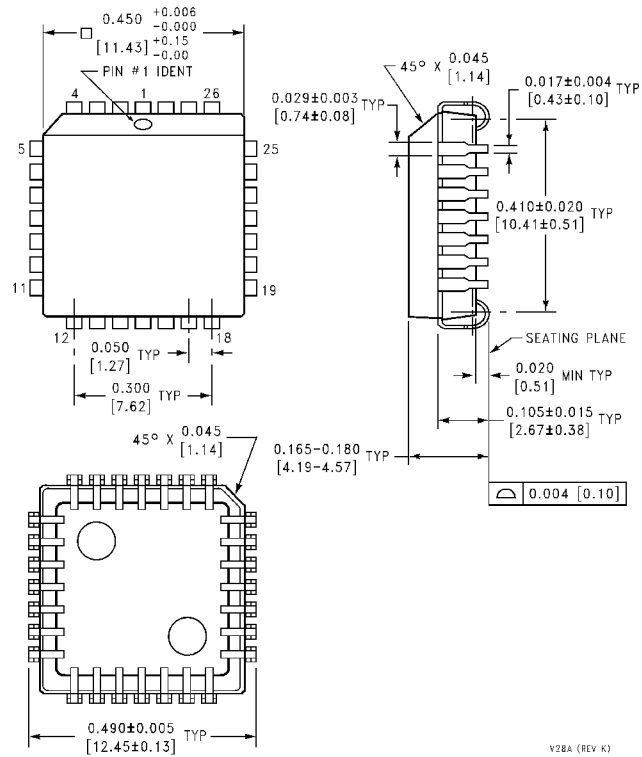


**24-Lead Molded Package (0.300" Wide) (S)**  
**Package Number M24B**



**24-Lead Plastic Dual-In-Line Package (P)**  
**Package Number N24E**

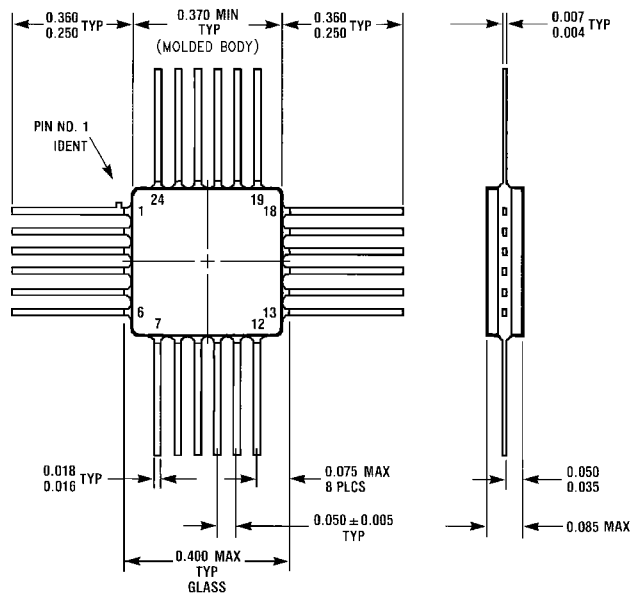
**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**28-Lead Plastic Chip Carrier (Q)  
Package Number V28A**

V28A (REV K)

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



W24B (REV D)

**24-Lead Quad Cerpak (F)  
Package Number W24B**

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