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# MAX9273

# 22-Bit GMSL Serializer with Coax or STP Cable Drive

## General Description

The MAX9273 compact serializer is designed to drive 50Ω coax or 100Ω shielded twisted-pair (STP) cable. The device pairs with the MAX9272 deserializer. The parallel input is programmable for single or double input. Double input allows higher pixel clock input frequency by registering two pixels of typical image-sensor video data before serializing. This doubles the maximum pixel clock frequency compared to single input.

The device features an embedded control channel that operates at 9.6kbps to 1Mbps in UART and mixed UART/I²C modes, and up to 400kbps in I²C mode. Using the control channel, a microcontroller (µC) is capable of programming serializer, deserializer, and camera (or any peripheral) registers at any time, independent of video timing. There is one dedicated GPIO, four optional GPIOs, and a GPO output, allowing remote power-up of a camera module, camera frame synchronization, and other uses. Error-detection and correction coding are programmable.

For driving longer cables, the serializer has programmable pre/deemphasis. Programmable spread spectrum is available on the serial output. The serial output meets ISO 10605 and IEC 61000-4-2 ESD standards. The core supply range is 1.7V to 1.9V and the I/O supply range is 1.7V to 3.6V. The device is available in a 40-pin (6mm x 6mm) TQFN-EP package with 0.5mm lead pitch and operates over the -40°C to +105°C temperature range.

## Applications

Automotive Camera Systems

Navigation Displays

*Ordering Information appears at end of data sheet.*

*Typical Application Circuit appears at end of data sheet.*

*For related parts and recommended products to use with this part, refer to www.maximintegrated.com/MAX9273.related.*

## Benefits and Features

- **Ideal for Camera Applications**
  - **Drives Low-Cost 50Ω Coax Cable and FAKRA Connectors or 100Ω STP**
  - **Error Detection/Correction**
  - **9.6kbps to 1Mbps Control Channel in I²C-to-I²C Mode with Clock Stretch Capability**
  - **Best-in-Class Supply Current: 75mA (max)**
  - **Double-Rate Clock for Megapixel Cameras**
  - **Serializer Pre/Deemphasis Allows 15m Cable at Full Speed**
  - **40-Pin (6mm x 6mm) TQFN Package with 0.5mm Lead Pitch**
- **High-Speed Data Serialization for Megapixel Cameras**
  - **Up to 1.5Gbps Serial-Bit Rate with Single or Double Input: 6.25MHz to 100MHz Clock**
- **Multiple Control-Channel Modes for System Flexibility**
  - **9.6kbps to 1Mbps Control Channel in UART-to-UART or UART-to-I²C Modes**
- **Reduces EMI and Shielding Requirements**
  - **Output Programmable for 100mV to 500mV Single-Ended or 100mV to 400mV Differential**
  - **Programmable Spread Spectrum on the Serial Output Reduces EMI**
  - **Bypassable Input PLL for Parallel Clock Jitter Attenuation**
  - **Tracks Spread Spectrum on Parallel Input**
- **Peripheral Features for Camera Power-Up and Verification**
  - **Built-In PRBS Generator for BER Testing of the Serial Link**
  - **Up to Five GPIO Ports**
  - **Dedicated "Up/Down" GPO for Camera Frame Sync Trigger and Other Uses**
- **Reduces Power Requirements**
  - **Remote/Local Wake-Up from Sleep Mode**
- **Meets Rigorous Automotive and Industrial Requirements**
  - **-40°C to +105°C Operating Temperature**
  - **±8kV Contact and ±15kV Air ISO 10605 and IEC 61000-4-2 ESD Protection**

**For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maximintegrated.com.**

*19-6384; Rev 1; 11/12*

# MAX9273

# 22-Bit GMSL Serializer with Coax or STP Cable Drive

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## ABSOLUTE MAXIMUM RATINGS*

AVDD to EP ..... -0.5V to +1.9V
DVDD to EP ..... -0.5V to +1.9V
IOVDD to EP ..... -0.5V to +3.9V
OUT+, OUT- to EP ..... -0.5V to +1.9V
All other pins to EP ..... -0.5V to ($V_{IOVDD}$ + 0.5V)
OUT+, OUT- short circuit to ground or supply ..... Continuous

Continuous Power Dissipation ($T_A$ = +70°C)
TQFN (derate 37mW/°C above +70°C) ..... 2963mW
Junction Temperature ..... +150°C
Operating Temperature Range ..... -40ºC to +105°C
Storage Temperature Range ..... -65ºC to +150°C
Lead Temperature (soldering, 10s) ..... +300°C
Soldering Temperature (reflow) ..... +260°C

**EP connected to PCB ground.*

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## PACKAGE THERMAL CHARACTERISTICS (Note 1)

TQFN
Junction-to-Ambient Thermal Resistance ($\theta_{JA}$) ..... 27°C/W
Junction-to-Case Thermal Resistance ($\theta_{JC}$) ..... 1°C/W

**Note 1:** Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

## DC ELECTRICAL CHARACTERISTICS

($V_{AVDD}$ = $V_{DVDD}$ = 1.7V to 1.9V, $V_{IOVDD}$ = 1.7V to 3.6V, $R_L$= 100Ω ±1% (differential), EP connected to PCB ground (GND), $T_A$ = -40°C to +105°C, unless otherwise noted. Typical values are at $V_{AVDD}$ = $V_{DVDD}$ = $V_{IOVDD}$ = 1.8V, $T_A$ = +25°C.)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **SINGLE-ENDED INPUTS (DIN_, HS, VS, MS, $\overline{PWDN}$, DRS, $\overline{AUTOS}$, PCLKIN)** | | | | | | | |
| High-Level Input Voltage | $V_{IH1}$ | | | 0.65 x $V_{IOVDD}$ | | | V |
| Low-Level Input Voltage | $V_{IL1}$ | | | | | 0.35 x $V_{IOVDD}$ | V |
| Input Current | $I_{IN1}$ | $V_{IN}$ = 0V to $V_{IOVDD}$ | | -10 | | +20 | µA |
| **THREE-LEVEL LOGIC INPUTS (CONF0, CONF1)** | | | | | | | |
| High-Level Input Voltage | $V_{IH}$ | | | 0.7 x $V_{IOVDD}$ | | | V |
| Low-Level Input Voltage | $V_{IL}$ | | | | | 0.3 x $V_{IOVDD}$ | V |
| Midlevel Input Current | $I_{INM}$ | (Note 2) | | -10 | | +10 | µA |
| Input Current | $I_{IN}$ | | | -150 | | +150 | µA |
| **SINGLE-ENDED OUTPUT (GPO)** | | | | | | | |
| High-Level Output Voltage | $V_{OH1}$ | $I_{OUT}$ = -2mA | | $V_{IOVDD}$ - 0.2 | | | V |
| Low-Level Output Voltage | $V_{OL1}$ | $I_{OUT}$ = 2mA | | | | 0.2 | V |
| Output Short-Circuit Current | $I_{OS}$ | $V_O$ = 0V | $V_{IOVDD}$ = 3.0V to 3.6V | 16 | 35 | 64 | mA |
| | | | $V_{IOVDD}$ = 1.7V to 1.9V | 3 | 12 | 21 | |

## DC ELECTRICAL CHARACTERISTICS (continued)

($V_{AVDD}$ = $V_{DVDD}$ = 1.7V to 1.9V, $V_{IOVDD}$ = 1.7V to 3.6V, $R_L$= 100Ω ±1% (differential), EP connected to PCB ground (GND), $T_A$ = -40°C to +105°C, unless otherwise noted. Typical values are at $V_{AVDD}$ = $V_{DVDD}$ = $V_{IOVDD}$ = 1.8V, $T_A$ = +25°C.)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **OPEN-DRAIN INPUTS/OUTPUTS (RX/SDA, TX/SCL, GPIO_)** | | | | | | | |
| High-Level Input Voltage | $V_{IH2}$ | | | 0.7 x $V_{IOVDD}$ | | | V |
| Low- Level Input Voltage | $V_{IL2}$ | | | | | 0.3 x $V_{IOVDD}$ | V |
| Input Current | $I_{IN2}$ | (Note 3) | RX/SDA, TX/SCL | -110 | | +1 | µA |
| | | | GPIO_ | -80 | | +1 | |
| Low-Level Output Voltage | $V_{OL2}$ | $I_{OUT}$ = 3mA | $V_{IOVDD}$ = 1.7V to 1.9V | | | 0.4 | V |
| | | | $V_{IOVDD}$ = 3.0V to 3.6V | | | 0.3 | |
| **DIFFERENTIAL SERIAL OUTPUTS (OUT+, OUT-)** | | | | | | | |
| Differential Output Voltage | $V_{OD}$ | Preemphasis off (Figure 1) | | 300 | 400 | 500 | mV |
| | | 3.3dB preemphasis setting (Figure 2) | | 350 | | 610 | |
| | | 3.3dB deemphasis setting (Figure 2) | | 240 | | 425 | |
| Change in $V_{OD}$ Between Complementary Output States | $\Delta V_{OD}$ | | | | | 25 | mV |
| Output Offset Voltage ($V_{OUT+}$ + $V_{OUT-}$)/2 = $V_{OS}$ | $V_{OS}$ | Preemphasis off | | 1.1 | 1.4 | 1.56 | V |
| Change in $V_{OS}$ Between Complementary Output States | $\Delta V_{OS}$ | | | | | 25 | mV |
| Output Short-Circuit Current | $I_{OS}$ | $V_{OUT+}$ or $V_{OUT-}$ = 0V | | -62 | | | mA |
| | | $V_{OUT+}$ or $V_{OUT-}$ = 1.9V | | | | 25 | |
| Magnitude of Differential Output Short-Circuit Current | $I_{OSD}$ | $V_{OD}$ = 0V | | | | 25 | mA |
| Output Termination Resistance (Internal) | $R_O$ | From $V_{OUT+}$, $V_{OUT-}$ to $V_{AVDD}$ | | 45 | 54 | 63 | Ω |
| **SINGLE-ENDED SERIAL OUTPUTS (OUT+, OUT-)** | | | | | | | |
| Single-Ended Output Voltage | $V_{OD}$ | Preemphasis off, high drive (Figure 3) | | 375 | 500 | 625 | mV |
| | | 3.3dB preemphasis setting, high drive (Figure 2) | | 435 | | 765 | |
| | | 3.3dB deemphasis setting, high drive (Figure 2) | | 300 | | 535 | |
| Output Short-Circuit Current | $I_{OS}$ | $V_{OUT+}$ or $V_{OUT-}$ = 0V | | -69 | | | mA |
| | | $V_{OUT+}$ or $V_{OUT-}$ = 1.9V | | | | 32 | |
| Output Termination Resistance (Internal) | $R_O$ | From $V_{OUT+}$ or $V_{OUT-}$ to $V_{AVDD}$ | | 45 | 54 | 63 | Ω |

## DC ELECTRICAL CHARACTERISTICS (continued)

($V_{AVDD}$ = $V_{DVDD}$ = 1.7V to 1.9V, $V_{IOVDD}$ = 1.7V to 3.6V, $R_L$= 100Ω ±1% (differential), EP connected to PCB ground (GND), $T_A$ = -40°C to +105°C, unless otherwise noted. Typical values are at $V_{AV\ DD}$ = $V_{DVDD}$ = $V_{IOVDD}$ = 1.8V, $T_A$ = +25°C.)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **REVERSE CONTROL-CHANNEL RECEIVER OUTPUTS (OUT+, OUT-)** | | | | | | | |
| High Switching Threshold | $V_{CHR}$ | | | | | 27 | mV |
| Low Switching Threshold | $V_{CLR}$ | | | -27 | | | mV |
| **POWER SUPPLY** | | | | | | | |
| Worst-Case Supply Current (Figure 4) | $I_{WCS}$ | Single input, BWS = 0 | $f_{PCLKIN}$ = 25MHz | | 40 | 65 | mA |
| | | | $f_{PCLKIN}$ = 50MHz | | 50 | 75 | |
| | | Double input, BWS = 0 | $f_{PCLKIN}$ = 50MHz | | 40 | 65 | |
| | | | $f_{PCLKIN}$ = 100MHz | | 51 | 75 | |
| Sleep Mode Supply Current | $I_{CCS}$ | Single wake-up receiver enabled | | | 40 | 100 | µA |
| Power-Down Supply Current | $I_{CCZ}$ | $\overline{PWDN}$ = EP | | | 5 | 70 | µA |
| **ESD PROTECTION** | | | | | | | |
| OUT+, OUT- (Note 4) | $V_{ESD}$ | Human Body Model, $R_D$ = 1.5kΩ, $C_S$ = 100pF | | ±8 | | | kV |
| | | IEC 61000-4-2, $R_D$ = 330Ω, $C_S$ = 150pF | Contact discharge | ±10 | | | |
| | | | Air discharge | ±15 | | | |
| | | ISO 10605, $R_D$ = 2kΩ, $C_S$ = 330pF | Contact discharge | ±10 | | | |
| | | | Air discharge | ±30 | | | |
| All Other Pins (Note 5) | $V_{ESD}$ | Human Body Model, $R_D$ = 1.5kΩ, $C_S$ = 100pF | | ±4 | | | kV |

## AC ELECTRICAL CHARACTERISTICS

($V_{DVDD}$ = $V_{AVDD}$ = 1.7V to 1.9V, $V_{IOVDD}$ = 1.7V to 3.6V, $R_L$ = 100Ω ±1% (differential), EP connected to PCB ground (GND), $T_A$ = -40°C to +105°C, unless otherwise noted. Typical values are at $V_{DVDD}$ = $V_{AVDD}$ = $V_{IOVDD}$ = 1.8V, $T_A$ = +25°C)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **CLOCK INPUT (PCLKIN)** | | | | | | |
| Clock Frequency | $f_{PCLKIN}$ | BWS = 1, DRS = 1 | 6.25 | | 12.5 | MHz |
| | | BWS = 0, DRS = 1 | 8.33 | | 16.66 | |
| | | BWS = 1, DRS = 0 | 12.5 | | 37.5 | |
| | | BWS = 0, DRS = 0 | 16.66 | | 50 | |
| | | BWS = 1, DRS = 0, 15-bit double input | 25 | | 75 | |
| | | BWS = 0, DRS = 0, 11-bit double input | 33.33 | | 100 | |
| Clock Duty Cycle | DC_ | $t_{HIGH}/t_T$ or $t_{LOW}/t_T$ (Figure 5, Note 6) | 35 | 50 | 65 | % |
| Clock Transition Time | $t_R$, $t_{F_}$ | (Figure 5, Note 6) | | | 4 | ns |
| Clock Jitter | $t_J$ | 1.5Gbps bit rate, 300kHz sinusoidal jitter | | | 800 | ps (pk-pk) |

## AC ELECTRICAL CHARACTERISTICS (continued)

($V_{DVDD}$ = $V_{AVDD}$ = 1.7V to 1.9V, $V_{IOVDD}$ = 1.7V to 3.6V, $R_L$ = 100Ω ±1% (differential), EP connected to PCB ground (GND), $T_A$ = -40°C to +105°C, unless otherwise noted. Typical values are at $V_{DVDD}$ = $V_{AVDD}$ = $V_{IOVDD}$ = 1.8V, $T_A$ = +25°C)

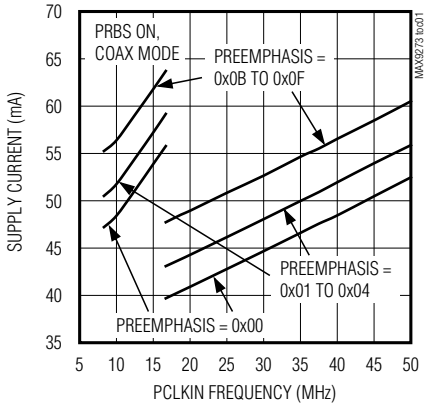
| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **I²C/UART and GPIO Port Timing** | | | | | | | |
| I²C/UART Bit Rate | | | | 9.6 | | 1000 | kbps |
| Output Rise Time | $t_R$ | 30% to 70%, $C_L$ = 10pF to 100pF, 1kΩ pullup to IOVDD | | 20 | | 120 | ns |
| Output Fall Time | $t_F$ | 70% to 30%, $C_L$ = 10pF to 100pF, 1kΩ pullup to IOVDD | | 20 | | 120 | ns |
| Input Setup Time | $t_{SET}$ | I²C only (Figure 6, Note 6) | | 100 | | | ns |
| Input Hold Time | $t_{HOLD}$ | I²C only (Figure 6, Note 6) | | 0 | | | ns |
| **SWITCHING CHARACTERISTICS (Note 6)** | | | | | | | |
| Differential Output Rise/Fall Time | $t_R$, $t_F$ | 20% to 80%, $V_{OD} \geq$ 400mV $R_L$ = 100Ω, serial-bit rate = 1.5Gbps | | | | 250 | ps |
| Total Serial Output Jitter (Differential Output) | $t_{TSOJ1}$ | 1.5Gbps PRBS signal, measured at $V_{OD}$ = 0V differential, preemphasis disabled (Figure 7) | | | 0.25 | | UI |
| Deterministic Serial Output Jitter (Differential Output) | $t_{DSOJ2}$ | 1.5Gbps PRBS signal, measured at $V_{OD}$ = 0V differential, preemphasis disabled (Figure 7) | | | 0.15 | | UI |
| Total Serial Output Jitter (Single-Ended Output) | $t_{TSOJ1}$ | 1.5Gbps PRBS signal, measured at $V_O$/2, preemphasis disabled (Figure 3) | | | 0.25 | | UI |
| Deterministic Serial Output Jitter (Single-Ended Output) | $t_{DSOJ2}$ | 1.5Gbps PRBS signal, measured at $V_O$/2, preemphasis disabled (Figure 3)1.5Gbps PRBS signal | | | 0.15 | | UI |
| Parallel Data Input Setup Time | $t_{SET}$ | (Figure 8) | | 2 | | | ns |
| Parallel Data Input Hold Time | $t_{HOLD}$ | (Figure 8) | | 1 | | | ns |
| GPI-to-GPO Delay | $t_{GPIO_}$ | Deserializer GPI to serializer GPO (Figure 9) | | | | 350 | µs |
| Serializer Delay (Note 7) | $t_{SD}$ | (Figure 10) | Spread spectrum enabled | | | 6880 | Bits |
| | | | Spread spectrum disabled | | | 3040 | |
| Link Start Time | $t_{LOCK}$ | (Figure 11) | | | | 2 | ms |
| Power-Up Time | $t_{PU}$ | (Figure 12) | | | | 7 | ms |

**Note 2:** To provide a midlevel, leave the input open, or, if driven, put driver in high impedance. High-impedance leakage current must be less than ±10µA.
**Note 3:** $I_{IN}$ min due to voltage drop across the internal pullup resistor.
**Note 4:** Specified pin to ground.
**Note 5:** Specified pin to all supply/ground.
**Note 6:** Guaranteed by design and not production tested.
**Note 7:** Measured in serial link bit times. Bit time = 1/(30 x $f_{PCLKIN}$) for BWS = 0. Bit time = 1/(40 x $f_{PCLKIN}$) for BWS = 1.

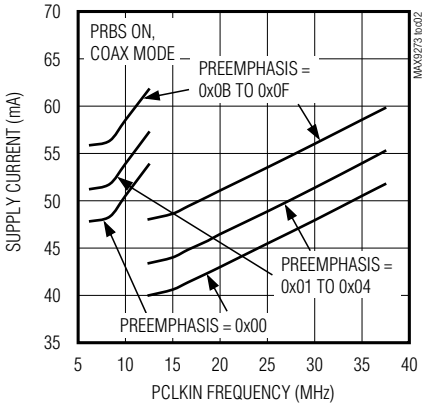
## *Typical Operating Characteristics*

($V_{AVDD}$ = $V_{DVDD}$ = $V_{IOVDD}$ = 1.8V, DBL = low, $T_A$ = +25°C, unless otherwise noted.)

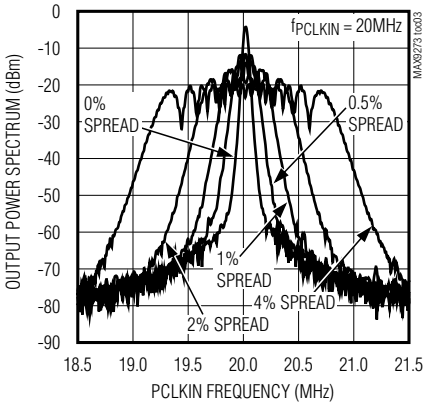
**SUPPLY CURRENT vs.PCLKIN FREQUENCY (BWS = 0)**



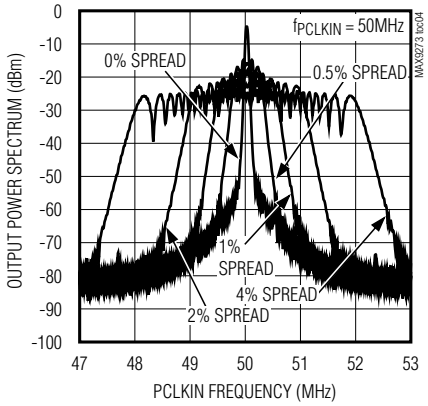

**SUPPLY CURRENT vs. PCLKIN FREQUENCY (BWS = 1)**



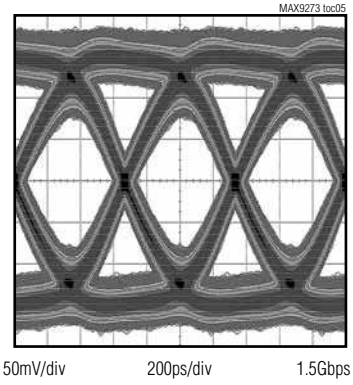

**OUTPUT POWER SPECTRUM vs. PCLKIN FREQUENCY (VARIOUS SPREAD)**



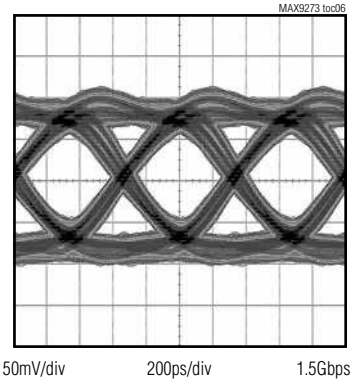

**OUTPUT POWER SPECTRUM vs. PCLKIN FREQUENCY (VARIOUS SPREAD)**



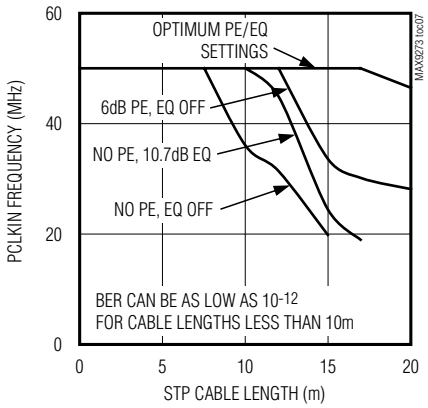

**SERIAL LINK SWITCHING PATTERN WITH 6dB PREEMPHASIS (PARALLEL BIT RATE = 50MHz, 10m STP CABLE)**



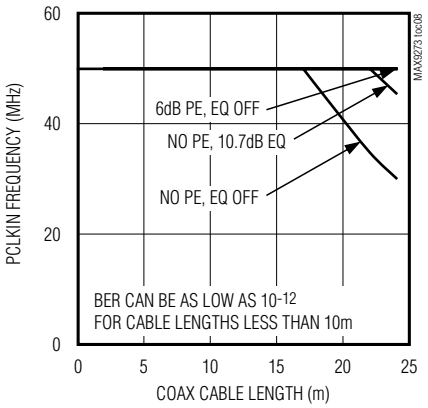

**SERIAL LINK SWITCHING PATTERN WITH 6dB PREEMPHASIS (PARALLEL BIT RATE = 50MHz, 20m COAX CABLE)**



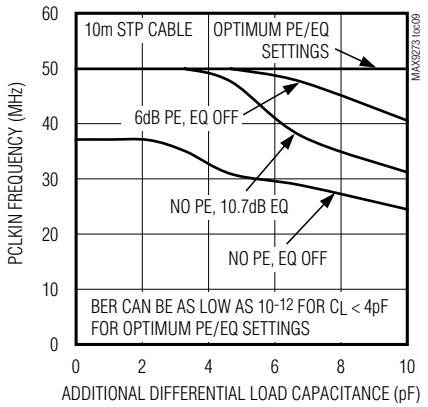

**MAXIMUM PCLKIN FREQUENCY vs. STP CABLE LENGTH (BER ≤ $10^{-10}$)**



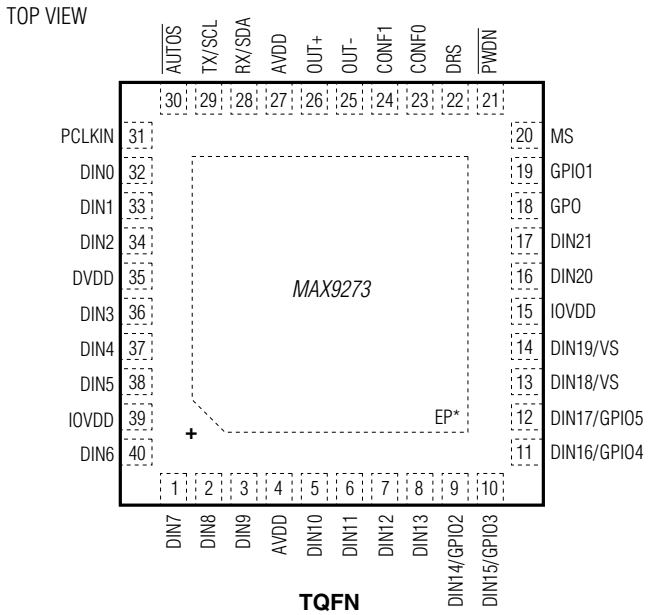

**MAXIMUM PCLKIN FREQUENCY vs. COAX CABLE LENGTH (BER ≤ $10^{-10}$)**




**MAXIMUM PCLKIN FREQUENCY vs. ADDITIONAL DIFFERENTIAL $C_L$ (BER < $10^{-10}$)**



## Pin Configuration




**TQFN**
**(6mm x 6mm x 0.75mm)**
**CONNECT EP TO GROUND PLANE**

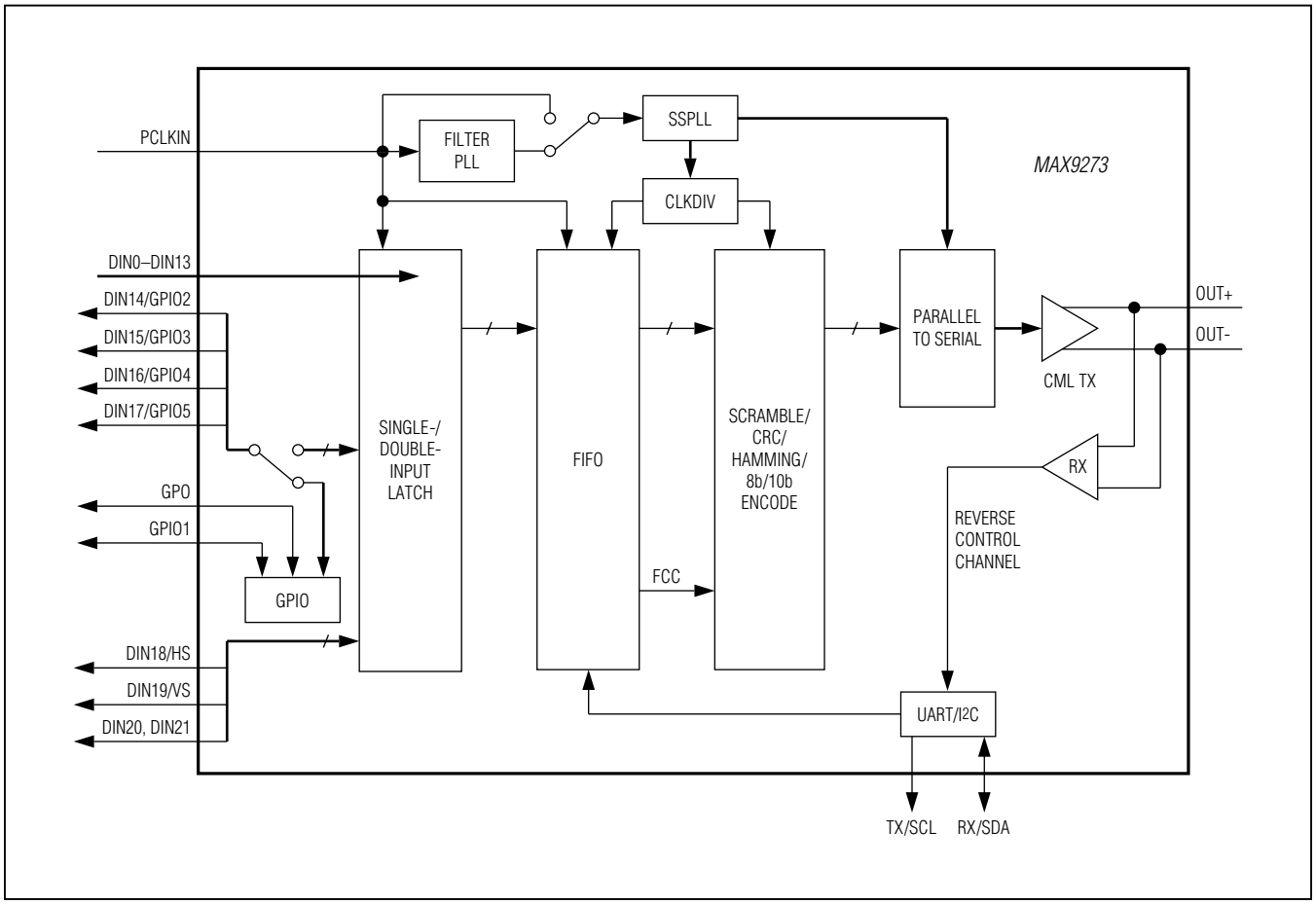
## Pin Description

| PIN | NAME | FUNCTION |
|---|---|---|
| 1, 2, 3, 5–8, 16, 17, 32, 33, 34, 36, 37, 38 | DIN0–DIN13, DIN20, DIN21 | Parallel Data Inputs with Internal Pulldown to EP |
| 4, 27 | AVDD | 1.8V Analog Power Supply. Bypass AVDD to EP with 0.1µF and 0.001µF capacitors as close as possible to the device with the smaller capacitor closest to AVDD. |
| 9–12 | DIN14/ GPIO2–DIN17/ GPIO5 | Parallel Data Inputs/GPIO. Defaults to parallel data input on power-up.<br>Parallel data input has internal pulldown to EP.<br>GPIO_ has an open-drain output with internal 60kΩ pullup to IOVDD. See register table for programming details. |
| 13 | DIN18/HS | Parallel Data Input/Horizontal Sync with Internal Pulldown to EP. Defaults to parallel data input on power-up.<br>Horizontal sync input when VS/HS encoding is enabled (Table 2). |
| 14 | DIN19/VS | Parallel Data Input/Vertical Sync with Internal Pulldown to EP. Defaults to parallel data input on power-up.<br>Vertical sync input when VS/HS encoding is enabled (Table 2). |

## Pin Description (continued)

| PIN | NAME | FUNCTION |
|---|---|---|
| 15, 39 | IOVDD | I/O Supply Voltage. 1.8V to 3.3V logic I/O power supply. Bypass IOVDD to EP with 0.1µF and 0.001µF capacitors as close as possible to the device with the smallest value capacitor closest to IOVDD. |
| 18 | GPO | General-Purpose Output. GPO follows the GMSL deserializer GPI (or INT) input. GPO = low upon power-up and when $\overline{PWDN}$ = low. |
| 19 | GPIO1 | Open-Drain, General-Purpose Input/Output with Internal 60kΩ Pullup to IOVDD |
| 20 | MS | Mode-Select Input with Internal Pulldown to EP. Set MS = low to select base mode. Set MS = high to select bypass mode. |
| 21 | $\overline{PWDN}$ | Active-Low, Power-Down Input with Internal Pulldown to EP. Set $\overline{PWDN}$ low to enter power-down mode to reduce power consumption. |
| 22 | DRS | Data-Rate Select Input with Internal Pulldown to EP (Table 15). |
| 23 | CONF0 | Configuration 0. Three-level configuration input (Table 9). |
| 24 | CONF1 | Configuration 1. Three-level configuration input (Table 9). |
| 25 | OUT- | Inverting Coax/Twisted-Pair Serial Output |
| 26 | OUT+ | Noninverting Coax/Twisted-Pair Serial Output |
| 28 | RX/SDA | UART Receive or I²C Serial-Data Input/Output with Internal 30kΩ Pullup to IOVDD. In UART mode, RX/SDA is the Rx input of the serializer's UART. In the I²C mode, RX/SDA is the SDA input/output of the serializer's I²C master/slave. RX/SDA has an open-drain driver and requires a pullup resistor. |
| 29 | TX/SCL | UART Transmit or I²C Serial-Clock Input/Output with Internal 30kΩ Pullup to IOVDD. In UART mode, TX/SCL is the Tx output of the serializer's UART. In the I²C mode, TX/SCL is the SCL input/output of the serializer's I²C master/slave. TX/SCL has an open-drain driver and requires a pullup resistor. |
| 30 | $\overline{AUTOS}$ | Autostart Input with Internal Pulldown to EP. $\overline{AUTOS}$ = low enables serialization upon power-up and automatic frequency range selection of PCLKIN. $\overline{AUTOS}$ = high puts the part in sleep mode upon power-up. |
| 31 | PCLKIN | Parallel Clock Input with Internal Pulldown to EP. Latches parallel data inputs and provides the PLL reference clock. |
| 35 | DVDD | 1.8V Digital Power Supply. Bypass DVDD to EP with 0.1µF and 0.001µF capacitors as close as possible to the device with the smaller value capacitor closest to DVDD. |
| — | EP | Exposed Pad. EP is internally connected to device ground. **MUST** connect EP to the PCB ground plane through an array of vias for proper thermal and electrical performance. |

## Functional Diagram



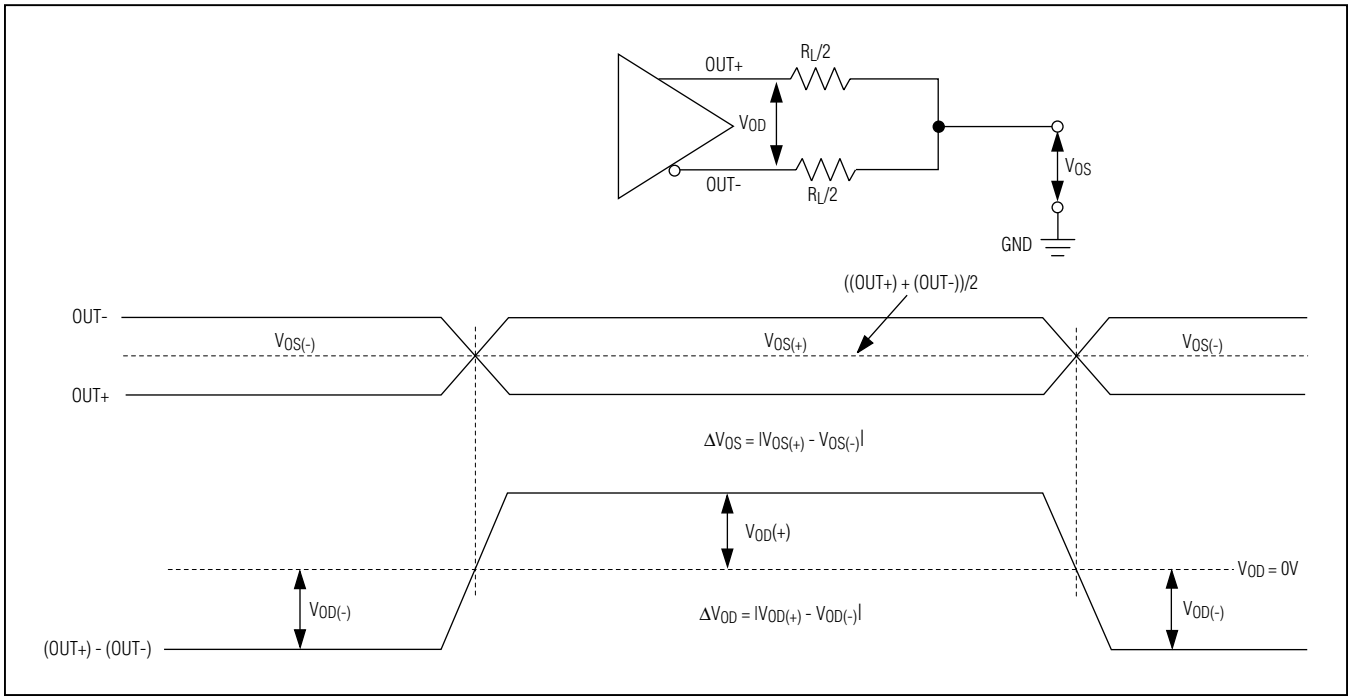



*Figure 1. Serial-Output Parameters*

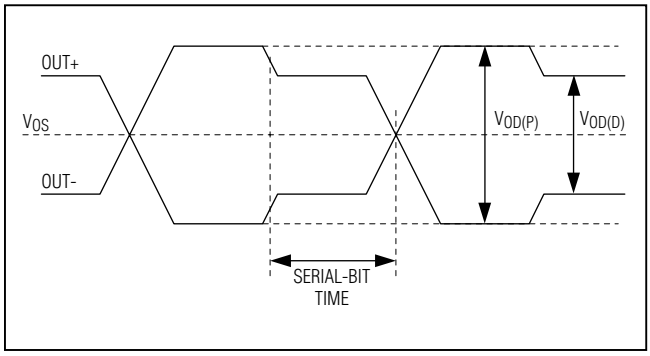



*Figure 2. Output Waveforms at OUT+, OUT-*

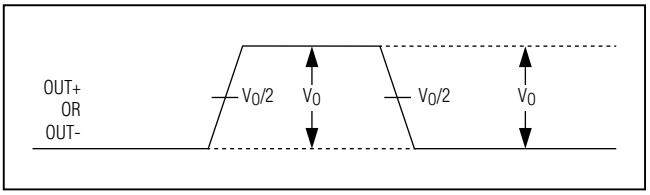



*Figure 3. Single-Ended Output Template*

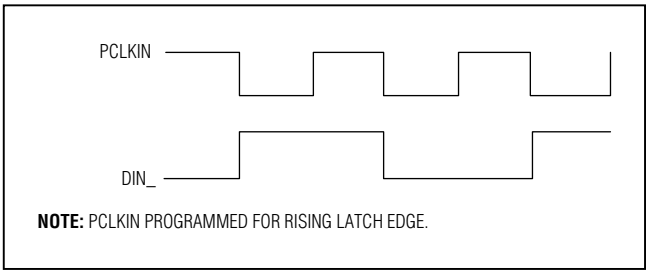



*Figure 4. Worst-Case Pattern Input*

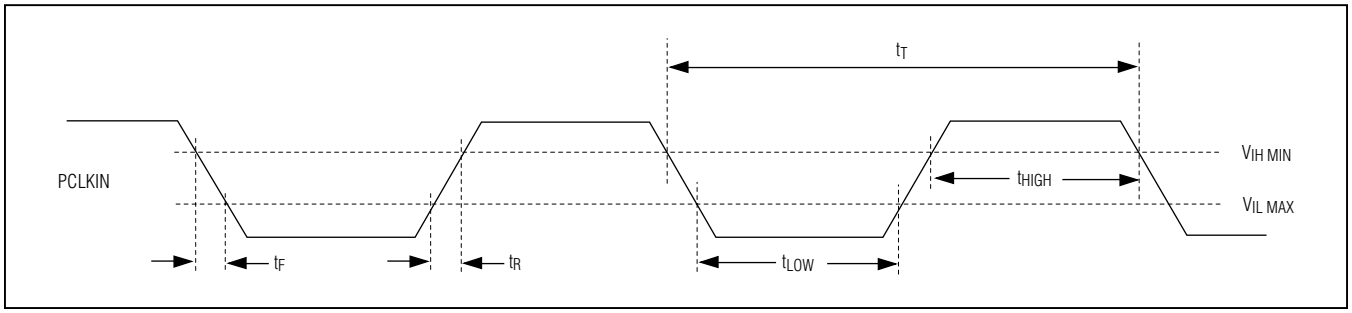



*Figure 5. Parallel Clock Input Requirements*

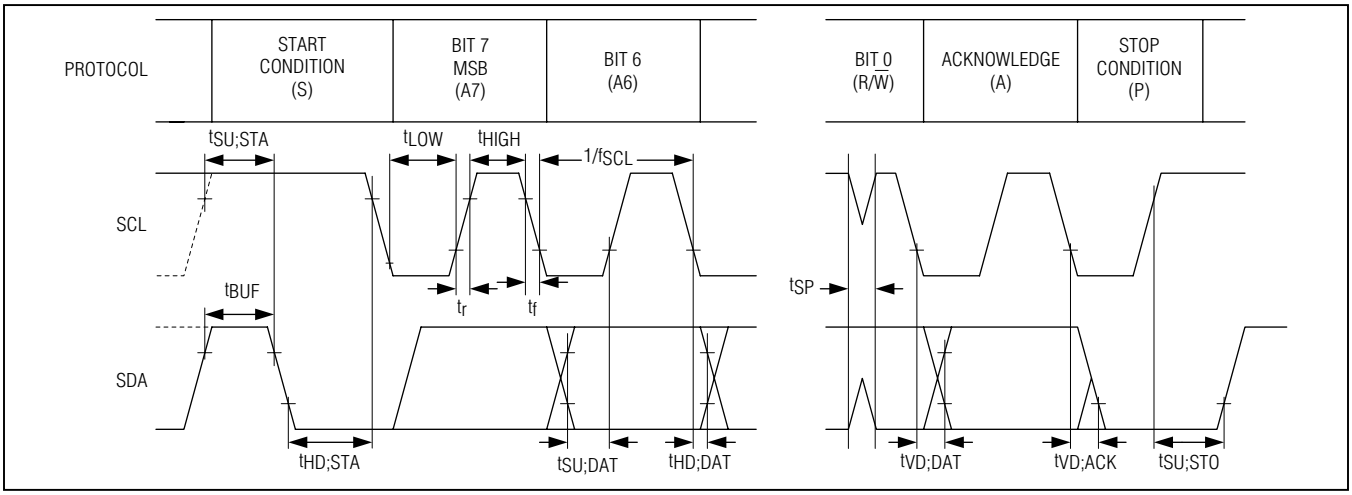



*Figure 6. I²C Timing Parameters*

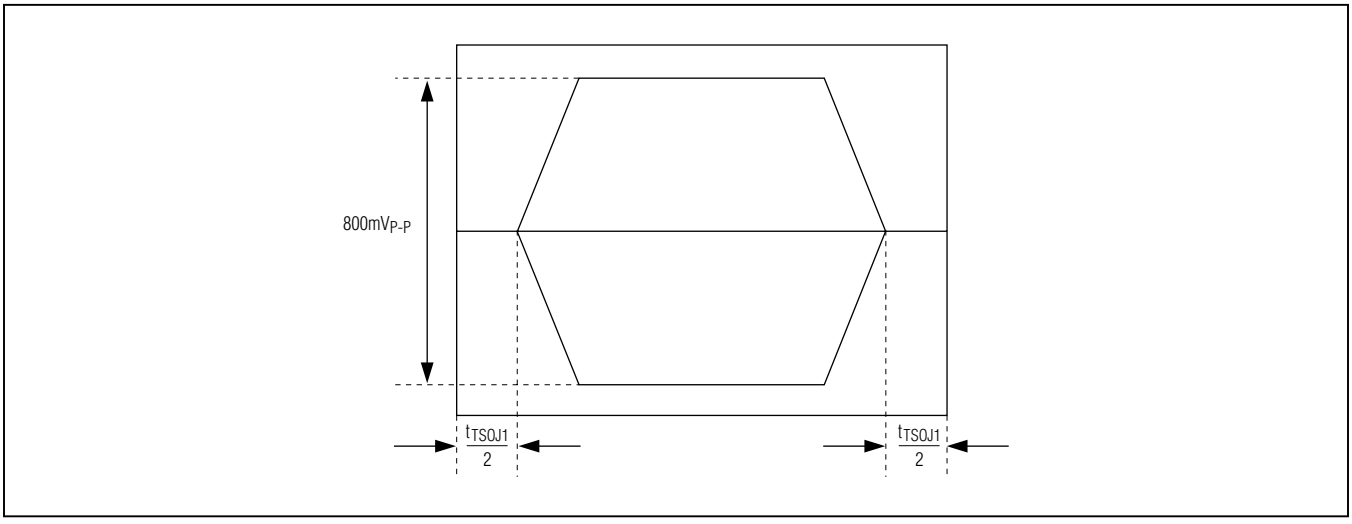



*Figure 7. Differential Output Template*

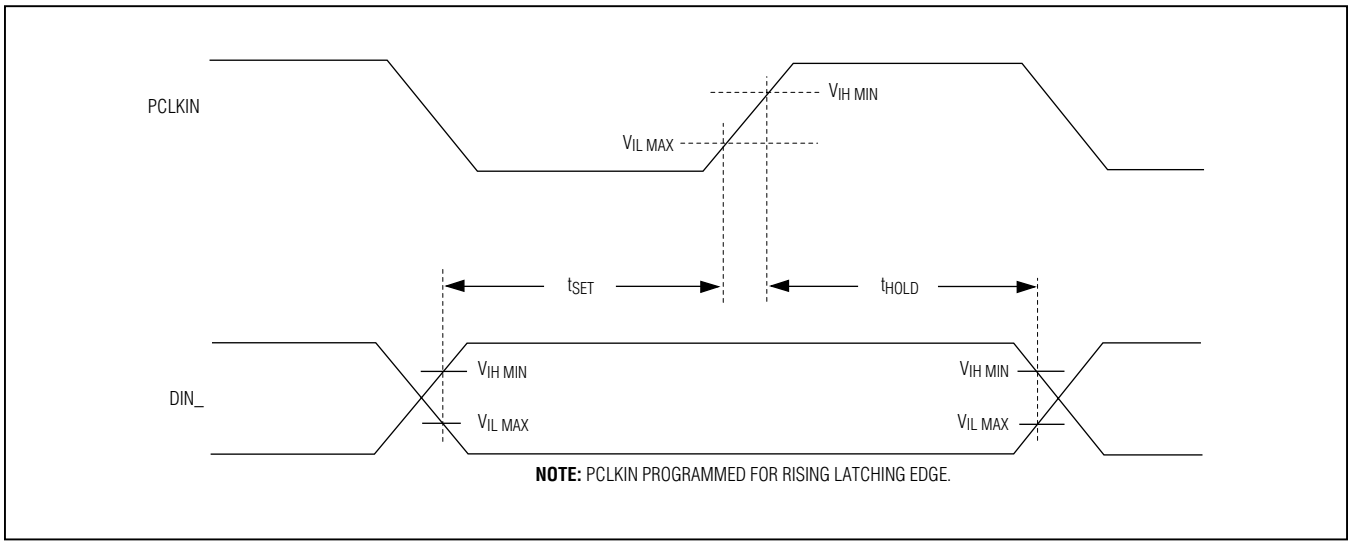



*Figure 8. Input Setup and Hold Times*

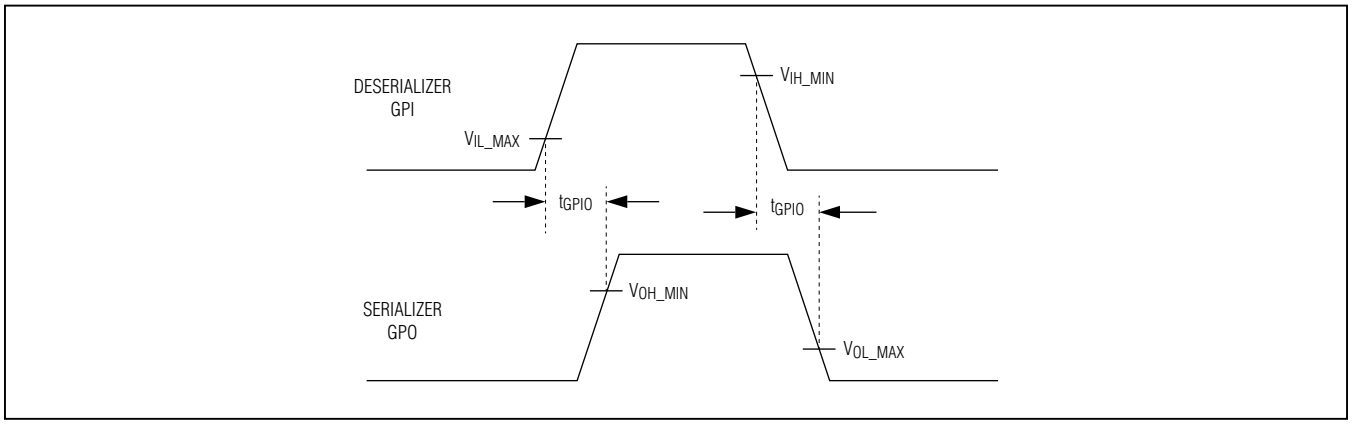



*Figure 9. GPI-to-GPO Delay*

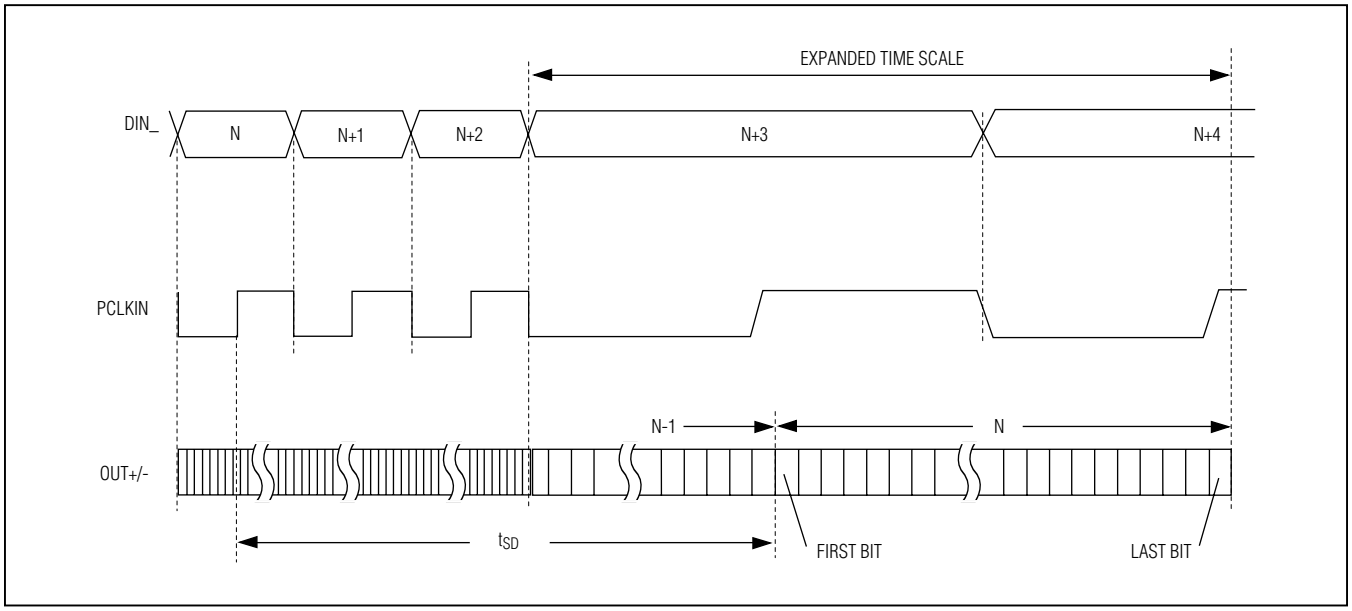



*Figure 10. Serializer Delay*

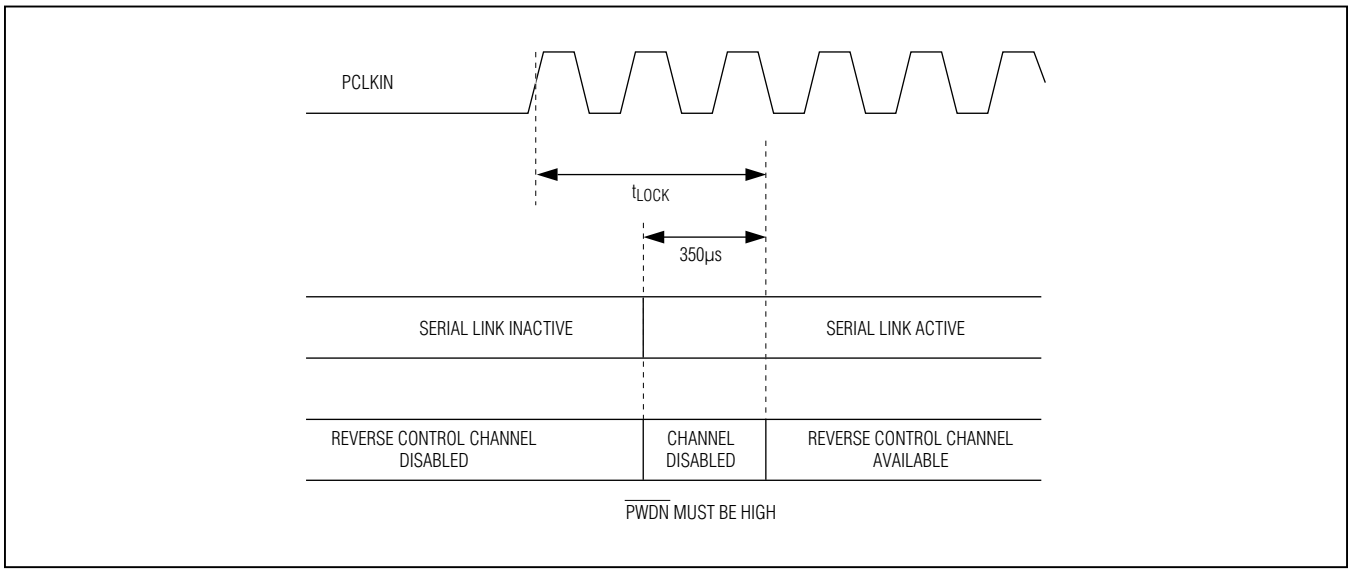



*Figure 11. Link Startup Time*

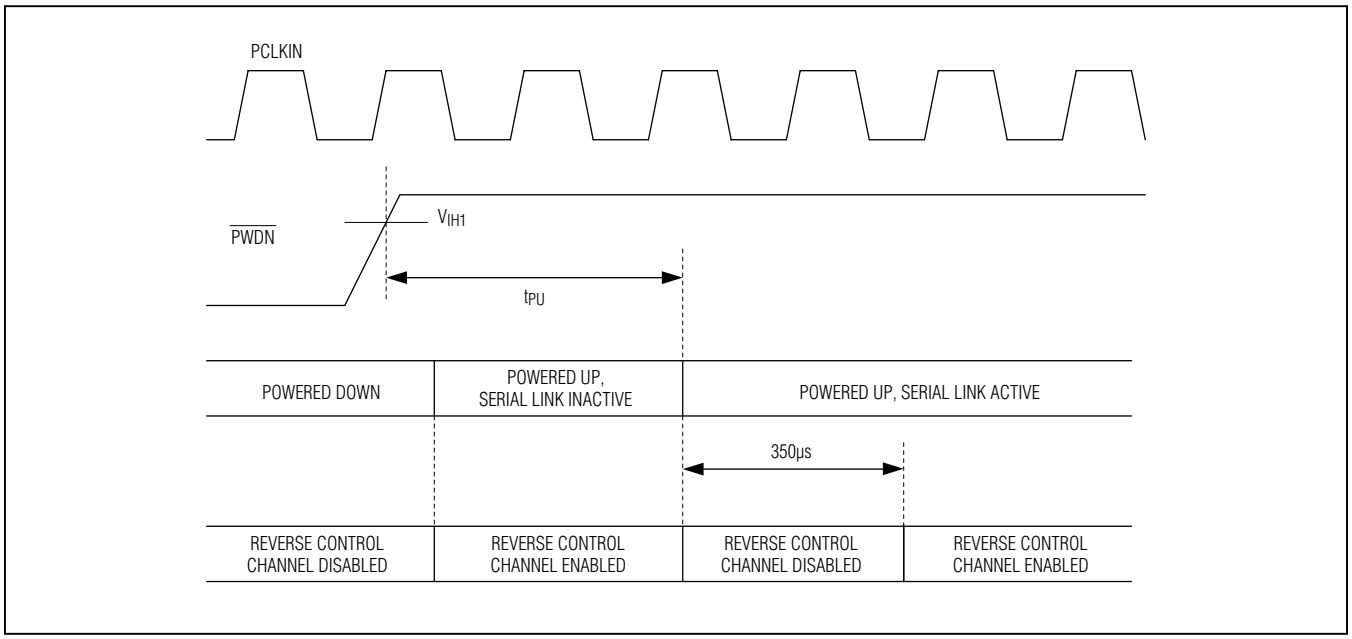



*Figure 12. Power-Up Delay*

## Detailed Description

The MAX9273 serializer, when paired with the MAX9272 deserializer, provides the full set of operating features, but offers basic functionality when paired with any GMSL deserializer.

The serializer has a maximum serial-bit rate of 1.5Gbps for 15m or more of cable and operates up to a maximum input clock of 50MHz in 22-bit, single-input mode, or 75MHz/100MHz in 15-bit/11-bit, double-input mode, respectively. Pre/deemphasis, along with the GMSL deserializer channel equalizer, extends the link length and enhances link reliability.

The control channel enables a µC to program serializer and deserializer registers and program registers on peripherals. The µC can be located at either end of the link, or at both ends. Two modes of control-channel operation are available with associated protocols and data formats. Base mode uses either I²C or GMSL UART, while bypass mode uses a user-defined UART.

Spread spectrum is available to reduce EMI on the serial output. The serial output complies with ISO 10605 and IEC 61000-4-2 ESD protection standards.

### Register Mapping

Registers set the operating conditions of the serializer and are programmed using the control channel in base mode. The serializer holds its device address and the device address of the deserializer it is driving. Similarly, the driven deserializer holds its device address and the address of the serializer by which it is driven. Whenever a device address is changed, be sure to write the new address to both devices. The default device address of the MAX9273 serializer (or any GMSL serializer) is 0x80 and the default device address of any GMSL deserializer is 0x90 (Table 1). Registers 0x00 and 0x01 in both devices hold the device addresses.

### Input Bit Map

The parallel input functioning and width depends on settings of the double-/single-input mode (DBL), HS/VS encoding (HVEN), error correction (EDC), and bus width (BWS). DINA are the inputs latched by the pixel clock in single-input mode, or the inputs latched on the first pixel clock in double-input mode. DINB are the inputs latched on the second pixel clock in double-input mode. Table 2 lists the bit map for the control pin settings.

## Table 1. Power-Up Default Register Map (see Table 15)

| REGISTER ADDRESS (hex) | POWER-UP DEFAULT (hex) | POWER-UP DEFAULT SETTINGS (MSB FIRST) |
|---|---|---|
| 0x00 | 0x80 | SERID = 1000000, serializer device address<br>CFGBLOCK = 0, registers 0x00 to 0x1F are read/write |
| 0x01 | 0x90 | DESID = 1001000, deserializer device address<br>RESERVED = 0 |
| 0x02 | 0x1F | SS = 000, no spread spectrum<br>RESERVED = 1<br>PRNG = 11, automatically detect the pixel clock range<br>SRNG = 11, automatically detect serial-data rate |
| 0x03 | 0x00 | AUTOFM = 00, calibrate spread-modulation rate only once after locking<br>SDIV = 000000, auto calibrate sawtooth divider |
| 0x04 | 0x07, 0x87 | SEREN = 0 ($\overline{AUTOS}$ = high), SEREN = 1($\overline{AUTOS}$ = low), serial link enable default depends on $\overline{AUTOS}$ pin state at power-up<br>CLINKEN = 0, configuration link disabled<br>PRBSEN = 0, PRBS test disabled<br>SLEEP = 0, sleep mode disabled (see the *Link Startup Procedure* section)<br>INTTYPE = 01, local control channel uses UART<br>REVCCEN = 1, reverse control channel active (receiving)<br>FWDCCEN = 1, forward control channel active (sending) |
| 0x05 | 0x01 | I2CMETHOD = 0, I²C packets include register address<br>ENJITFILT = 0, jitter filter disabled<br>PRBSLEN = 00, continuous PRBS length<br>RESERVED = 00<br>ENWAKEN = 0, OUT- wake-up receiver disabled<br>ENWAKEP = 1, OUT+ wake-up receiver enabled |
| 0x06 | 0x80, 0xA0 | CMLLVL = 1000 or 1010, output level determined by the state of CONF1, CONF0 at power-up<br>PREEMP = 0000, preemphasis disabled |
| 0x07 | 0x00, 0x10 | DBL = 0, double-input mode<br>DRS = 0, high data-rate mode<br>BWS = 0, 24-bit mode<br>ES = 0 or 1, edge-select input setting determined by the state of CONF1, CONF0 at startup<br>RESERVED = 0<br>HVEN = 0, HS/VS encoding disabled<br>EDC = 00, 1-bit parity error detection |
| 0x08 | 0x00 | INVVS = 0, serializer does not invert VSYNC<br>INVHS = 0, serializer does not invert HSYNC<br>RESERVED = 000000 |
| 0x09 | 0x00 | I2CSRCA = 0000000, I²C address translator source A is 0x00<br>RESERVED = 0 |

**Table 1. Power-Up Default Register Map (see Table 15) (continued)**

| REGISTER ADDRESS (hex) | POWER-UP DEFAULT (hex) | POWER-UP DEFAULT SETTINGS (MSB FIRST) |
|---|---|---|
| 0x0A | 0x00 | I2CDSTA = 0000000, I²C address translator destination A is 0x00<br>RESERVED = 0 |
| 0x0B | 0x00 | I2CSRCB = 0000000, I²C address translator source B is 0x00<br>RESERVED = 0 |
| 0x0C | 0x00 | I2CDSTB = 0000000, I²C address translator destination B is 0x00<br>RESERVED = 0 |
| 0x0D | 0xB6 | I2CLOCACK = 1, acknowledge generated when forward channel is not available<br>I2CSLVSH = 01, 469ns/234ns I²C setup/hold time<br>I2CMSTBT = 101, 339kbps (typ) I²C-to-I²C master bit-rate setting<br>I2CSLVTO = 10, 1024µs (typ) I²C-to-I²C slave remote timeout |
| 0x0E | 0x42 | DIS_REV_P = 0, OUT+ reverse channel receiver enabled<br>DIS_REV_N = 1, OUT- reverse channel receiver disabled<br>GPIO5EN = 0, GPIO5 disabled<br>GPIO4EN = 0, GPIO4 disabled<br>GPIO3EN = 0, GPIO3 disabled<br>GPIO2EN = 0, GPIO2 disabled<br>GPIO1EN = 1, GPIO1 enabled<br>RESERVED = 0 |
| 0x0F | 0xFE | RESERVED = 11<br>GPIO5OUT = 1, GPIO5 set high<br>GPIO4OUT = 1, GPIO4 set high<br>GPIO3OUT = 1, GPIO3 set high<br>GPIO2OUT = 1, GPIO2 set high<br>GPIO1OUT = 1, GPIO1 set high<br>SETGPO = 0, GPO set low |
| 0x10 | 0x3E | RESERVED = 00<br>GPIO5IN = 1, GPIO5 is input high<br>GPIO4IN = 1, GPIO4 is input high<br>GPIO3IN = 1, GPIO3 is input high<br>GPIO2IN = 1, GPIO2 is input high<br>GPIO1IN = 1, GPIO1 is input high<br>GPO_L = 0, GPO set low |
| 0x11 | 0x00 | ERRGRATE = 00, generate an error every 2560 bits<br>ERRGTYPE = 0, generate single-bit errors<br>ERRGCNT = 00, continuously generate errors<br>ERRGPER = 0, disable periodic error generation<br>ERRGEN = 0, disable error generation |
| 0x12 | 0x40 | RESERVED = 01000000 |
| 0x13 | 0x22 | RESERVED = 00100010 |
| 0x14 | 0xXX | RESERVED = XXXXXXXX |

## Table 1. Power-Up Default Register Map (see Table 15) (continued)

| REGISTER ADDRESS (hex) | POWER-UP DEFAULT (hex) | POWER-UP DEFAULT SETTINGS (MSB FIRST) |
|---|---|---|
| 0x15 | 0x00 | CXTP = 0, CXTP is low<br>I2CSEL = 0, input is low<br>LCCEN = 0, local control channel disabled<br>RESERVED = 000<br>OUTPUTEN = 0, output disabled<br>PCLKDET = 0, no valid PCLKIN detected |
| 0x16 | 0xXX (read only) | RESERVED = XXXXXXXX |
| 0x17 | 0xXX (read only) | RESERVED = XXXXXXXX |
| 0x1E | 0x0B (read only) | ID = 00001011, device ID is 0x0B |
| 0x1F | 0x0X (read only) | RESERVED = 000<br>CAPS = 0, serializer is not HDCP capable<br>REVISION = XXXX, revision number |

*X = Don't care.*

## Table 2. Input Map

| EDC | BWS | DBL | HVEN | DINA | DINB* | SERIAL LINK WORD BITS |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0:21 | — | 0:21 |
| 0 | 0 | 0 | 1 | 0:17, 20:21, HS, VS | — | 0:17, 20:21 |
| 0 | 0 | 1 | 0 | 0:10 | 0:10 | 0:21 |
| 0 | 0 | 1 | 1 | 0:10, HS, VS | 0:10, HS, VS | 0:21 |
| 0 | 1 | 0 | 0 | 0:21 | — | 0:21 |
| 0 | 1 | 0 | 1 | 0:17, 20:21, HS, VS | — | 0:17, 20:21 |
| 0 | 1 | 1 | 0 | 0:14 | 0:14 | 0:29 |
| 0 | 1 | 1 | 1 | 0:14, HS, VS | 0:14, HS, VS | 0:29 |
| 1 | 0 | 0 | 0 | 0:15 | — | 0:15 |
| 1 | 0 | 0 | 1 | 0:15, HS, VS | — | 0:15 |
| 1 | 0 | 1 | 0 | 0:7 | 0:7 | 0:15 |
| 1 | 0 | 1 | 1 | 0:7, HS, VS | 0:7, HS, VS | 0:15 |
| 1 | 1 | 0 | 0 | 0:21 | — | 0:21 |
| 1 | 1 | 0 | 1 | 0:17, 20:21, HS, VS | — | 0:17, 20:21 |
| 1 | 1 | 1 | 0 | 0:11 | 0:11, HS, VS | 0:23 |
| 1 | 1 | 1 | 1 | 0:11, HS, VS | 0:11, HS, VS | 0:23 |

**In double-input mode (DBL = 1), DINA are latched on the first cycle of PCLKIN and DINB are latched on the second cycle of PCLKIN.*

The parallel input has two input modes: single- and double-rate input. In single-input mode, LATCH A stores data from DIN_ every PCLKIN cycle (Figure 13). Parallel data from LATCH A is then sent to the scrambler for serialization (Figure 14). The device accepts pixel clocks from 6.25MHz to 50MHz.

In double-input mode, LATCH B stores two input words (Figure 15). Data from LATCH B is sent to the scrambler as a combined word. The MAX9272 deserializer outputs the combined word (single-output mode) or two half-sized words (double-output mode). The serializer/deserializer use pixel clock rates from 33.3MHz to 100MHz for 11-bit, double-input mode and 25MHz to 75MHz for 15-bit, double-input mode. See Figure 16 for timing details.

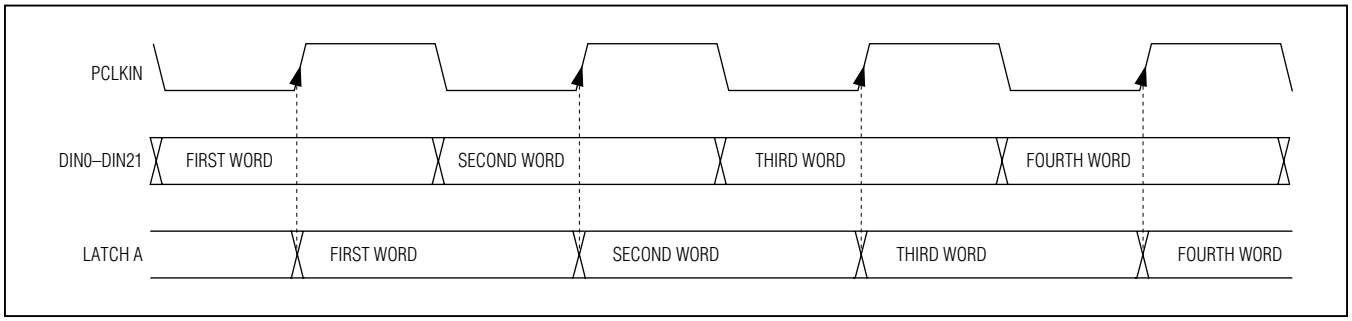



*Figure 13. Single-Input Waveform (Latch on Rising Edge of PCLKIN Selected)*

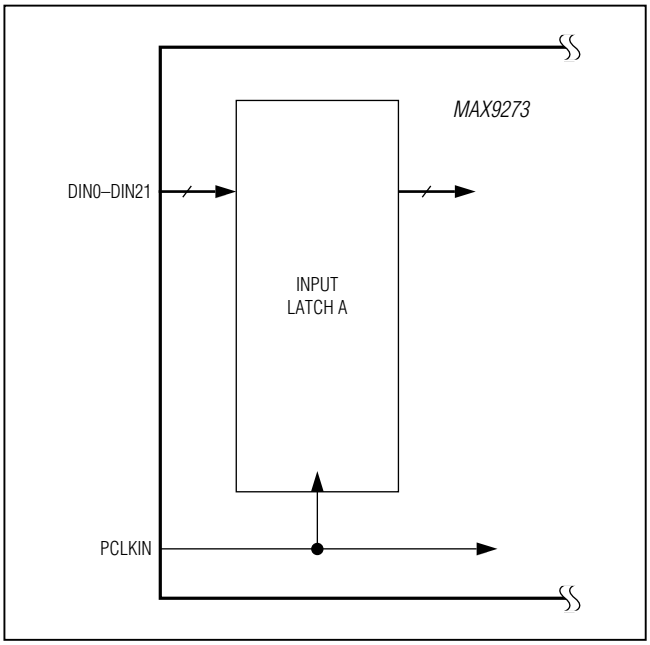



*Figure 14. Single-Input Function Block*

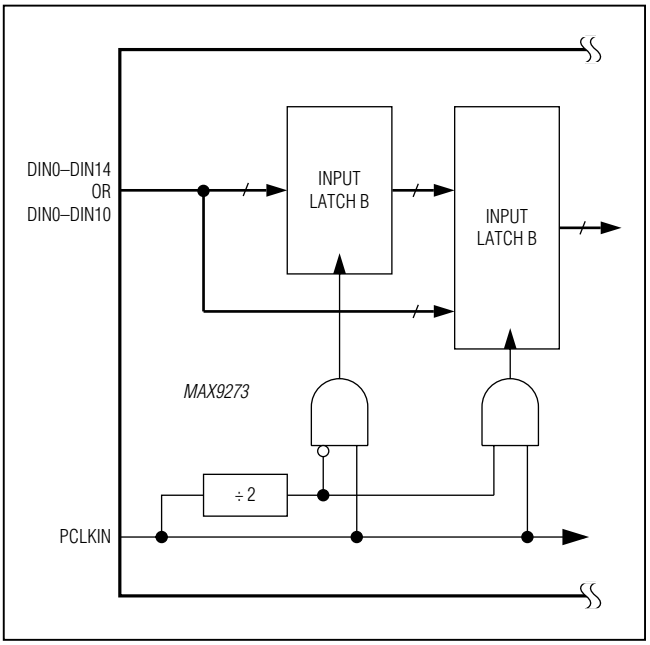



*Figure 15. Double-Input Function Block*

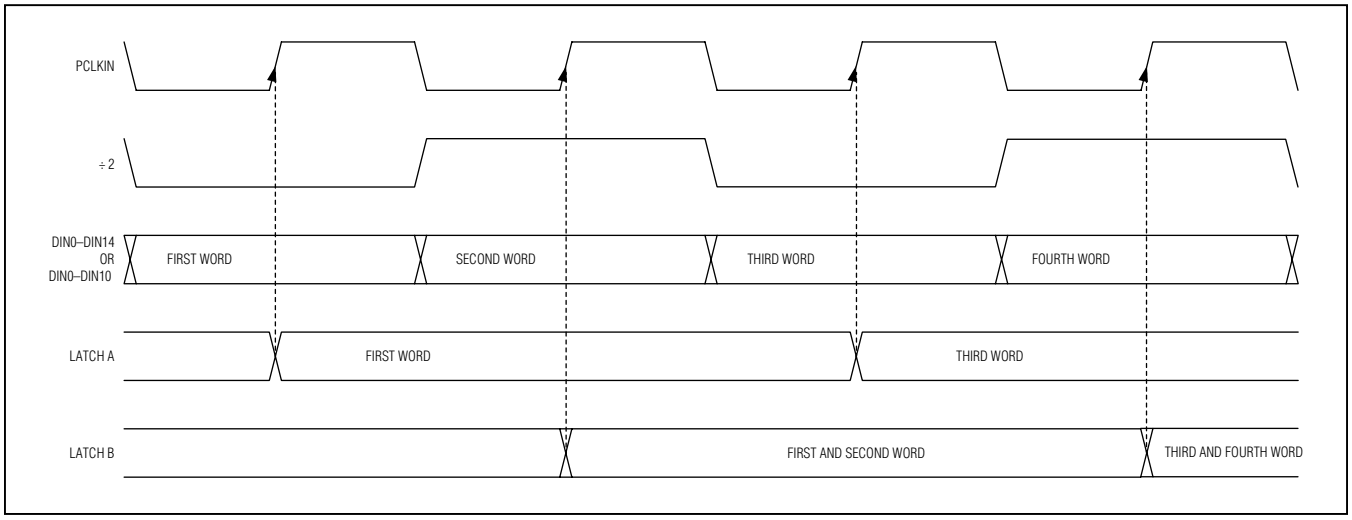



*Figure 16. Double-Input Waveform (Latch on Rising Edge of PCLKIN Selected)*

### Serial Link Signaling and Data Format

The serializer uses differential CML signaling to drive twisted-pair cable and single-ended CML to drive coaxial cable. The output amplitude is programmable.

Input data is scrambled and then 8b/10b coded. The deserializer recovers the embedded serial clock, then samples, decodes, and descrambles the data. In 24-bit or 32-bit mode, 22 or 30 bits contain the video data and/or error correction bits, if used. The 23rd or 31st bit carries the forward control-channel data. The last bit is the parity bit of the previous 23 or 31 bits (Figure 17).

### Reverse Control Channel

The serializer uses the reverse control channel to receive I²C/UART and GPO signals from the deserializer in the opposite direction of the video stream. The reverse control channel and forward video data coexist on the same serial cable forming a bidirectional link. The reverse control channel operates independently from the forward control channel. The reverse control channel is available 2ms after power-up. The serializer temporarily disables the reverse control channel for 350µs after starting/stopping the forward serial link.

### Data-Rate Selection

The serializer/deserializer use DRS, DBL, and BWS to set the PCLKIN frequency range (Table 3). Set DRS = 1 for a PCLKIN frequency range of 6.25MHz to 12.5MHz (32-bit, single-input mode) or 8.33MHz to 16.66MHz (24-bit, single-input mode). Set DRS = 0 for normal operation. It is not recommended to use double-input mode when DRS = 1.

### Control Channel and Register Programming

The control channel is available for the µC to send and receive control data over the serial link simultaneously with the high-speed data. The µC controls the link from either the serializer or deserializer side. The control channel between the µC and serializer or deserializer runs in base mode or bypass mode, according to the mode-selection (MS) input of the device connected to the µC. Base mode is a half-duplex control channel and bypass mode is a full-duplex control channel.

### UART Interface

In base mode, the µC is the host and can access the registers of both the serializer and deserializer from either side of the link using the GMSL UART protocol. The µC can also program the peripherals on the remote side by sending the UART packets to the serializer or deserializer, with the UART packets converted to I²C by the device on the remote side of the link. The µC communicates with a UART peripheral in base mode (through INTTYPE register settings), using the half-duplex default GMSL UART protocol of the serializer/deserializer. The device addresses of the serializer/deserializer in base mode are programmable. The default value is 0x80 for the serializer and 0x90 for the deserializer.

When the peripheral interface is I²C, the serializer/deserializer convert UART packets to I²C that have device addresses different from those of the serializer or deserializer. The converted I²C bit rate is the same as the original UART bit rate.

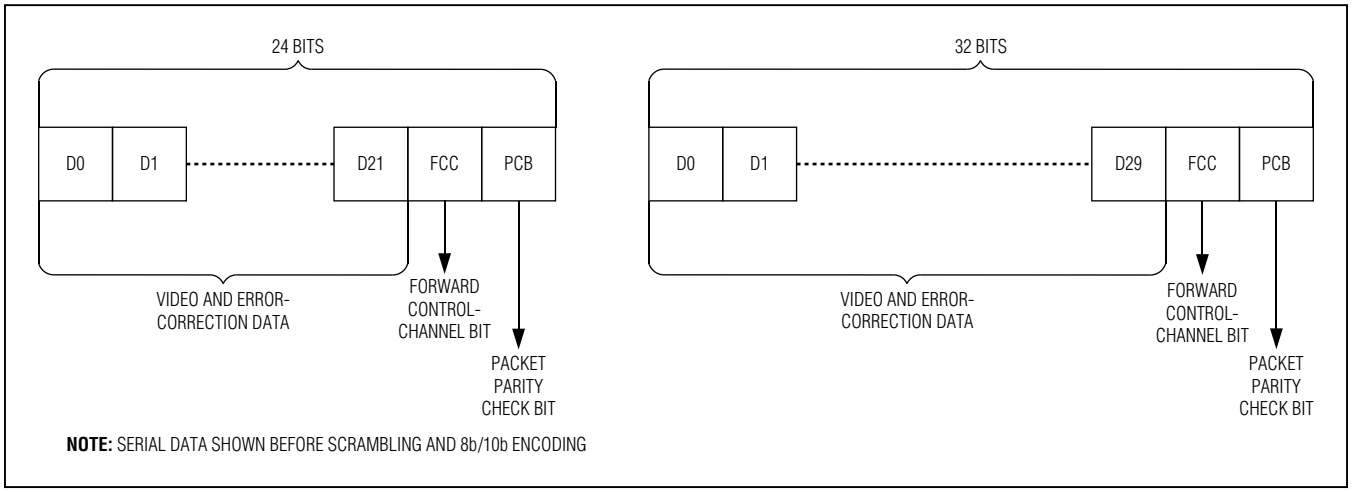



*Figure 17. Serial-Data Format*

## Table 3. Data-Rate Selection Table

| DRS SETTING | DBL SETTING | BWS SETTING | PCLKIN RANGE (MHz) |
|---|---|---|---|
| 0 | 0 (single input) | 0 (24-bit mode) | 16.66 to 50 |
| 0 | 0 | 1 (32-bit mode) | 12.5 to 35 |
| 0 | 1 (double input) | 0 | 33.3 to 100 |
| 0 | 1 | 1 | 25 to 75 |
| 1 | 0 | 0 | 8.33 to 16.66 |
| 1 | 0 | 1 | 6.25 to 12.5 |
| 1 | 1 | 0 | Do not use |
| 1 | 1 | 1 | Do not use |

The deserializer uses differential line coding to send signals over the reverse channel to the serializer. The bit rate of the control channel is 9.6kbps to 1Mbps in both directions. The serializer/deserializer automatically detect the control-channel bit rate in base mode. Packet bit-rate changes can be made in steps of up to 3.5 times higher or lower than the previous bit rate. See the *Changing the Clock Frequency* section for more information on changing the control-channel bit rate.

Figure 19 shows the UART data format. Figure 20 and Figure 21 detail the formats of the SYNC byte (0x79) and the ACK byte (0xC3). The µC and the connected slave chip generate the SYNC byte and ACK byte, respectively. Events such as device wake-up and GPI generate transitions on the control channel that can be ignored by the µC. Data written to the serializer/deserializer registers do not take effect until after the acknowledge byte is sent. This allows the µC to verify that write commands are received without error, even if the result of the write command directly affects the serial link. The slave uses the SYNC byte to synchronize with the host UART's data rate. If the GPI or MS/HVEN inputs of the deserializer toggle while there is control-channel communication, or if a line fault occurs, the control-channel communication is corrupted. In the event of a missed or delayed acknowledge (~1ms due to control-channel timeout), the µC should assume there was an error in the packet when the slave device received it, or that an error occurred during the response from the slave device. In base mode, the µC must keep the UART Tx/Rx lines high for 16 bit times before starting to send a new packet.

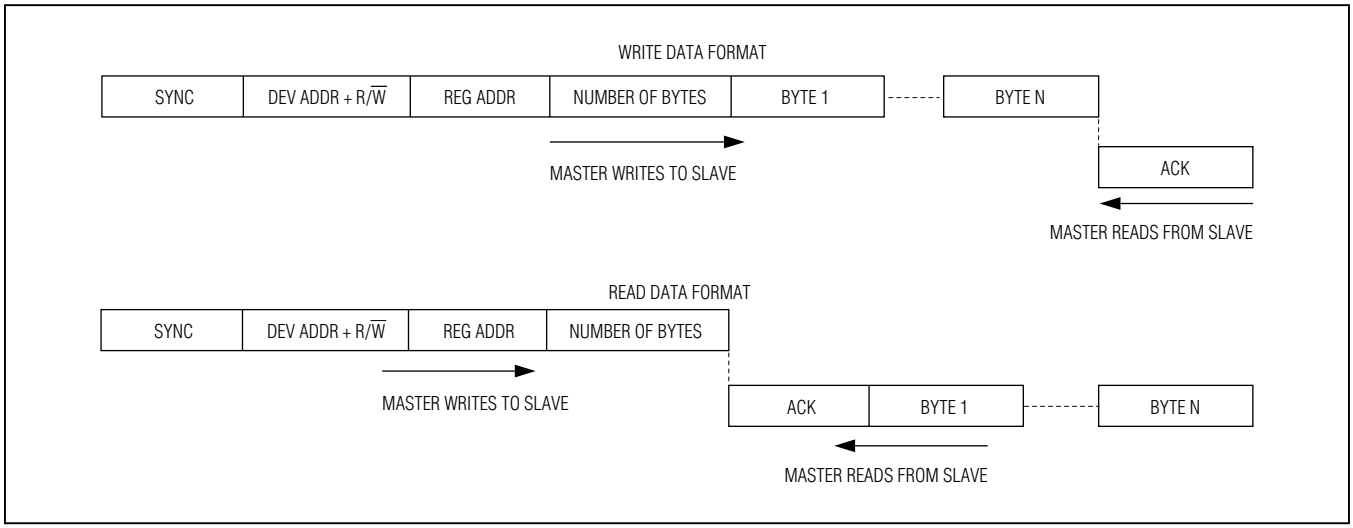



*Figure 18. GMSL UART Protocol for Base Mode*

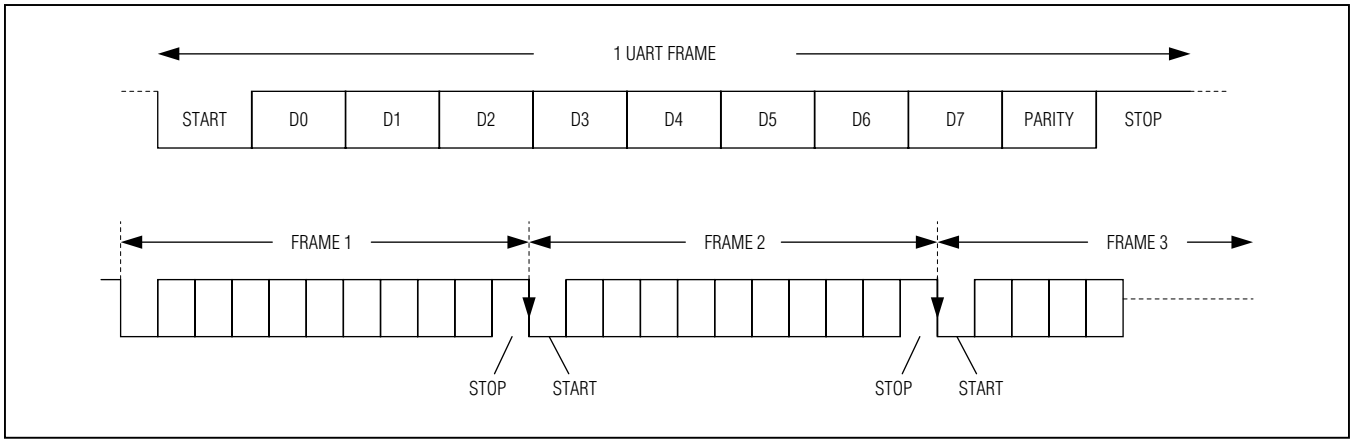



*Figure 19. GMSL UART Data Format for Base Mode*

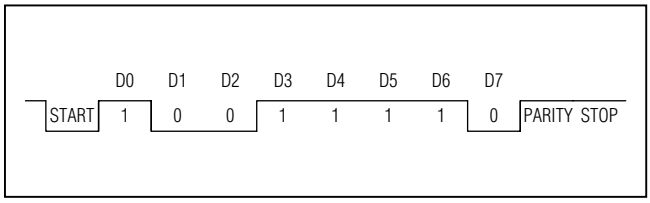



*Figure 20. SYNC Byte (0x79)*

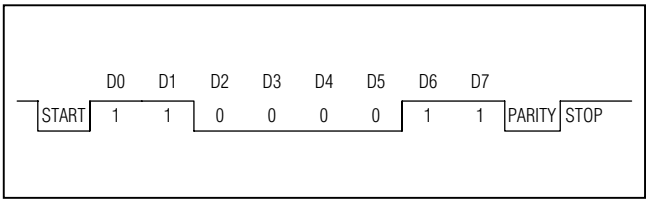



*Figure 21. ACK Byte (0xC3)*

As shown in Figure 22, the remote-side device converts packets going to or coming from the peripherals from UART format to I²C format and vice versa. The remote device removes the byte number count and adds or receives the ACK between the data bytes of I²C. The I²C bit rate is the same as the UART bit rate.

### *Interfacing Command-Byte-Only I²C Devices with UART*

The serializer/deserializer UART-to-I²C conversion can interface with devices that do not require register addresses, such as the MAX7324 GPIO expander. In this mode, the I²C master ignores the register address byte and directly reads/writes the subsequent data bytes (Figure 23). Change the communication method of the I²C master using the I2CMETHOD bit. I2CMETHOD = 1 sets command-byte-only mode, while I2CMETHOD = 0 sets normal mode where the first byte in the data stream is the register address.

### *UART Bypass Mode*

In bypass mode, the serializer/deserializer ignore UART commands from the µC and the µC communicates with the peripherals directly using its own defined UART protocol. The µC cannot access the serializer/deserializer registers in this mode. Peripherals accessed through the forward control channel using the UART interface need to handle at least one PCLKIN period ± 10ns of jitter due to the asynchronous sampling of the UART signal by PCLKIN. Set MS = high to put the control channel into bypass mode. For applications with the µC connected to the deserializer, there is a 1ms wait time between setting MS high and the bypass control channel being active. There is no delay time when switching to bypass mode when the µC is connected to the serializer. Do not send a logic-low value longer than 100µs to ensure proper GPO functionality. Bypass mode accepts bit rates down to 10kbps in either direction. See the *GPO/GPI Control* section for GPO functionality limitations. The control-channel data pattern should not be held low longer than 100µs if GPO control is used.

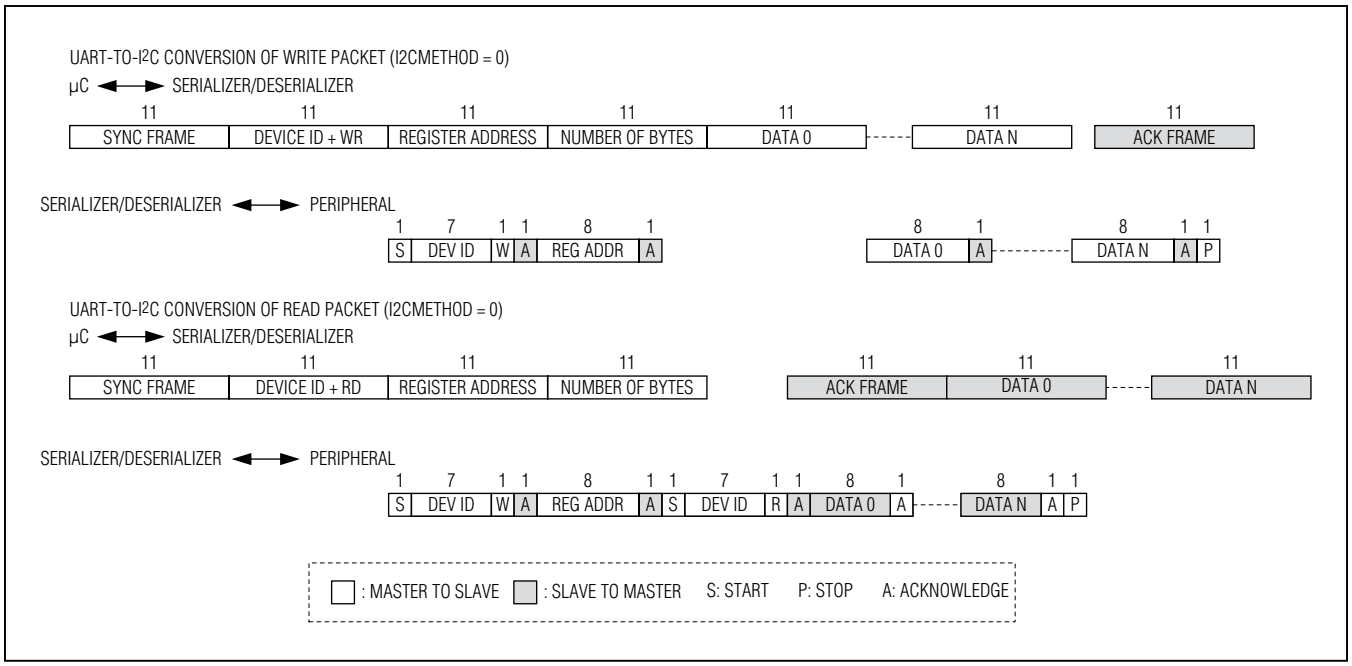



*Figure 22. Format Conversion Between GMSL UART and I²C with Register Address (I2CMETHOD = 0)*

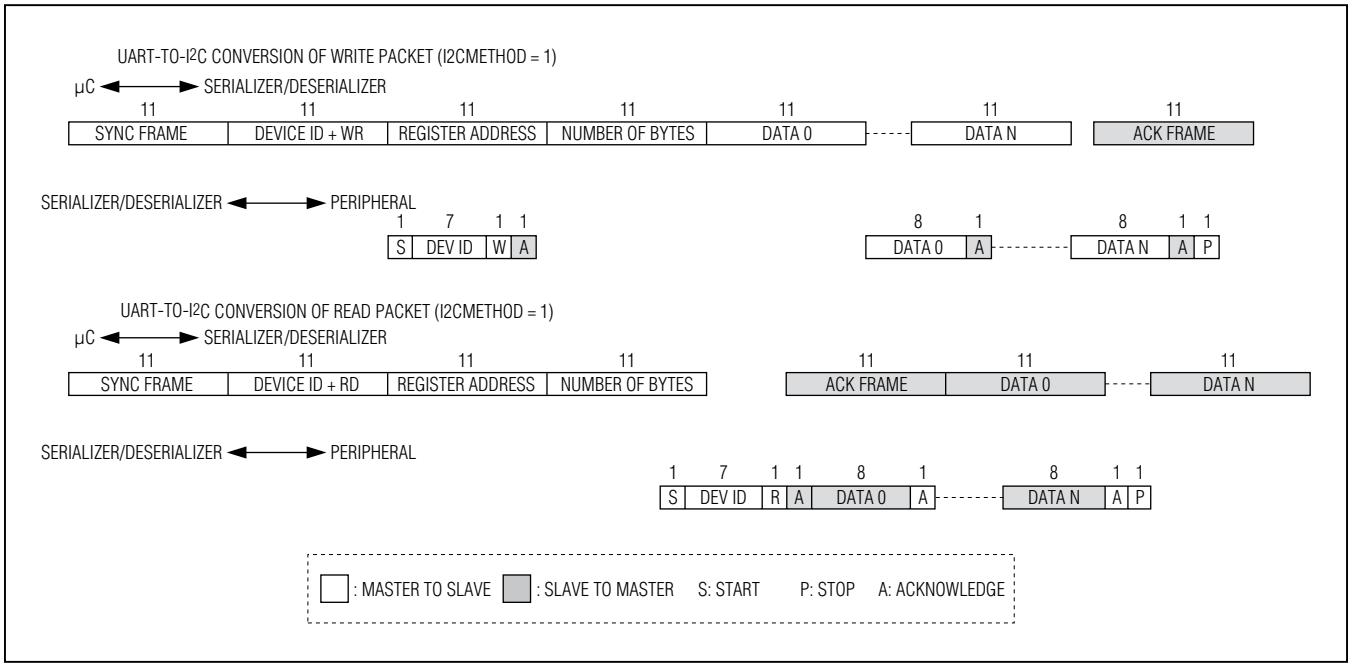



*Figure 23. Format Conversion Between GMSL UART and I²C with Register Address (I2CMETHOD = 1)*

### I²C Interface

In I²C-to-I²C mode, the serializer control-channel interface sends and receives data through an I²C-compatible 2-wire interface. The interface uses a serial-data line (SDA) and a serial-clock line (SCL) to achieve bidirectional communication between master and slave(s). A µC master initiates all data transfers to and from the device and generates the SCL clock that synchronizes the data transfer. When an I²C transaction starts on the local-side device's control-channel port, the remote-side device's control-channel port becomes an I²C master that interfaces with remote-side I²C peripherals. The I²C master must accept clock stretching that is imposed by the serializer (holding SCL low). The SDA and SCL lines operate as both an input and an open-drain output. Pullup resistors are required on SDA and SCL. Each transmission consists of a START condition (Figure 6) sent by a master, followed by the device's 7-bit slave address plus a R/$\overline{W}$ bit, a register address byte, one or more data bytes, and finally a STOP condition.

#### START and STOP Conditions

Both SCL and SDA remain high when the interface is not busy. A master signals the beginning of a transmission with a START (S) condition by transitioning SDA from high to low while SCL is high (Figure 24). When the master has finished communicating with the slave, it issues a STOP (P) condition by transitioning SDA from low to high while SCL is high. The bus is then free for another transmission.

#### Bit Transfer

One data bit is transferred during each clock pulse (Figure 25). The data on SDA must remain stable while SCL is high.

#### Acknowledge

The acknowledge bit is a clocked 9th bit that the recipient uses to handshake receipt of each byte of data (Figure 26). Thus, each byte transferred effectively requires nine bits. The master generates the 9th clock pulse, and the recipient pulls down SDA during the acknowledge clock pulse. The SDA line is stable low during the high period of the clock pulse. When the master is transmitting to the slave device, the slave device generates the acknowledge bit

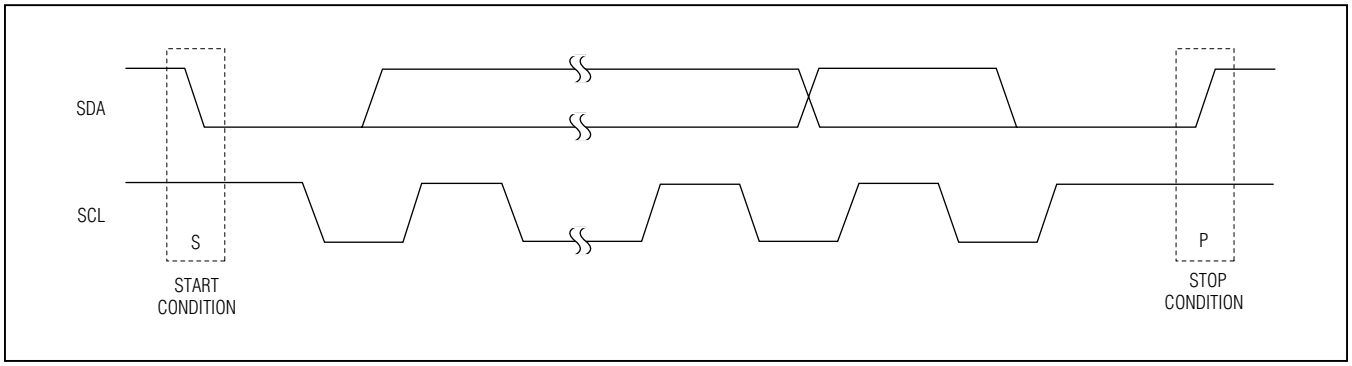



*Figure 24. START and STOP Conditions*

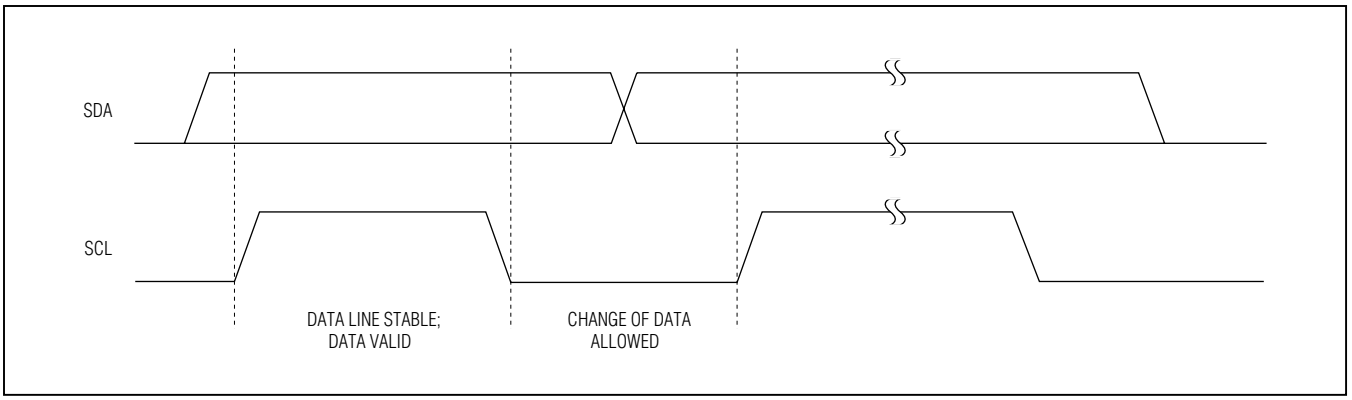



*Figure 25. Bit Transfer*

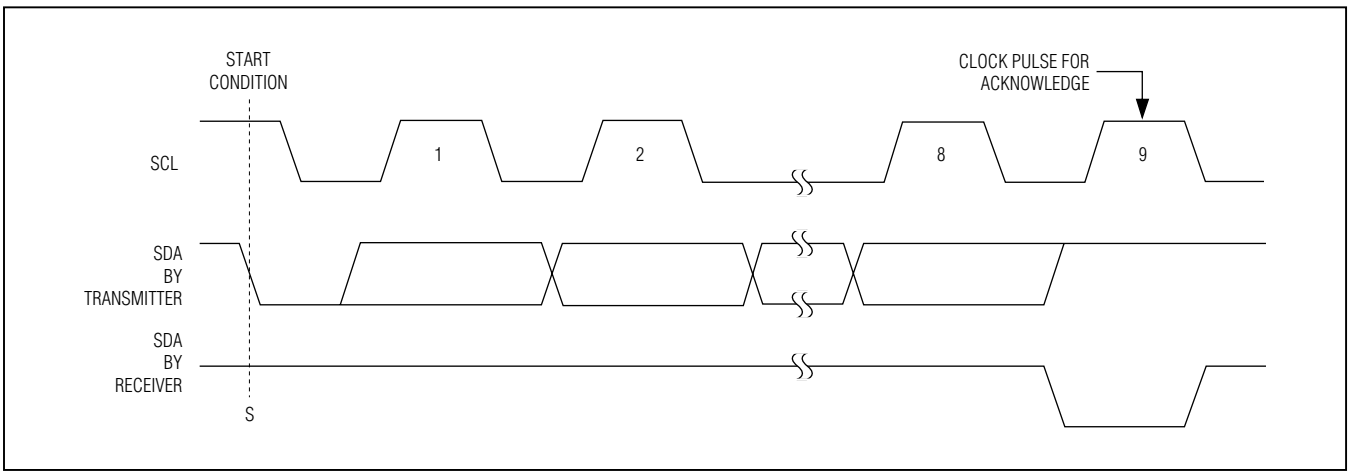



*Figure 26. Acknowledge*

because the slave device is the recipient. When the slave device is transmitting to the master, the master generates the acknowledge bit because the master is the recipient. The device generates an acknowledge even when the forward control channel is not active (not locked). To prevent acknowledge generation when the forward control channel is not active, set the I2CLOCACK bit low.

### Slave Address

The serializer/deserializer have a 7-bit-long slave address. The bit following a 7-bit slave address is the R/$\overline{W}$ bit, which is low for a write command and high for a read command. The slave address is 10000001 for read commands and 10000000 for write commands. See Figure 27.

### Bus Reset

The device resets the bus with the I²C START condition for reads. When the R/$\overline{W}$ bit is set to 1, the serializer/deserializer transmit data to the master, thus the master is reading from the device.

### Format for Writing

A write to the serializer/deserializer comprises the transmission of the slave address with the R/$\overline{W}$ bit set to zero, followed by at least one byte of information. The first byte of information is the register address or command byte. The register address determines which register of the device is to be written by the next byte, if received. If a STOP (P) condition is detected after the register address is received, the device takes no further action

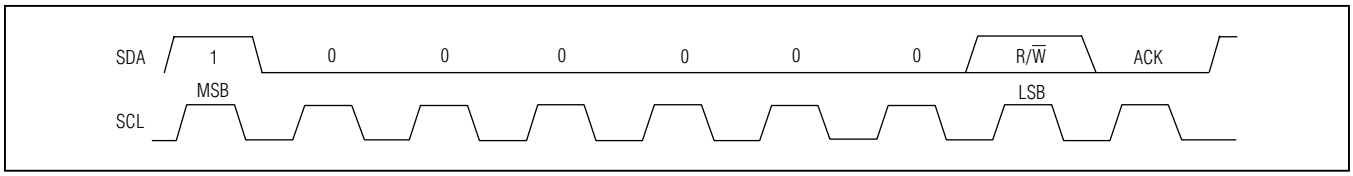



*Figure 27. Slave Address*

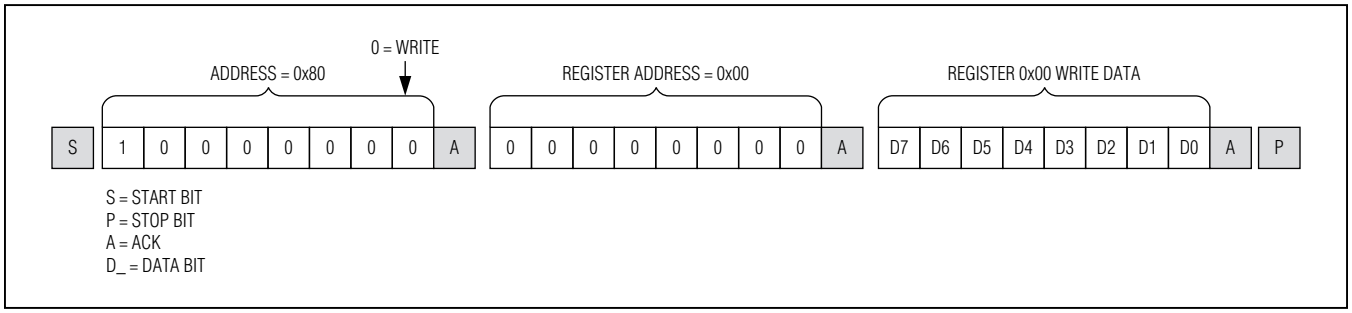



*Figure 28. Format for I²C Write*

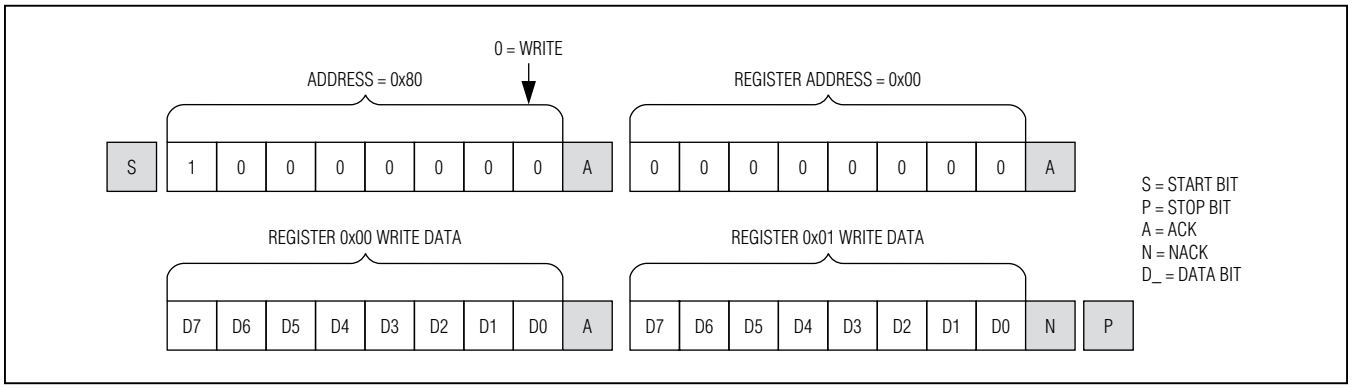



*Figure 29. Format for Write to Multiple Registers*

beyond storing the register address (Figure 28). Any bytes received after the register address are data bytes. The first data byte goes into the register selected by the register address, and subsequent data bytes go into subsequent registers (Figure 29). If multiple data bytes are transmitted before a STOP condition, these bytes are stored in subsequent registers because the register addresses autoincrement.

### *Format for Reading*

The serializer/deserializer are read using the internally stored register address as an address pointer, the same way the stored register address is used as an address pointer for a write. The pointer autoincrements after each data byte is read using the same rules as for a write. Thus, a read is initiated by first configuring the register address by performing a write (Figure 30). The master can now read consecutive bytes from the device, with the first data byte being read from the register address pointed by the previously written register address. Once the master sends a NACK, the device stops sending valid data.

### *I²C Communication with Remote-Side Devices*

The serializer supports I²C communication with a peripheral on the remote side of the communication link using SCL clock stretching. While multiple masters can reside on either side of the communication link, arbitration is not provided. The connected masters need to support SCL clock stretching. The remote-side I²C bit-rate range must be set according to the local-side I²C bit rate. Supported remote-side bit rates can be found in Table 4. Set the I2CMSTBT (register 0x0D) to set the remote I²C bit-rate. If using a bit rate different than 400kbps, local- and remote-side I²C setup and hold times should be adjusted by setting the SLV_SH register settings on both sides.

### *I²C Address Translation*

The serializer supports I²C address translation for up to two device addresses. Use address translation to assign unique device addresses to peripherals with limited I²C addresses. Source addresses (address to translate from) are stored in registers 0x09 and 0x0B. Destination addresses (address to translate to) are stored in registers 0x0A and 0x0C.

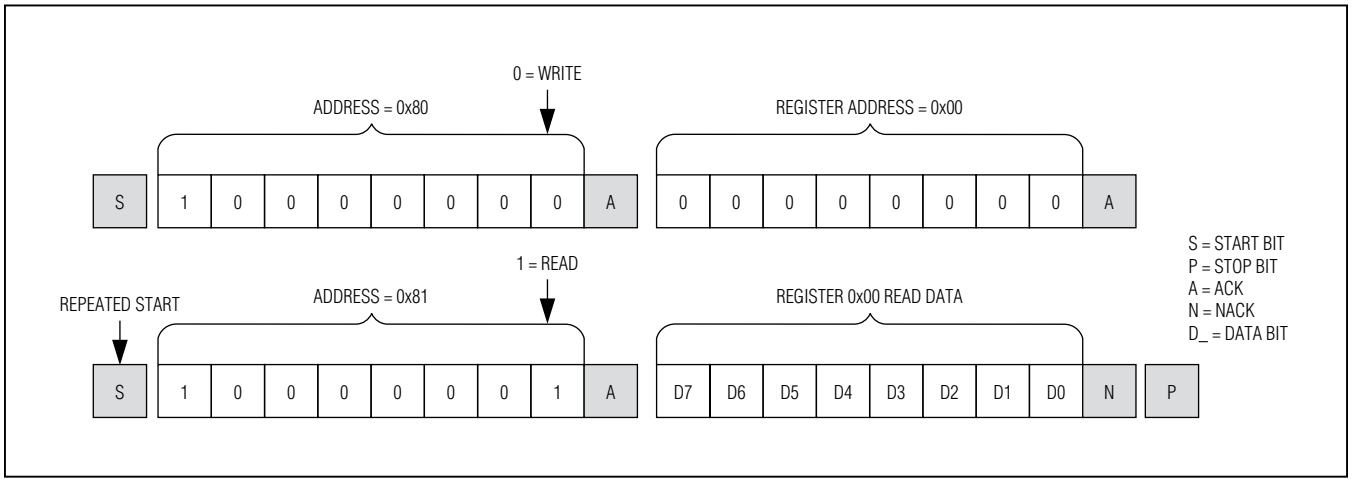



*Figure 30. Format for I²C Read*

## Table 4. I²C Bit-Rate Ranges

| LOCAL BIT RATE | REMOTE BIT-RATE RANGE | I2CMSTBT SETTING |
|---|---|---|
| f > 50kbps | Up to 1Mbps | Any |
| 20kbps > f > 50kbps | Up to 400kbps | Up to 110 |
| f < 20kbps | Up to 10kbps | 000 |

### Control-Channel Broadcast Mode

The serializer supports broadcast commands to control multiple peripheral devices. Select an unused device address to use as a broadcast device address. Program the remote-side GMSL device to translate the broadcast device address (source address stored in registers 0x09, 0x0B) to the peripheral device address (destination address stored in register 0x0A, 0x0C). Any commands sent to the broadcast address are sent to all designated peripherals, while commands sent to a peripheral's unique device address are sent to that particular device only.

### GPO/GPI Control

GPO on the serializer follows GPI transitions on the deserializer. This GPO/GPI function can be used to transmit signals such as frame sync in a surround-view camera system. The GPI-to-GPO delay is 0.35ms (max). Keep time between GPI transitions to a minimum 0.35ms. This includes transitions from the other deserializer in the coax-mode splitter. Bit D4 of register 0x0E in the deserializer stores the GPI input state. GPO is low after power-up. The µC can set GPO by writing to the SET_GPO register bit. Do not send a logic-low value on the serializer RX/SDA input (UART mode) longer than 100µs in either base or bypass mode to ensure proper GPO/GPI functionality.

### Pre/Deemphasis Driver

The serial line driver employs current-mode logic (CML) signaling. The driver is differential when programmed for twisted-pair cable. When programmed for coax, one side of the CML driver is used. The line driver has programmable pre/deemphasis that modifies the output to compensate for cable length. There are 13 preemphasis settings, as shown in Table 5. Negative preemphasis levels are deemphasis levels where the preemphasized swing level is the same as normal swing, but the no-transition data (e.g., a 1 followed by a 1) is deemphasized. Program the preemphasis levels through register 0x06 D[3:0] of the serializer. This preemphasis function compensates the high-frequency loss of the cable and enables reliable transmission over longer link distances. Current drive for both TP and coax modes is programmable. CMLLVL bits (0x06, D[7:4]) program drive current in TP and coax modes for single-ended voltage swings from 100mV to 500mV.

### Spread Spectrum

To reduce the EMI generated by the transitions on the serial link, the serializer output is programmable for spread spectrum. If the deserializer driven by the serializer has programmable spread spectrum, do not enable spread for both at the same time or their interaction

## Table 5. TP/Coax Drive Current (CMLLVL = 1000)

| PREEMPHASIS LEVEL (dB)* | PREEMP SETTING (0x06, D[3:0]) | $I_{CML}$ (mA) | $I_{PRE}$ (mA) | SINGLE-ENDED VOLTAGE SWING | |
|---|---|---|---|---|---|
| | | | | MAX (mV) | MIN (mV) |
| -6.0 | 0100 | 12 | 4 | 400 | 200 |
| -4.1 | 0011 | 13 | 3 | 400 | 250 |
| -2.5 | 0010 | 14 | 2 | 400 | 300 |
| -1.2 | 0001 | 15 | 1 | 400 | 350 |
| **0 (power-on default)** | **0000** | **16** | **0** | **400** | **400** |
| 1.1 | 1000 | 16 | 1 | 425 | 375 |
| 2.2 | 1001 | 16 | 2 | 450 | 350 |
| 3.3 | 1010 | 16 | 3 | 475 | 325 |
| 4.4 | 1011 | 16 | 4 | 500 | 300 |
| 6.0 | 1100 | 15 | 5 | 500 | 250 |
| 8.0 | 1101 | 14 | 6 | 500 | 200 |
| 10.5 | 1110 | 13 | 7 | 500 | 150 |
| 14.0 | 1111 | 12 | 8 | 500 | 100 |

**Negative preemphasis levels denote deemphasis.*

## Table 6. Serial Output Spread

| SS | SPREAD (%) |
|---|---|
| 000 | No spread spectrum. **Power-up default.** |
| 001 | ±0.5% spread spectrum. |
| 010 | ±1.5% spread spectrum. |
| 011 | ±2% spread spectrum. |
| 100 | No spread spectrum. |
| 101 | ±1% spread spectrum. |
| 110 | ±3% spread spectrum. |
| 111 | ±4% spread spectrum. |

## Table 7. Spread Limitations

| BWS = 0 MODE, PCLKIN FREQUENCY (MHz) | BWS = 1 MODE PCLKIN FREQUENCY (MHz) | SERIAL LINK BIT RATE (Mbps) | AVAILABLE SPREAD RATES |
|---|---|---|---|
| < 33.3 (DBL=0) | < 25 (DBL = 0) | < 1000 | All rates available |
| < 66.6 (DBL = 1) | < 50 (DBL = 1) | | |
| 33.3 to 50 (DBL = 0) | 25 to 37.5 (DBL = 0) | ≥ 1000 | 1.5%, 1.0%, 0.5% |
| 66.6 to 100 (DBL = 1) | 50 to 75 (DBL = 1) | | |

cancels benefits. The deserializer tracks the serializer's spread and passes the spread to the deserializer output. The programmable spread-spectrum amplitudes are ±0.5%, ±1%, ±1.5%, ±2%, ±3%, and ±4% (Table 6). Some spread-spectrum amplitudes can only be used at lower PCLKIN frequencies (Table 7). There is no PCLKIN frequency limit for the ±0.5% spread rate.

When the spread spectrum is turned on or off, the serial link stops for several microseconds and then restarts in order for the deserializer to lose and relock to the new serial-data stream.

The serializer includes a sawtooth divider to control the spread-modulation rate. Autodetection of the PCLKIN operation range guarantees a spread-spectrum modulation frequency within 20kHz to 40kHz. Additionally, manual configuration of the sawtooth divider (SDIV: 0x03, D[5:0]) allows the user to set a modulation frequency according to the PCLKIN frequency. When ranges are manually selected, program the SDIV value for a fixed modulation frequency around 20kHz.

### *Manual Programming of the Spread-Spectrum Divider*

The modulation rate relates to the PCLKIN frequency as follows:

$$f_M = (1 + DRS)\frac{f_{PCLKIN}}{MOD \times SDIV}$$

where:

$f_M$ = Modulation frequency

DRS = DRS value (0 or 1)

$f_{PCLKIN}$ = PCLKIN frequency

MOD = Modulation coefficient given in Table 8

SDIV = 6-bit SDIV setting, manually programmed by the µC

To program the SDIV setting, first look up the modulation coefficient according to the desired bus-width and spread-spectrum settings. Solve the above equation for SDIV using the desired pixel clock and modulation frequencies. If the calculated SDIV value is larger than the maximum allowed SDIV value in Table 8, set SDIV to the maximum value.

**Table 8. Modulation Coefficients and Maximum SDIV Settings**

| BWS | SPREAD-SPECTRUM SETTING (%) | MODULATION COEFFICIENT (dec) | SDIV UPPER LIMIT (dec) |
|---|---|---|---|
| 1 | 1 | 104 | 40 |
| | 0.5 | 104 | 63 |
| | 3 | 152 | 27 |
| | 1.5 | 152 | 54 |
| | 4 | 204 | 15 |
| | 2 | 204 | 30 |
| 0 | 1 | 80 | 52 |
| | 0.5 | 80 | 63 |
| | 3 | 112 | 37 |
| | 1.5 | 112 | 63 |
| | 4 | 152 | 21 |
| | 2 | 152 | 42 |

### *Additional Error Detection and Correction*

In default mode (additional error detection and correction disabled), data encoding/decoding is the same as in previous GMSL serializers/deserializers (parity only). At the serializer, the parallel input word is scrambled and a parity bit added. The scrambled word is divided into 3 or 4 bytes (depending on the BWS setting), 8b/10b encoded, and then transmitted serially. At the deserializer, the same operations are performed in reverse order. The parity bit is used by the deserializer to find the word boundary and for error detection. Errors are counted in an error counter register and an error pin indicates errors.

The serializer can use of of two additional error-detection/correction methods (selectable by register setting):

1) 6-bit cyclic redundancy check
2) 6-bit hamming code with 16-word interleaving

#### *Cyclic Redundancy Check (CRC)*

When CRC is enabled, the serializer adds 6 bits of CRC to the input data. This reduces the available bits in the input data word by 6, compared to the non-CRC case (see Table 2 for details). For example, 16 bits are available for input data instead of 22 bits when BWS = 0, and 24 bits instead of 30 bits when BWS = 1.

The CRC generator polynomial is $x^6 + x + 1$ (as used in the ITU-T G704 telecommunication standard).

The parity bit is still added when CRC is enabled, because it is used for word-boundary detection. When CRC is enabled, each data word is scrambled and then the 6-bit CRC and 1-bit parity are added before the 8b/10b encoding.

At the deserializer, the CRC code is recalculated. If the recalculated CRC code does not match the received CRC code, an error is flagged. This CRC error is reported to the error counter.

#### *Hamming Code*

Hamming code is a simple and effective error-correction code to detect and/or correct errors. The MAX9273 serializer (when used with the MAX9272 GMSL deserializer) uses single-error correction/double-error detection per pixel hamming-code scheme.

The serializer uses data interleaving for burst-error tolerance. Burst errors up to 11 consecutive bits on the serial link are corrected, and burst errors up to 31 consecutive bits are detected.

Hamming code adds overhead similar to CRC. See Table 2 for details regarding the available input word size.

### *HS/VS Encoding and/or Tracking*

HS/VS encoding by a GMSL serializer allows horizontal and vertical synchronization signals to be transmitted while conserving pixel data bandwidth. With HS/VS encoding enabled, 10-bit pixel data with a clock up to 100MHz can be transmitted using 1 pixel of data per HS/VS transition, versus 8-bit data with a clock up to 100MHz without HS/VS encoding. The deserializer performs HV decoding, tracks the period of the HV signals, and uses voting to filter HS/VS bit errors. When using HV encoding, use a minimum low-pulse duration of two PCLKIN cycles when DBL = 0 on the MAX9271/MAX9273. When DBL = 1, use a minimum HS/VS low-pulse duration of five PCLKIN cycles and a minimum high-pulse duration of two PCLKIN cycles. When using hamming code and HS/VS encoding, do not send more than two transitions every 16 PCLKIN cycles.

When the serializer uses double-input mode (DBL = 1), the active duration, plus the blanking duration of HS or VS signals, should be an even number of PCLKIN cycles.

If HS/VS tracking is used without HV encoding, use DIN0 for HSYNC and DIN1 for VSYNC. In this case, if DBL values on the serializer and the deserializer are different, set the deserializer's UNEQDBL register bit to 1. If the

serializer and deserializer have unequal DBL settings and HVEN = 0, then HS/VS inversion should only be used on the side that has DBL = 1. HS/VS encoding sends packets when HSYNC or VSYNC is low, use HS/VS inversion register bits if the input HSYNC and VSYNC signals use an active-low convention to send data packets during the inactive pixel clock periods.

### Serial Output

The driver output is programmable for two types of cable: 100Ω twisted pair and 50Ω coax (contact the factory for serializers with 75Ω cable drive).

### Coax-Mode Splitter

In coax mode, OUT+ and OUT- are active. This enables use as a 1:2 splitter (Figure 31). In coax mode, connect OUT+ to IN+ of the deserializer. Connect OUT- to IN- of the second deserializer. Control-channel data is broadcast from the serializer to both deserializers and their attached peripherals. Assign a unique device address to send control data to one deserializer. Leave all unused IN_ pins unconnected, or connect them to ground through 50Ω and a capacitor for increased power-supply rejection. If OUT- is not used, connect OUT- to AVDD through a 50Ω resistor (Figure 32). When there are µCs at the serializer, and at each deserializer, only one µC can communicate at a time. Disable one splitter control-channel link to prevent contention. Use the DIS_REV_P or DIS_REV_N register bits to disable a control-channel link.

### Configuration Inputs (CONF1, CONF0)

CONF1 and CONF0 determine the power-up values of the serial output type, the input data latch, and the control-channel interface type (Table 9). These functions can be changed after power-up by writing to the appropriate register bits

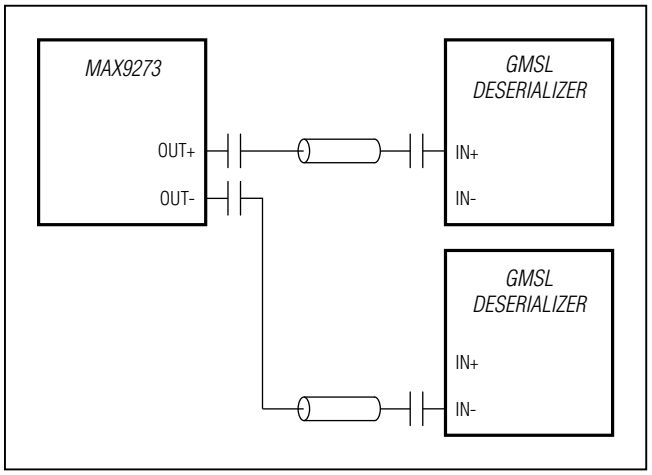



*Figure 31. 2:1 Coax-Mode Splitter Connection Diagram*

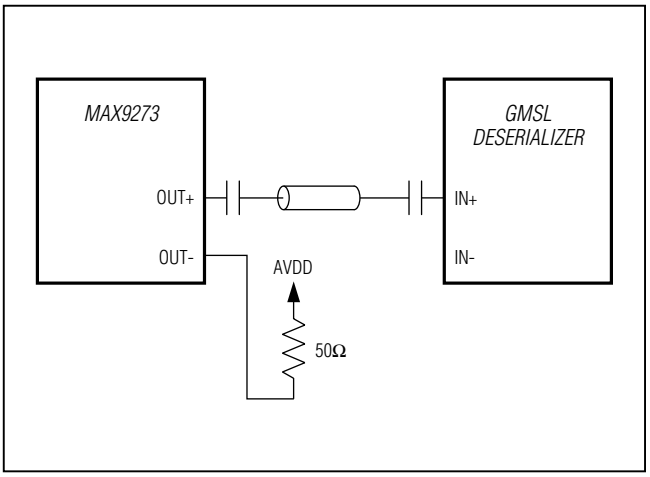



*Figure 32. Coax-Mode Connection Diagram*

## Table 9. Configuration Input Map

| CONF1 | CONF0 | CXTP (OUT+/OUT- OUTPUT TYPE) | ES (PCLKIN LATCH EDGE) | I2CSEL (CONTROL-CHANNEL TYPE) |
|---|---|---|---|---|
| Low | Low | 1 (coax) | 1 (falling) | 1 ($I^2C$-to-$I^2C$) |
| Low | Mid | 1 (coax) | 1 (falling) | 0 (UART-to-$I^2C$/UART) |
| Low | High | 1 (coax) | 0 (rising) | 1 ($I^2C$-to-$I^2C$) |
| Mid | Low | 1 (coax) | 0 (rising) | 0 (UART-to-$I^2C$/UART) |
| Mid | Mid | 0 (STP) | 1 (falling) | 1 ($I^2C$-to-$I^2C$) |
| Mid | High | 0 (STP) | 1 (falling) | 0 (UART-to-$I^2C$/UART) |
| High | Low | 0 (STP) | 0 (rising) | 1 ($I^2C$-to-$I^2C$) |
| High | Mid | 0 (STP) | 0 (rising) | 0 (UART-to-$I^2C$/UART) |
| High | High | Do not use | Do not use | Do not use |

### Sleep Mode

The serializer includes a sleep mode to reduce power consumption. The device enters or exits sleep mode by a command from a local µC or a remote µC using the control channel. Set the SLEEP bit to 1 to initiate sleep mode. The serializer sleeps immediately after setting its SLEEP = 1. The OUT+ and OUT- serial outputs each have wake-up receiver to accept wake-up commands from the attached deserializers. On power-up, the OUT+ wake-up receiver is enabled and the OUT- wake-up receiver is disabled. Disable the wake-up receivers (through ENWAKEP or ENWAKEN) if the devices are disconnected or wake-up is not used in order to reduce sleep-mode current. If both wake-up receivers are disabled, the device can only be woken up from the local control channel. To wake up the device, send an arbitrary control-channel command to the serializer. Wait 5ms for the chip to power up and then write 0 to the SLEEP register bit to make the wake-up permanent.

### Power-Down Mode

The serializer has a power-down mode that further reduces power consumption compared to sleep mode. Set $\overline{PWDN}$ low to enter power-down mode. In power-down mode, the serial outputs are in high impedance. Entering power-down resets the device's registers. Upon exiting power-down, the state of the MS, DRS, CONF0, CONF1, and $\overline{AUTOS}$ pins are latched.

## Table 10. Startup Procedure for Video-Display Applications

| NO. | µC | SERIALIZER | DESERIALIZER |
|---|---|---|---|
| — | µC connected to serializer. | Sets all configuration inputs. If any configuration inputs are available on one end of the link but not on the other, always connects that configuration input low. | Sets all configuration inputs. If any configuration inputs are available on one end of the link but not on the other, always connects that configuration input low. |
| 1 | Powers up. | Powers up and loads default settings. | Powers up and loads default settings. |
| 2 | Enables configuration link by setting CLINKEN = 1 (if not enabled automatically) and gets an acknowledge. Waits for link to be established (~3ms). | Establishes configuration link. | Locks to configuration link signal. |
| 3 | Writes one link configuration bit (DRS, BWS, or EDC) in the deserializer and gets an acknowledge. | — | Configuration changed from default settings (loss-of-lock occurs if BWS or EDC changes). |
| 4 | Writes corresponding serializer link configuration bit and gets an acknowledge. | Configuration changed from default settings. | Relocks to configuration link signal. |
| 5 | Waits for link to be established (~3ms) and then repeats steps 3 through 4 until all serial link bits are configured. | — | — |
| 6 | Writes remaining configuration bits in the serializer/deserializer and gets an acknowledge. | Configuration changed from default settings. | Configuration changed from default settings. |
| 7 | Enables video link by setting SEREN = 1 and gets an acknowledge. Waits for link to be established (~3ms). | Begins serializing data. | Locks to serial link signal and begins deserializing data. |

**Table 11. Startup Procedure for Image-Sensing Applications**

| NO. | µC | SERIALIZER | DESERIALIZER |
|---|---|---|---|
| — | µC connected to deserializer. | Sets all configuration inputs. If any inputs are available on one chip but not on the other, always connects input low. | Sets all configuration inputs. If any inputs are available on one chip but not on the other, always connects input low. |
| 1 | Powers up. | Powers up and loads default settings. Establishes serial link. | Powers up and loads default settings. Locks to serial link signal. |
| 3 | Writes deserializer configuration bits and gets an acknowledge. | — | Configuration changed from default settings (loss-of-lock occurs if BWS or EDC changes). |
| 4 | Writes serializer configuration bits. Does not get an acknowledge (or gets a dummy acknowledge) if loss-of-lock occurred. | Configuration changed from default settings. | Relocks to serial link signal. |
| 5 | Enables video link by setting SEREN = 1 (if not enabled automatically). Cannot get an acknowledge (or gets a dummy acknowledge) if loss-of-lock occurred. Waits for link to be established (~3ms). | Begins serializing data. | Locks to serial link signal and begins deserializing data. |

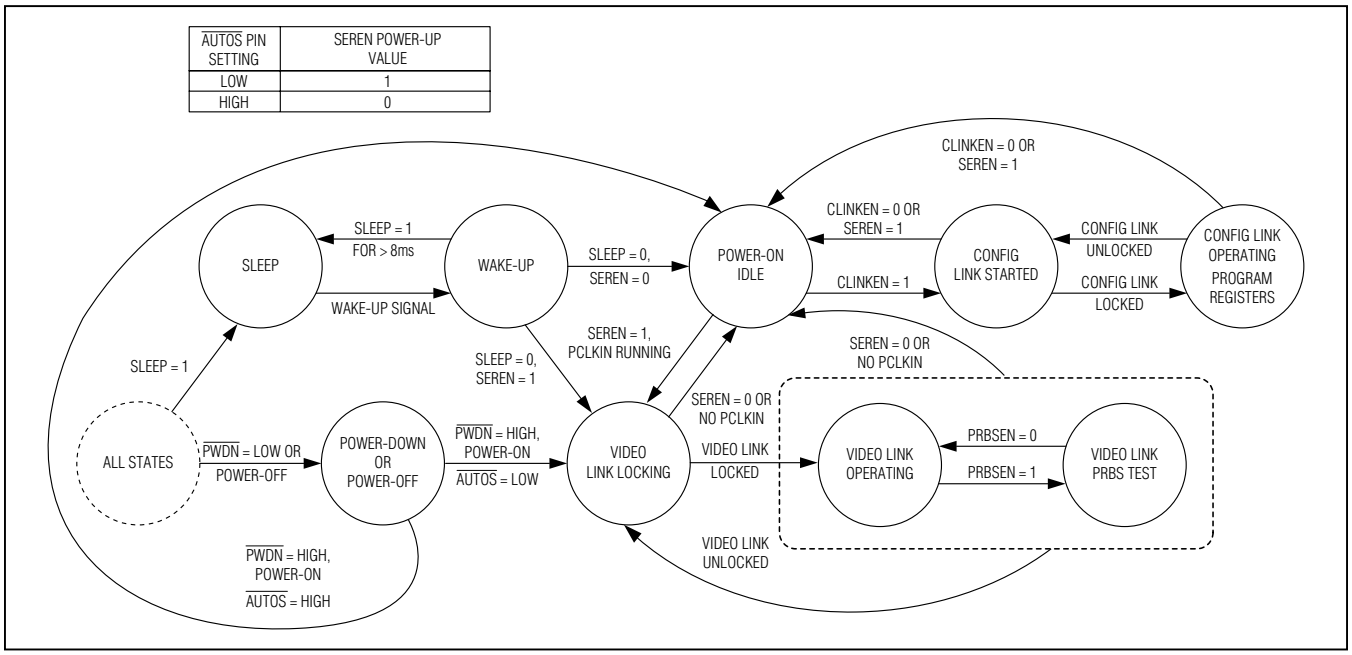



*Figure 33. State Diagram, All Applications*

### Configuration Link

The control channel can operate in a low-speed mode called configuration link in the absence of a clock input. This allows a microprocessor to program configuration registers before starting the video link. An internal oscillator provides the clock for configuration link. Set CLINKEN = 1 on the serializer to enable configuration link. Configuration link is active until the video link is enabled. The video link overrides the configuration link and attempts to lock when SEREN = 1.

## Link Startup Procedure

Table 10 lists the start-up procedure for video-display applications. Table 11 lists the startup procedure for image-sensing applications. The control channel is available after the video link or the configuration link is established. If the deserializer powers up after the serializer, the control channel becomes unavailable until 2ms after power-up.

## Applications Information

### PRBS Test

The serializer includes a PRBS pattern generator that works with bit-error verification in the deserializer. To run the PRBS test, set PRBSEN = 1 (0x04, D5) in the deserializer and then in the serializer. To exit the PRBS test, set PRBSEN = 0 (0x04, D5) in the serializer.

### Error Generator

The serializer contains an error generator that enables repeatable testing of the error-detection/correction features of the GMSL link. Register 0x11 stores the configuration bits for the error generator. A µC sets the error-generation rate, type of errors, and the total number of errors. The error generator is off by default.

### Dual µC Control

Usually systems have one µC to run the control channel, located on the serializer side for video-display applications or on the deserializer side for image-sensing applications. However, a µC can reside on each side simultaneously and trade off running the control channel. In this case, each µC can communicate with the serializer and deserializer and any peripheral devices.

Contention occurs if both µCs attempt to use the control channel at the same time. It is up to the user to prevent this contention by implementing a higher-level protocol. In addition, the control channel does not provide arbitration between I²C masters on both sides of the link. An acknowledge frame is not generated when communication fails due to contention. If communication across the serial link is not required, the µCs can disable the forward and reverse control channel using the FWDCCEN and REVCCEN bits (0x04, D[1:0]) in the serializer/deserializer. Communication across the serial link is stopped and contention between µCs cannot occur.

As an example of dual µC use in an image-sensing application, the serializer can be in sleep mode, waiting for wake-up by the µC on the deserializer side. After wake-up, the serializer-side µC assumes master control of the serializer's registers.

### Jitter-Filtering PLL

In some applications, the clock input (PCLKIN) includes noise, which reduces link reliability. The clock input has a programmable narrowband jitter-filter PLL that attenuates frequencies higher than 100kHz (typ). Enable the jitter-filter by setting ENJITFILT = 1 (0x05, D6).

### PCLKIN Spread Tracking

The serializer can operate with a spread PCLKIN signal. When using a spread PCLKIN signal, disable the jitter-filter by setting ENJITFILT = 0 (0x05, D6). Do not exceed the spread limitations in Table 7 and keep modulation less than 40kHz. In addition, turn off spread spectrum in the serializer/deserializer. The serializer/deserializer track the spread on PCLKIN.

### Changing the Clock Frequency

It is recommended that the serial link be enabled after the video clock ($f_{PCLKIN}$) and the control-channel clock ($f_{UART}/f_{I2C}$) are stable. When changing clock frequency, stop the video clock for 5µs, apply the clock at the new frequency, then restart the serial link or toggle SEREN. On-the-fly changes in clock frequency are possible if the new frequency is immediately stable and without glitches. The reverse control channel remains unavailable for 350µs after serial link start or stop. When using the UART interface, limit on-the-fly changes in $f_{UART}$ to factors of less than 3.5 at a time to ensure that the device recognizes the UART sync pattern. For example, when lowering the UART frequency from 1Mbps to 100kbps, first send data at 333kbps, then at 100kbps for reduction ratios of 3 and 3.333, respectively.

### Fast Detection of Loss-of-Synchronization

A measure of link quality is the recovery time from loss-of-synchronization. The host can be quickly notified of loss-of-lock by connecting the deserializer's LOCK output to the deserializer's GPI input. If LOCK is lost, GPO on the

serializer follows the transition of LOCK at GPI. If other sources also use the GPI input, the µC can implement a routine to distinguish between interrupts from loss-of-lock and normal interrupts. The control channel does not require an active video link and thus can always monitor LOCK. LOCK asserts for a synchronized video link but not for the configuration link.

### Providing a Frame Sync (Camera Applications)

The GPI/GPO provides a simple solution for camera applications that require a frame sync signal from the ECU (e.g., surround-view systems). Connect the ECU frame sync signal to the GPI input and connect the GPO output to the camera frame sync input. GPI/GPO have a typical delay of 275µs. Skew between multiple GPI/GPO channels is maximum 115µs. If a lower skew signal is required, connect the camera's frame sync input to one of the serializer's GPIOs and use an I²C broadcast write command to change the GPIO output state. This has a maximum skew of 1.5µs, independent from the used I²C bit rate.

### Software Programming of the Device Addresses

The serializer and deserializer have programmable device addresses. This allows multiple GMSL devices, along with I²C peripherals, to coexist on the same control channel. The serializer device address is in register 0x00 of each device, while the deserializer device address is in register 0x01 of each device. To change a device address, first write to the device whose address changes (register 0x00 of the serializer for serializer device address change, or register 0x01 of the deserializer for deserializer device address change). Then write the same address into the corresponding register on the other device (register 0x00 of the deserializer for serializer device address change, or register 0x01 of the serializer for deserializer device address change).

### Three-Level Configuration Inputs

CONF1 and CONF0 are three-level inputs that control the serial interface configuration and power-up defaults. Connect CONF1or CONF0 through a pullup resistor to IOVDD to set a high level, a pulldown resistor to GND to set a low level, or IOVDD/2 or open to set a midlevel. For digital control, use three-state logic to drive the three-level logic inputs.

### Configuration Blocking

The serializer can block changes to registers. Set CFGBLOCK to make all registers read only. Once set, the registers remain blocked until the supplies are removed or until $\overline{PWDN}$ is low.

### Compatibility with Other GMSL Devices

The MAX9273 serializer is designed to pair with the MAX9272 deserializer, but interoperates with any GMSL deserializer. See Table 12 for operating limitations.

### GPIOs

The serializer has five open-drain GPIOs available when not used as data or configuration inputs. Setting the GPIO enable bits (register 0x0E) to 1 enables the GPIOs and internally connects the respective data or configuration input low. Setting the GPIO output bits to 0 pulls the output low, while setting the bits to 1 leaves the output undriven, and pulled high through internal/external pullup resistors. The GPIO input buffers are enabled when the GPIO is enabled. The input states are stored in register 0x10. Set GPIO_OUT to 1 when using a GPIO_ as an input.

## Table 12. MAX9273 Feature Compatibility

| MAX9273 FEATURE | GMSL DESERIALIZER |
|---|---|
| HSYNC/VSYNC encoding | If feature not supported in deserializer, must be turned off in the serializer. |
| Hamming-code error correction | If feature not supported in deserializer, must be turned off in the serializer. |
| I²C-to-I²C | If feature not supported in deserializer, must use UART-to-I²C or UART-to-UART. |
| CRC error detection | If feature not supported in deserializer, must be turned off in the serializer. |
| Double input | If feature not supported in deserializer, data is output as a single word at half the input frequency. |
| Coax | If feature not supported in deserializer, must connect unused serial input through 200nF and 50Ω in series to AVDD and set the reverse control-channel amplitude to 100mV. |
| I²S encoding | If supported in the deserializer, disable I²S in the deserializer. |

### Internal Input Pulldowns

The control and configuration inputs (except three-level inputs) include a pulldown resistor to GND. External pulldown resistors are not needed.

### Choosing I²C/UART Pullup Resistors

The I²C and UART open-drain lines require a pullup resistor to provide a logic-high level. There are tradeoffs between power dissipation and speed, and a compromise may be required when choosing pullup resistor values. Every device connected to the bus introduces some capacitance even when the device is not in operation. I²C specifies 300ns rise times (30% to 70%) for fast mode, which is defined for data rates up to 400kbps (see the I²C specifications in the *AC Electrical Characteristics* table for details). To meet the fast-mode rise-time requirement, choose the pullup resistors so that rise time $t_R$ = 0.85 x $R_{PULLUP}$ x $C_{BUS}$ < 300ns. The waveforms are not recognized if the transition time becomes too slow. The serializer supports I²C/UART rates up to 1Mbps (UART-to-I²C mode) and 400kbps (I²C-to-I²C mode).

### AC-Coupling

AC-coupling isolates the receiver from DC voltages up to the voltage rating of the capacitor. Capacitors at the serializer output and at the deserializer input are needed for proper link operation and to provide protection if either end of the cable is shorted to battery. AC-coupling blocks low-frequency ground shifts and low-frequency common-mode noise.

### Selection of AC-Coupling Capacitors

Voltage droop and the digital sum variation (DSV) of transmitted symbols cause signal transitions to start from different voltage levels. Because the transition time is fixed, starting the signal transition from different voltage levels causes timing jitter. The time constant for an AC-coupled link needs to be chosen to reduce droop and jitter to an acceptable level. The RC network for an AC-coupled link consists of the CML/coax receiver termination resistor ($R_{TR}$), the CML/coax driver termination resistor ($R_{TD}$), and the series AC-coupling capacitors (C). The RC time constant for four equal-value series capacitors is (C x ($R_{TD}$ + $R_{TR}$))/4. $R_{TD}$ and $R_{TR}$ are required to match the transmission line impedance (usually 100Ω differential, 50Ω single-ended). This leaves the capacitor selection to change the system time constant. Use 0.2µF or larger high-frequency surface-mount ceramic capacitors, with sufficient voltage rating to withstand a short to battery, to pass the lower speed reverse control-channel signal. Use capacitors with a case size less than 3.2mm x 1.6mm to have lower parasitic effects to the high-speed signal.

### Power-Supply Circuits and Bypassing

The serializer uses an AVDD and DVDD of 1.7V to 1.9V. All inputs and outputs, except for the serial output, derive power from an IOVDD of 1.7V to 3.6V that scales with IOVDD. Proper voltage-supply bypassing is essential for high-frequency circuit stability.

### Power-Supply Table

Power-supply currents shown in the *Electrical Characteristics* table are the sum of the currents from AVDD, DVDD, and IOVDD. Typical currents from the individual power supplies are shown in Table 13.

### Cables and Connectors

Interconnect for CML typically has a differential impedance of 100Ω. Use cables and connectors that have matched differential impedance to minimize impedance discontinuities. Coax cables typically have a characteristic impedance of 50Ω (contact the factory for 75Ω operation). Table 14 lists the suggested cables and connectors used in the GMSL link.

## Table 13. Typical Power-Supply Currents (Using Worst-Case Input Pattern)

| PCLK (MHz) | AVDD (mA) | DVDD (mA) | IOVDD (mA) |
|---|---|---|---|
| 25 | 29.5 | 9.4 | 0.2 |
| 50 | 34.9 | 14.4 | 0.3 |

## Table 14. Suggested Connectors and Cables for GMSL

| SUPPLIER | CONNECTOR | CABLE | TYPE |
|---|---|---|---|
| Rosenberger | 59S2AX-400A5-Y | RG174 | Coax |
| JAE | MX38-FF | A-BW-Lxxxxx | STP |
| Nissei | GT11L-2S | F-2WME AWG28 | STP |
| Rosenberger | D4S10A-40ML5-Z | Dacar 538 | STP |

### Board Layout

Separate the LVCMOS logic signals and CML/coax high-speed signals to prevent crosstalk. Use a four-layer PCB with separate layers for power, ground, CML/coax, and LVCMOS logic signals. Layout PCB traces close to each other for a 100Ω differential characteristic impedance. The trace dimensions depend on the type of trace used (microstrip or stripline). Note that two 50Ω PCB traces do not have 100Ω differential impedance when brought close together—the impedance goes down when the traces are brought closer. Use a 50Ω trace for the single-ended output when driving coax.

Route the PCB traces for differential CML in parallel to maintain the differential characteristic impedance. Avoid vias. Keep PCB traces that make up a differential pair equal length to avoid skew within the differential pair.

### ESD Protection

ESD tolerance is rated for Human Body Model, IEC 61000-4-2, and ISO 10605. The ISO 10605 and IEC 61000-4-2 standards specify ESD tolerance for electronic systems. The serial outputs are rated for ISO 10605 ESD protection and IEC 61000-4-2 ESD protection. All pins are tested for the Human Body Model. The Human Body Model discharge components are $C_S$ = 100pF and $R_D$ = 1.5kΩ (Figure 34). The IEC 61000-4-2 discharge components are $C_S$ = 150pF and $R_D$ = 330Ω (Figure 35). The ISO 10605 discharge components are $C_S$ = 330pF and $R_D$ = 2kΩ (Figure 36).

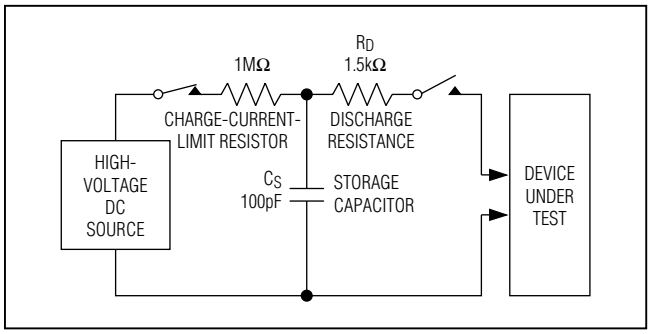



*Figure 34. Human Body Model ESD Test Circuit*

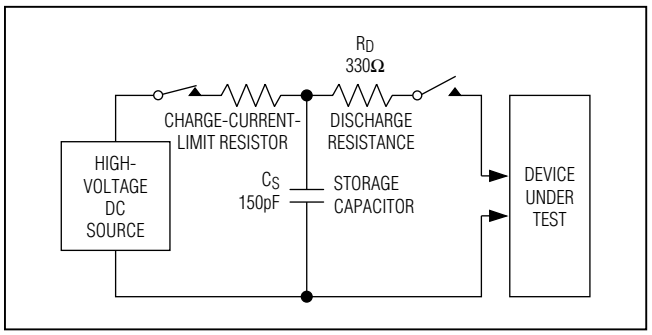



*Figure 35. IEC 61000-4-2 Contact Discharge ESD Test Circuit*

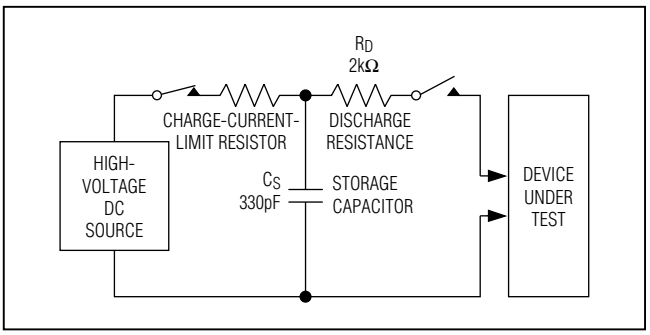



*Figure 36. ISO 10605 Contact Discharge ESD Test Circuit*

**Table 15. Register Table (see Table 1)**

| REGISTER ADDRESS | BITS | NAME | VALUE | FUNCTION | DEFAULT VALUE |
|---|---|---|---|---|---|
| 0x00 | D[7:1] | SERID | XXXXXXX | Serializer device address. | 1000000 |
| | D0 | CFGBLOCK | 0 | Normal operation. | 0 |
| | | | 1 | Registers 0x00 to 0x1F are read only. | |
| 0x01 | D[7:1] | DESID | XXXXXXX | Deserializer device address. | 1001000 |
| | D0 | — | 0 | Reserved. | 0 |
| 0x02 | D[7:5] | SS | 000 | No spread spectrum. | 000 |
| | | | 001 | ±0.5% spread spectrum. | |
| | | | 010 | ±1.5% spread spectrum. | |
| | | | 011 | ±2% spread spectrum. | |
| | | | 100 | No spread spectrum. | |
| | | | 101 | ±1% spread spectrum. | |
| | | | 110 | ±3% spread spectrum. | |
| | | | 111 | ±4% spread spectrum. | |
| | D4 | — | 1 | Reserved. | 1 |
| | D[3:2] | PRNG | 00 | 12.5MHz to 25MHz pixel clock. | 11 |
| | | | 01 | 25MHz to 50MHz pixel clock. | |
| | | | 10 | Automatically detect the pixel clock range. | |
| | | | 11 | Automatically detect the pixel clock range. | |
| | D[1:0] | SRNG | 00 | 0.5 to 1Gbps serial-bit rate. | 11 |
| | | | 01 | 1 to 2Gps serial-bit rate. | |
| | | | 10 | Automatically detect serial-bit rate. | |
| | | | 11 | Automatically detect serial-bit rate. | |
| 0x03 | D[7:6] | AUTOFM | 00 | Calibrate spread-modulation rate only once after locking. | 00 |
| | | | 01 | Calibrate spread-modulation rate every 2ms after locking. | |
| | | | 10 | Calibrate spread-modulation rate every 16ms after locking. | |
| | | | 11 | Calibrate spread-modulation rate every 256ms after locking. | |
| | D[5:0] | SDIV | 000000 | Autocalibrate sawtooth divider. | 000000 |
| | | | XXXXXX | Manual SDIV setting. See the *Manual Programming of the Spread-Spectrum Divider* section. | |

**Table 15. Register Table (see Table 1) (continued)**

| REGISTER ADDRESS | BITS | NAME | VALUE | FUNCTION | DEFAULT VALUE |
|---|---|---|---|---|---|
| 0x04 | D7 | SEREN | 0 | Disable serial link. **Power-up default when $\overline{\text{AUTOS}}$ = high.** Reverse control-channel communication remains unavailable for 350µs after the serializer starts/stops the serial link. | 0, 1 |
| | | | **1** | Enable serial link. **Power-up default when $\overline{\text{AUTOS}}$ = low.** Reverse control-channel communication remains unavailable for 350µs after the serializer starts/stops the serial link. | |
| | D6 | CLINKEN | 0 | Disable configuration link. | 0 |
| | | | 1 | Enable configuration link. | |
| | D5 | PRBSEN | 0 | Disable PRBS test. | 0 |
| | | | 1 | Enable PRBS test. | |
| | D4 | SLEEP | 0 | Normal mode. | 0 |
| | | | 1 | Activate sleep mode. | |
| | D[3:2] | INTTYPE | 00 | Local control channel uses I²C when I2CSEL = 0. | 00 |
| | | | 01 | Local control channel uses UART when I2CSEL = 0. | |
| | | | 10, 11 | Local control channel disabled. | |
| | D1 | REVCCEN | 0 | Disable reverse control channel from deserializer (receiving). | 1 |
| | | | 1 | Enable reverse control channel from deserializer (receiving). | |
| | D0 | FWDCCEN | 0 | Disable forward control channel to deserializer (sending). | 1 |
| | | | 1 | Enable forward control channel to deserializer (sending). | |
| 0x05 | D7 | I2CMETHOD | 0 | I²C conversion sends the register address when converting UART to I²C. | 0 |
| | | | 1 | Disable sending of I²C register address when converting UART-to-I²C (command-byte -only mode). | |
| | D6 | ENJITFILT | 0 | Jitter filter disabled. | 0 |
| | | | 1 | Jitter filter active. | |
| | D[5:4] | PRBSLEN | 00 | Continuous PRBS length. | 00 |
| | | | 01 | 9.83Mbit PRBS length. | |
| | | | 10 | 167.1Mbit PRBS length. | |
| | | | 11 | 1341.5Mbit PRBS length. | |
| | D[3:2] | — | 00 | Reserved. | 00 |
| | D1 | ENWAKEN | 0 | Disable wake-up receiver. | 0 |
| | | | 1 | Enable OUT- wake-up receiver during sleep mode. | |
| | D0 | ENWAKEP | 0 | Disable wake-up receiver. | 1 |
| | | | 1 | Enable OUT- wake-up receiver during sleep mode. | |

**Table 15. Register Table (see Table 1) (continued)**

| REGISTER ADDRESS | BITS | NAME | VALUE | FUNCTION | DEFAULT VALUE |
|---|---|---|---|---|---|
| 0x06 | D[7:4] | CMLLVL | 0000 | Do not use. | 1000, 1010 |
| | | | 0001 | Do not use. | |
| | | | 0010 | 100mV output level. | |
| | | | 0011 | 150mV output level. | |
| | | | 0100 | 200mV output level. | |
| | | | 0101 | 250mV output level. | |
| | | | 0110 | 300mV output level | |
| | | | 0111 | 350mV output level. | |
| | | | **1000** | 400mV output level. **Power-up default when twisted-pair output is selected (Table 9).** | |
| | | | 1001 | 450mV output level | |
| | | | **1010** | 500mV output level. **Power-up default when coax output is selected (Table 9).** | |
| | | | 1011 | Do not use. | |
| | | | 1100 | Do not use. | |
| | | | 1101 | Do not use. | |
| | | | 1110 | Do not use. | |
| | | | 1111 | Do not use. | |
| | D[3:0] | PREEMP | 0000 | Preemphasis off. | 0000 |
| | | | 0001 | -1.2dB preemphasis. | |
| | | | 0010 | -2.5dB preemphasis. | |
| | | | 0011 | -4.1dB preemphasis. | |
| | | | 0100 | -6.0dB preemphasis. | |
| | | | 0101 | Do not use. | |
| | | | 0110 | Do not use. | |
| | | | 0111 | Do not use. | |
| | | | 1000 | 1.1dB preemphasis. | |
| | | | 1001 | 2.2dB preemphasis. | |
| | | | 1010 | 3.3dB preemphasis. | |
| | | | 1011 | 4.4dB preemphasis. | |
| | | | 1100 | 6.0dB preemphasis. | |
| | | | 1101 | 8.0dB preemphasis. | |
| | | | 1110 | 10.5dB preemphasis. | |
| | | | 1111 | 14.0dB preemphasis. | |

**Table 15. Register Table (see Table 1) (continued)**

| REGISTER ADDRESS | BITS | NAME | VALUE | FUNCTION | DEFAULT VALUE |
|---|---|---|---|---|---|
| 0x07 | D7 | DBL | **0** | Single-input mode. | 0 |
| | | | 1 | Double-input mode. | |
| | D6 | DRS | 0 | High data-rate mode. | 0 |
| | | | 1 | Low data-rate mode. | |
| | D5 | BWS | 0 | 24-bit mode. | 0 |
| | | | 1 | 32-bit mode. | |
| | D4 | ES | 0 | Input data latched on rising edge of PCLKIN. **Power-up default determined by CONF1 and CONF0 (Table 9).** Do not change this value while the pixel clock is running. | 0, 1 |
| | | | 1 | Input data latched on falling edge of PCLKIN. **Power-up default determined by CONF1 and CONF0 (Table 9).** Do not change this value while the pixel clock is running. | |
| | D3 | — | 0 | Reserved. | 0 |
| | D2 | HVEN | 0 | HS/VS encoding disabled. | 0 |
| | | | 1 | HS/VS encoding enabled. | |
| | D[1:0] | EDC | 00 | 1-bit parity error detection (GMSL compatible). | 00 |
| | | | 01 | 6-bit CRC error detection. | |
| | | | 10 | 6-bit hamming code (single-bit error correct, double-bit error detect) and 16- word interleaving. | |
| | | | 11 | Do not use. | |
| 0x08 | D7 | INVVS | 0 | No VS or DIN0 inversion. | 0 |
| | | | 1 | Invert VS when HVEN = 1.<br>Invert DIN0 when HVEN = 0.<br>Do not use if DBL = 0 in the serializer and DBL = 1 in the deserializer. | |
| | D6 | INVHS | 0 | No HS or DIN1 inversion | 0 |
| | | | 1 | Invert HS when HVEN = 1.<br>Invert DIN1 when HVEN = 0.<br>Do not use if DBL = 0 in the serializer and DBL = 1 in the deserializer. | |
| | D[5:0] | — | 000000 | Reserved. | 000000 |
| 0x09 | D[7:1] | I2CSRCA | XXXXXXX | I²C address translator source A. | 0000000 |
| | D0 | — | 0 | Reserved. | 0 |
| 0x0A | D[7:1] | I2CDSTA | XXXXXXX | I²C address translator destination A. | 0000000 |
| | D0 | — | 0 | Reserved. | 0 |
| 0x0B | D[7:1] | I2CSRCB | XXXXXXX | I²C address translator source B. | 0000000 |
| | D0 | — | 0 | Reserved. | 0 |

**Table 15. Register Table (see Table 1) (continued)**

| REGISTER ADDRESS | BITS | NAME | VALUE | FUNCTION | DEFAULT VALUE |
|---|---|---|---|---|---|
| 0x0C | D[7:1] | I2CDSTB | XXXXXXX | I²C address translator destination B. | 0000000 |
| | D0 | — | 0 | Reserved. | 0 |
| 0x0D | D7 | I2CLOCACK | 0 | Acknowledge not generated when forward channel is not available. | 1 |
| | | | 1 | I²C-to-I²C slave generates local acknowledge when forward channel is not available. | |
| | D[6:5] | I2CSLVSH | 00 | 352ns/117ns I²C setup/hold time. | 01 |
| | | | 01 | 469ns/234ns I²C setup/hold time. | |
| | | | 10 | 938ns/352ns I²C setup/hold time. | |
| | | | 11 | 1046ns/469ns I²C setup/hold time. | |
| | D[4:2] | I2CMSTBT | 000 | 8.47kbps (typ) I²C-to-I²C master bit-rate setting. | 101 |
| | | | 001 | 28.3kbps (typ) I²C-to-I²C master bit-rate setting. | |
| | | | 010 | 84.7kbps (typ) I²C-to-I²C master bit-rate setting. | |
| | | | 011 | 105kbps (typ) I²C-to-I²C master bit-rate setting. | |
| | | | 100 | 173kbps (typ) I²C-to-I²C master bit-rate setting. | |
| | | | 101 | 339kbps (typ) I²C-to-I²C master bit-rate setting. | |
| | | | 110 | 533kbps (typ) I²C-to-I²C master bit-rate setting. | |
| | | | 111 | 837kbps (typ) I²C-to-I²C master bit-rate setting. | |
| | D[1:0] | I2CSLVTO | 00 | 64µs (typ) I²C-to-I²C slave remote timeout. | 10 |
| | | | 01 | 256µs (typ) I²C-to-I²C slave remote timeout. | |
| | | | 10 | 1024µs (typ) I²C-to-I²C slave remote timeout. | |
| | | | 11 | No I²C-to-I²C slave remote timeout. | |
| 0x0E | D7 | DIS_REV_P | 0 | OUT+ reverse channel receiver enabled. | 0 |
| | | | 1 | OUT+ reverse channel receiver disabled. | |
| | D6 | DIS_REV_N | 0 | OUT- reverse channel receiver enabled. | 1 |
| | | | 1 | OUT- reverse channel receiver disabled. | |
| | D5 | GPIO5EN | 0 | Disable GPIO5. | 0 |
| | | | 1 | Enable GPIO5. | |
| | D4 | GPIO4EN | 0 | Disable GPIO4. | 0 |
| | | | 1 | Enable GPIO4. | |
| | D3 | GPIO3EN | 0 | Disable GPIO3. | 0 |
| | | | 1 | Enable GPIO3. | |
| | D2 | GPIO2EN | 0 | Disable GPIO2. | 0 |
| | | | 1 | Enable GPIO2. | |
| | D1 | GPIO1EN | 0 | Disable GPIO1. | 1 |
| | | | 1 | Enable GPIO1. | |
| | D0 | — | 0 | Reserved. | 0 |

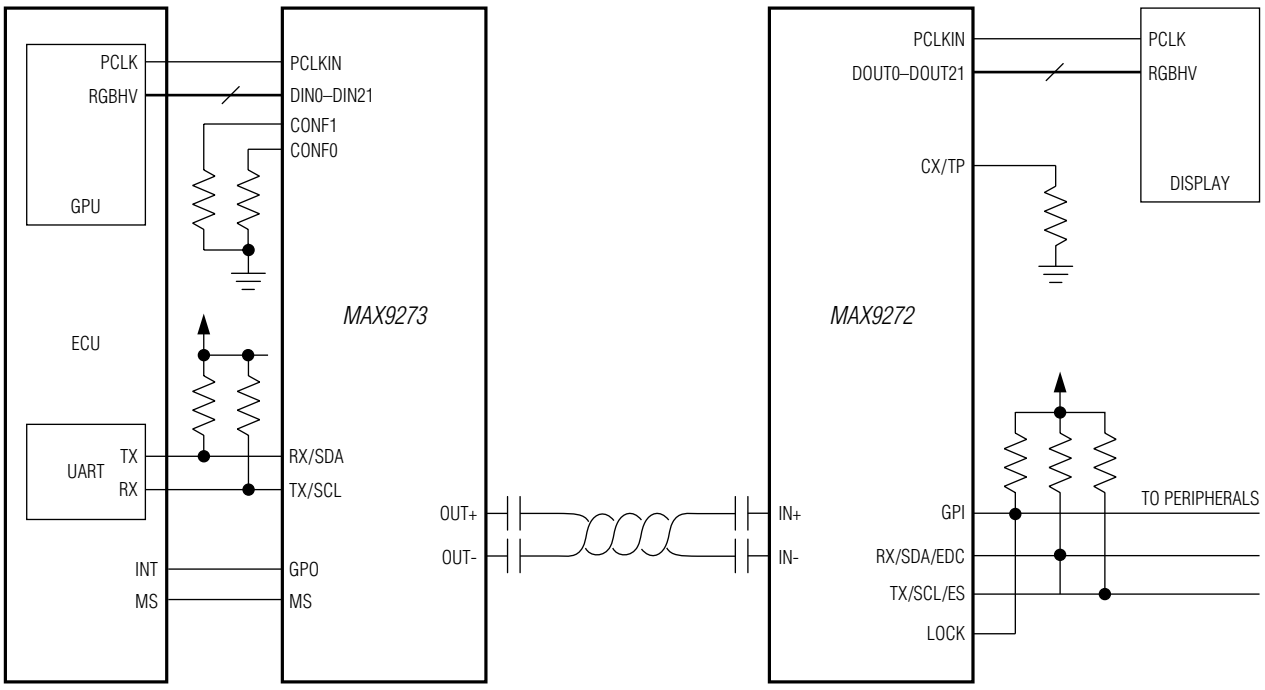
**Table 15. Register Table (see Table 1) (continued)**

| REGISTER ADDRESS | BITS | NAME | VALUE | FUNCTION | DEFAULT VALUE |
|---|---|---|---|---|---|
| 0x0F | D[7:6] | — | 11 | Reserved. | 11 |
| | D5 | GPIO5OUT | 0 | Set GPIO5 low. | 1 |
| | | | 1 | Set GPIO5 high. | |
| | D4 | GPIO4OUT | 0 | Set GPIO4 low. | 1 |
| | | | 1 | Set GPIO4 high. | |
| | D3 | GPIO3OUT | 0 | Set GPIO3 low. | 1 |
| | | | 1 | Set GPIO3 high. | |
| | D2 | GPIO2OUT | 0 | Set GPIO2 low. | 1 |
| | | | 1 | Set GPIO2 high. | |
| | D1 | GPIO1OUT | 0 | Set GPIO1 low. | 1 |
| | | | 1 | Set GPIO1 high. | |
| | D0 | SETGPO | 0 | Set GPO low. | 0 |
| | | | 1 | Set GPO high. | |
| 0x10 | D[7:6] | — | 00 | Reserved. | 00 |
| | D5 | GPIO5IN | 0 | GPIO5 is low. | 1 (read only) |
| | | | 1 | GPIO5 is high. | |
| | D4 | GPIO4IN | 0 | GPIO4 is low. | 1 (read only) |
| | | | 1 | GPIO4 is high. | |
| | D3 | GPIO3IN | 0 | GPIO3 is low. | 1 (read only) |
| | | | 1 | GPIO3 is high. | |
| | D2 | GPIO2IN | 0 | GPIO2 is low. | 1 (read only) |
| | | | 1 | GPIO2 is high. | |
| | D1 | GPIO1IN | 0 | GPIO1 is low. | 1 (read only) |
| | | | 1 | GPIO1 is high. | |
| | D0 | GPO_L | 0 | GPO is set low. | 0 (read only) |
| | | | 1 | GPO is set high. | |
| 0x11 | D[7:6] | ERRGRATE | 00 | Generate an error every 2560 bits. | 00 |
| | | | 01 | Generate an error every 40,960 bits. | |
| | | | 10 | Generate an error every 655,360 bits. | |
| | | | 11 | Generate an error every 10,485,760 bits. | |
| | D[5:4] | ERRGTYPE | 00 | Generate single-bit errors. | 00 |
| | | | 01 | Generate 2 (8b/10b) symbol errors. | |
| | | | 10 | Generate 3 (8b/10b) symbol errors. | |
| | | | 11 | Generate 4 (8b/10b) symbol errors. | |
| | D[3:2] | ERRGCNT | 00 | Continuously generate errors. | 00 |
| | | | 01 | 16 generated errors. | |
| | | | 10 | 128 generated errors. | |
| | | | 11 | 1024 generated errors. | |
| | D1 | ERRGPER | 0 | Disable periodic error generation. | 0 |
| | | | 1 | Enable periodic error generation. | |
| | D0 | ERRGEN | 0 | Disable error generator. | 0 |
| | | | 1 | Enable error generator. | |

**Table 15. Register Table (see Table 1) (continued)**

| REGISTER ADDRESS | BITS | NAME | VALUE | FUNCTION | DEFAULT VALUE |
|---|---|---|---|---|---|
| 0x12 | D[7:0] | — | 01000000 | Reserved. | 01000000 |
| 0x13 | D[7:0] | — | 00100010 | Reserved | 00100010 |
| 0x14 | D[7:0] | — | XXXXXXXX | Reserved. | 00000000 (read only) |
| 0x15 | D7 | CXTP | 0 | CXTP input is low. | 0 (read only) |
| | | | 1 | CXTP input is high. | |
| | D6 | I2CSEL | 0 | Input is high. | 0 (read only) |
| | | | 1 | Input is low. | |
| | D5 | LCCEN | 0 | Input is high. | 0 (read only) |
| | | | 1 | Input is low. | |
| | D[4:2] | — | 000 | Reserved. | 000 (read only) |
| | D1 | OUTPUTEN | 0 | Output disabled. | 0 (read only) |
| | | | 1 | Output enabled. | |
| | D0 | PCLKDET | 0 | Valid PCLKIN detected. | 0 (read only) |
| | | | 1 | Valid PCLKIN not detected. | |
| 0x16 | D[7:0] | — | XXXXXXXX | Reserved. | 00000000 (read only) |
| 0x17 | D[7:0] | — | XXXXXXXX | Reserved. | 00000000 (read only) |
| 0x1E | D[7:0] | ID | 00001011 | Device identifier (MAX9273 = 0x0B). | 00001011 (read only) |
| 0x1F | D[7:5] | — | 000 | Reserved. | 000 (read only) |
| | D4 | CAPS | 0 | Not HDCP capable. | 0 (read only) |
| | | | 1 | HDCP capable. | |
| | D[3:0] | REVISION | XXXX | Device revision. | (read only) |

## Typical Application Circuit




**NOTE:** NOT ALL PULLUP/PULLDOWN RESISTORS ARE SHOWN. SEE PIN DESCRIPTION FOR DETAILS.

VIDEO-DISPLAY APPLICATION

## Ordering Information

| PART | TEMP RANGE | PIN-PACKAGE |
|---|---|---|
| MAX9273GTL+ | -40°C to +105°C | 40 TQFN-EP* |
| MAX9273GTL/V+** | -40°C to +105°C | 40 TQFN-EP* |

*/V denotes an automotive qualified part.*
*+Denotes a lead(Pb)-free/RoHS-compliant package.*
**EP = Exposed pad.*
***Future product—contact factory for availability.*

## Chip Information

PROCESS: CMOS

## Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

| PACKAGE TYPE | PACKAGE CODE | OUTLINE NO. | LAND PATTERN NO. |
|---|---|---|---|
| 40 TQFN-EP | T4066+3 | 21-0141 | 90-0054 |

## Revision History

| REVISION NUMBER | REVISION DATE | DESCRIPTION | PAGES CHANGED |
|---|---|---|---|
| 0 | 6/12 | Initial release | — |
| 1 | 11/12 | Added nonautomotive package to *Ordering Information*. | 48 |

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