AT17LV65A[1], AT17LV128A[1], AT17LV256A[1]
AT17LV512A, AT17LV010A, AT17LV002A

FPGA Configuration EEPROM Memory
3.3V and 5V System Support

DATASHEET

Note 1. AT17LV65A, AT17LV128A, and AT17LV256A are Not Recommended for New Designs (NRND) and are Replaced by AT17LV512A.

Features

- EE Programmable Serial Memories Designed to Store Configuration Programs for Altera® FLEX® and APEX™ Field Programmable Gate Arrays (FPGA)
  - 65,536 x 1-bit[1]
  - 131,072 x 1-bit[1]
  - 262,144 x 1-bit[1]
  - 524,288 x 1-bit
  - 1,048,576 x 1-bit
  - 2,097,152 x 1-bit
- Supports both 3.3V and 5.0V Operating Voltage Applications
- In-System Programmable (ISP) via 2-wire Bus
- Simple Interface to SRAM FPGAs
- Compatible with the Atmel® AT6000, AT40K and AT94K Devices, Altera FLEX, APEX Devices, ORCA® FPGAs, Xilinx® XC3000, XC4000, XC5200, Spartan®, Virtex™ FPGAs, Motorola MPA1000 FPGAs
- Cascadable Read-back to Support Additional Configurations or Higher-density Arrays
- Very Low-power CMOS EEPROM Process
- Programmable Reset Polarity
- 8-lead PDIP and 20-lead PLCC Packages (Pin-compatible Across Product Family)
- Emulation of the Atmel AT24C Serial EEPROMs
- Low-power Standby Mode
- High-reliability
  - Endurance: 100,000 Write Cycles
  - Data Retention: 90 Years for Industrial Parts (at 85°C)
- Green (Pb/Halide-free/RoHS Compliant) Package Options Available

Description

The Atmel® AT17LVxxxA FPGA configuration EEPROMs (Configurators) provide an easy-to-use, cost-effective configuration memory solution for FPGAs. The AT17LVxxxA are packaged in 8-lead PDIP and 20-lead PLCC options. The AT17LVxxxA configurator uses a simple serial-access procedure to configure one or more FPGA devices. The user can select the polarity of the reset function by programming four EEPROM bytes. These devices support a write protection mechanism within its programming mode.

The AT17LVxxxA configurators can be programmed with industry-standard programmers, the Atmel ATDH2200E Programming Kit, or the Atmel ATDH2225 ISP Cable.

Table 1. AT17LVxxxA Packages

Package	AT17LV512A	AT17LV010A	AT17LV002A
8-lead PDIP	Yes	Yes	–
20-lead PLCC	Yes	Yes	Yes

1. Pin Configuration and Descriptions

Table 1-1. Pin Descriptions

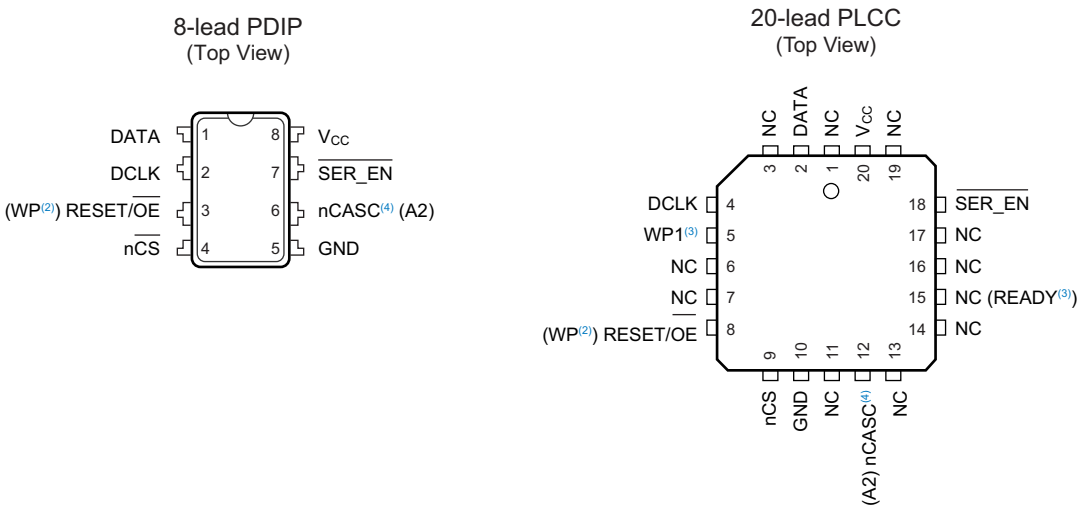
Pin	Description
DATA	**Three-state DATA Output for Configuration**. Open-collector bi-directional pin for programming.
DCLK	**Clock Output or Clock Input**. Rising edges on DCLK increment the internal address counter and present the next bit of data to the DATA pin. The counter is incremented only if the RESET/$\overline{OE}$ input is held High, the nCS input is held Low, and all configuration data has not been transferred to the target device (otherwise, as the master device, the DCLK pin drives Low).
WP1	**Write Protect (1)**. This pin is used to protect portions of memory during programming, and it is disabled by default due to internal pull-down resistor. This input pin is not used during FPGA loading operations. This pin is only available on the AT17LV512A/010A/002A.
$\overline{RESET/OE}$	**RESET** (Active Low) / **Output Enable** (Active High) when $\overline{SER\_EN}$ is High. A Low logic level resets the address counter. A High logic level (with nCS Low) enables DATA and permits the address counter to count. In the mode, if this pin is Low (reset), the internal oscillator becomes inactive and DCLK drives Low. The logic polarity of this input is programmable and must be programmed active High (RESET active Low) by the user during programming for Altera applications.
WP	**Write Protect Input** (when $\overline{nCS}$ is Low) during programming only ($\overline{SER\_EN}$ Low). When WP is Low, the entire memory can be written. When WP is enabled (High), the lowest block of the memory cannot be written. This pin is only available on AT17LV65A/128A/256A devices.
$\overline{nCS}$	**Chip Select Input** (Active Low). A Low input (with OE High) allows DCLK to increment the address counter and enables DATA to drive out. If the AT17LVxxxA is reset with nCS Low, the device initializes as the first (and master) device in a daisy-chain. If the AT17LVxxxA is reset with nCS High, the device initializes as a subsequent AT17LVxxxA in the chain.
GND	**Ground**. A 0.2µF decoupling capacitor between V_{CC} and GND is recommended.
nCASC	**Cascade Select Output** (Active Low). This output goes Low when the address counter has reached its maximum value. In a daisy-chain of AT17LVxxxA devices, the nCASC pin of one device is usually connected to the nCS input pin of the next device in the chain, which permits DCLK from the master configurator to clock data from a subsequent AT17LVxxxA device in the chain. This feature is not available on the AT17LV65A (NRND).
A2	**Device Selection Input, A2.** This is used to enable (or select) the device during programming (i.e., when $\overline{SER\_EN}$ is Low). A2 has an internal pull-down resistor.
READY	**Open Collector Reset State Indicator.** Driven Low during power-on reset cycle, released when power-up is complete. (recommended 4.7kΩ pull-up on this pin if used).
$\overline{SER\_EN}$	**Serial Enable** must be held High during FPGA loading operations. Bringing $\overline{SER\_EN}$ Low enables the 2-wire Serial Programming Mode. For non-ISP applications, $\overline{SER\_EN}$ should be tied to V_{CC}.
V_{CC}	**Power Supply.** 3.3V (±10%) and 5.0V (±10%) power supply pin.

Table 1-2. Pin Configurations

Name	I/O	AT17LV65A/128A/256A[2]	AT17LV512A/010A		AT17LV002A
		20-lead PLCC	8-lead PDIP	20-lead PLCC	20-lead PLCC
DATA	I/O	2	1	2	2
DCLK	I	4	2	4	4
WP1	I	–	–	5	5
RESET/$\overline{OE}$	I	8	3	8	8
$\overline{nCS}$	I	9	4	9	9
GND		10	5	10	10
$\overline{nCASC}$[1]	O	12	6	12	12
A2	I				
READY	O	–	–	15	15
$\overline{SER\_EN}$	I	18	7	18	18
V_{CC}		20	8	20	20

Notes: 1. The nCASC feature is not available on the AT17LV65A (NRND) device.
2. The AT17LV65A, AT17LV128A, and AT17LV256A are not recommended for new designs.

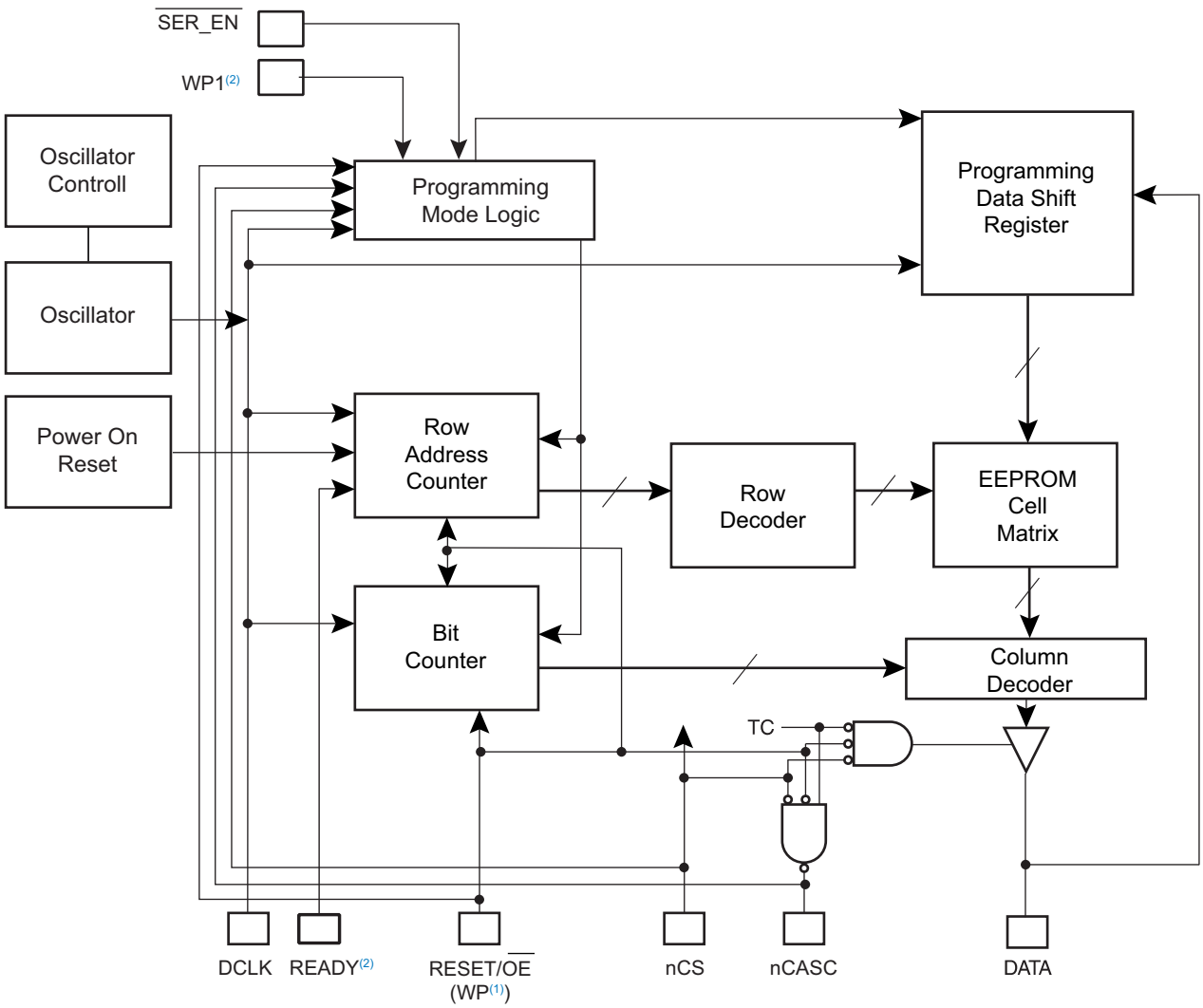
Figure 1-1. Pinouts[1]



Notes: 1. Drawings are not to scale.
2. This pin is only available on the AT17LV65A/128A/256A (NRND).
3. This pin is only available on the AT17LV512A/010A/002A.
4. The nCASC feature is not available on the AT17LV65A (NRND).

2. Block Diagram

Figure 2-1. Block Diagram



Notes:
1. This pin is only available on AT17LV65A/128A/256A (NRND).
2. This pin is only available on AT17LV512A/010A/002A.
3. The nCASC feature is not available on the AT17LV65A (NRND).

3. Device Description

The control signals for the configuration EEPROM (nCS, RESET/$\overline{OE}$ and DCLK) interface directly with the FPGA device control signals. All FPGA devices can control the entire configuration process and retrieve data from the configuration EEPROM without requiring an external controller.

The configuration EEPROM's RESET/$\overline{OE}$ and nCS pins control the tri-state buffer on the DATA output pin and enable the address counter and the oscillator. When RESET/$\overline{OE}$ is driven Low, the configuration EEPROM resets its address counter and tri-states its DATA pin. The nCS pin also controls the output of the AT17LVxxxA configurator. If nCS is held High after the RESET/$\overline{OE}$ pulse, the counter is disabled and the DATA output pin is tri-stated. When nCS is driven subsequently Low, the counter and the DATA output pin are enabled. When RESET/$\overline{OE}$ is driven Low again, the address counter is reset and the DATA output pin is tri-stated, regardless of the state of the nCS.

When the configurator has driven out all of its data and nCASC is driven Low, the device tri-states the DATA pin to avoid contention with other configurators. Upon power-up, the address counter is automatically reset.

This is the default setting for the device. Since almost all FPGAs use RESET Low and OE High, this document will describe $\overline{RESET}$/OE.

4. FPGA Master Serial Mode Summary

The I/O and logic functions of any SRAM-based FPGA are established by a configuration program. The program is loaded either automatically upon power-up, or on command, depending on the state of the FPGA mode pins. In Master mode, the FPGA automatically loads the configuration program from an external memory. The AT17LVxxxA Serial Configuration EEPROM has been designed for compatibility with the Master Serial mode.

This document discusses the Altera FLEX FPGA device interfaces.

5. Control of Configuration

Most connections between the FPGA device and the AT17LVxxxA Serial EEPROM are simple and self-explanatory.

- The DATA output of the AT17LVxxxA configurator drives DIN of the FPGA devices.
- The master FPGA DCLK output or external clock source drives the DCLK input of the AT17LVxxxA configurator.
- The nCASC output of any AT17LVxxxA configurator drives the nCS input of the next configurator in a cascaded chain of EEPROMs.
- $\overline{SER\_EN}$ must be connected to V_{CC} (except during ISP).

6. Cascading Serial Configuration EEPROMs

For multiple FPGAs configured as a daisy-chain, or for FPGAs requiring larger configuration memories, cascaded configurators provide additional memory.

After the last bit from the first configurator is read, the next clock signal to the configurator asserts its nCASC output low and disables its DATA line driver. The second configurator recognizes the low level on its nCS input and enables its DATA output.

After configuration is complete, the address counters of all cascaded configurators are reset if the RESET/$\overline{OE}$ on each configurator is driven to a Low level.

If the address counters are not to be reset upon completion, then the RESET/$\overline{OE}$ input can be tied to a High level.

The AT17LV65A (NRND) does not have the nCASC feature to perform cascaded configurations.

7. AT17LVxxxA Reset Polarity

The AT17LVxxxA configurator allows the user to program the polarity of the RESET/$\overline{OE}$ pin as either RESET/$\overline{OE}$ or $\overline{RESET}$/OE. This feature is supported by industry-standard programmer algorithms.

8. Programming Mode

The programming mode is entered by bringing $\overline{SER\_EN}$ Low. In this mode the chip can be programmed by the 2-wire serial bus. The programming is done at V_{CC} supply only. Programming super voltages are generated inside the chip.

9. Standby Mode

The AT17LVxxxA enters a low-power standby mode whenever nCS is asserted High. In this mode, the configurator consumes less than 150µA of current at 3.3V. The output remains in a high-impedance state regardless of the state of the RESET/$\overline{OE}$ input.

10. Electrical Specifications

10.1 Absolute Maximum Ratings*

Operating Temperature	-40°C to +85°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-0.1V to V_{CC} +0.5V
Supply Voltage (V_{CC})	-0.5V to +7.0V
Maximum Soldering Temp. (10s @ 1/16 in.)	260°C
ESD (R_{ZAP} = 1.5K, C_{ZAP} = 100 pF)	2000V

*Notice: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those listed under operating conditions is not implied. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect device reliability.

10.2 Operating Conditions

Table 10-1. Operating Conditions

Symbol	Description		3.3V		5.0V		Units
			Min	Max	Min	Max	
V_{CC}	Industrial	Supply voltage relative to GND -40°C to +85°C	3.0	3.6	4.5	5.5	V

10.3 DC Characteristics

Table 10-2. DC Characteristics for V_{CC} = 3.3V ± 10%

Symbol	Description	AT17LV65A/128A/256A(1)		AT17LV512A/010A		AT17LV002A		Units
		Min	Max	Min	Max	Min	Max	
V_{IH}	High-level Input Voltage	2.0	V_{CC}	2.0	V_{CC}	2.0	V_{CC}	V
V_{IL}	Low-level Input Voltage	0	0.8	0	0.8	0	0.8	V
V_{OH}	High-level Output Voltage (I_{OH} = -2mA)	2.4		2.4		2.4		V
V_{OL}	Low-level Output Voltage (I_{OL} = +3mA)		0.4		0.4		0.4	V
I_{CCA}	Supply Current, Active Mode		5		5		5	mA
I_L	Input or Output Leakage Current (V_{IN} = V_{CC} or GND)	-10	10	-10	10	-10	10	µA
I_{CCS}	Supply Current, Standby Mode		100		100		150	µA

Note: 1. The AT17LV65A, AT17LV128A, and AT17LV256A are not recommended for new designs.

Table 10-3. DC Characteristics for V_{CC} = 5.0V ± 10%

Symbol	Description	AT17LV65A/128A/256A(1)		AT17LV512A/010A		AT17LV002A		Units
		Min	Max	Min	Max	Min	Max	
V_{IH}	High-level Input Voltage	2.0	V_{CC}	2.0	V_{CC}	2.0	V_{CC}	V
V_{IL}	Low-level Input Voltage	0	0.8	0	0.8	0	0.8	V
V_{OH}	High-level Output Voltage (I_{OH} = -2mA)	3.6		3.76		3.76		V
V_{OL}	Low-level Output Voltage (I_{OL} = +3mA)		0.37		0.37		0.37	V
I_{CCA}	Supply Current, Active Mode		10		10		10	mA
I_L	Input or Output Leakage Current (V_{IN} = V_{CC} or GND)	-10	10	-10	10	-10	10	µA
I_{CCS1}	Supply Current, Standby Mode		150		200		350	µA

Note: 1. The AT17LV65A, AT17LV128A, and AT17LV256A are not recommended for new designs.

10.4 AC Characteristics

Table 10-4. AC Characteristics for V_{CC} = 3.3V ± 10%

Symbol	Description	AT17LV65A/128A/256A(3)		AT17LV512A/010A/002A		Units
		Min	Max	Min	Max	
T_{OE}(1)	OE to Data Delay		55		55	ns
T_{CE}(1)	$\overline{CE}$ to Data Delay		60		60	ns
T_{CAC}(1)	CLK to Data Delay		80		60	ns
T_{OH}	Data Hold from $\overline{CE}$, OE, or CLK	0		0		ns
T_{DF}(2)	$\overline{CE}$ or OE to Data Float Delay		55		50	ns
T_{LC}	CLK Low Time	25		25		ns
T_{HC}	CLK High Time	25		25		ns
T_{SCE}	$\overline{CE}$ Setup Time to CLK (to guarantee proper counting)	60		35		ns
T_{HCE}	$\overline{CE}$ Hold Time from CLK (to guarantee proper counting)	0		0		ns
T_{HOE}	OE High Time (guarantees counter is reset)	25		25		ns
F_{MAX}	Maximum Input Clock Frequency	10		10		MHz

Notes: 1. AC test lead = 50pF.
2. Float delays are measured with 5pF AC loads. Transition is measured ± 200mV from steady-state active levels.
3. The AT17LV65A, AT17LV128A, and AT17LV256A are not recommended for new designs.

Table 10-5. AC Characteristics when Cascading for V_{CC} = 3.3V ± 10%

Symbol	Description	AT17LV65A/128A/256A[3]		AT17LV512A/010A/002A		Units
		Min	Max	Min	Max	
T_{CDF}[2]	CLK to Data Float Delay		60		50	ns
T_{OCK}[1]	CLK to $\overline{CEO}$ Delay		60		55	ns
T_{OCE}[1]	$\overline{CE}$ to $\overline{CEO}$ Delay		60		40	ns
T_{OOE}[1]	$\overline{RESET}$/OE to $\overline{CEO}$ Delay		45		35	ns
F_{MAX}	Maximum Input Clock Frequency	8		10		MHz

Notes:
1. AC test lead = 50pF.
2. Float delays are measured with 5pF AC loads. Transition is measured ± 200mV from steady-state active levels.
3. The AT17LV65A, AT17LV128A, and AT17LV256A are not recommended for new designs.

Table 10-6. AC Characteristics for V_{CC} = 5.0V ± 10%

Symbol	Description	AT17LV65A/128A/256A[3]		AT17LV512A/010A/002A		Units
		Min	Max	Min	Max	
T_{OE}[1]	OE to Data Delay		35		35	ns
T_{CE}[1]	$\overline{CE}$ to Data Delay		45		45	ns
T_{CAC}[1]	CLK to Data Delay		55		50	ns
T_{OH}	Data Hold from $\overline{CE}$, OE, or CLK	0		0		ns
T_{DF}[2]	$\overline{CE}$ or OE to Data Float Delay		50		50	ns
T_{LC}	CLK Low Time	20		20		ns
T_{HC}	CLK High Time	20		20		ns
T_{SCE}	$\overline{CE}$ Setup Time to CLK (to guarantee proper counting)	40		25		ns
T_{HCE}	$\overline{CE}$ Hold Time from CLK (to guarantee proper counting)	0		0		ns
T_{HOE}	OE High Time (guarantees counter is reset)	20		20		ns
F_{MAX}	Maximum Input Clock Frequency	12.5		15		MHz

Notes:
1. AC test lead = 50pF.
2. Float delays are measured with 5pF AC loads. Transition is measured ± 200mV from steady-state active levels.
3. The AT17LV65A, AT17LV128A, and AT17LV256A are not recommended for new designs.

Table 10-7. AC Characteristics when Cascading for V_{CC} = 5.0V ± 10%

Symbol	Description	AT17LV65A/128A/256A(3)		AT17LV512A/010A/002A		Units
		Min	Max	Min	Max	
T_{CDF}(2)	CLK to Data Float Delay		50		50	ns
T_{OCK}(1)	CLK to $\overline{CEO}$ Delay		40		40	ns
T_{OCE}(1)	$\overline{CE}$ to $\overline{CEO}$ Delay		35		35	ns
T_{OOE}(1)	$\overline{RESET}$/OE to $\overline{CEO}$ Delay		35		30	ns
F_{MAX}	Maximum Input Clock Frequency	10		12.5		MHz

Notes: 1. AC test lead = 50pF.
2. Float delays are measured with 5pF AC loads. Transition is measured ± 200mV from steady-state active levels.
3. The AT17LV65A, AT17LV128A, and AT17LV256A are not recommended for new designs.

Figure 10-1. AC Waveforms

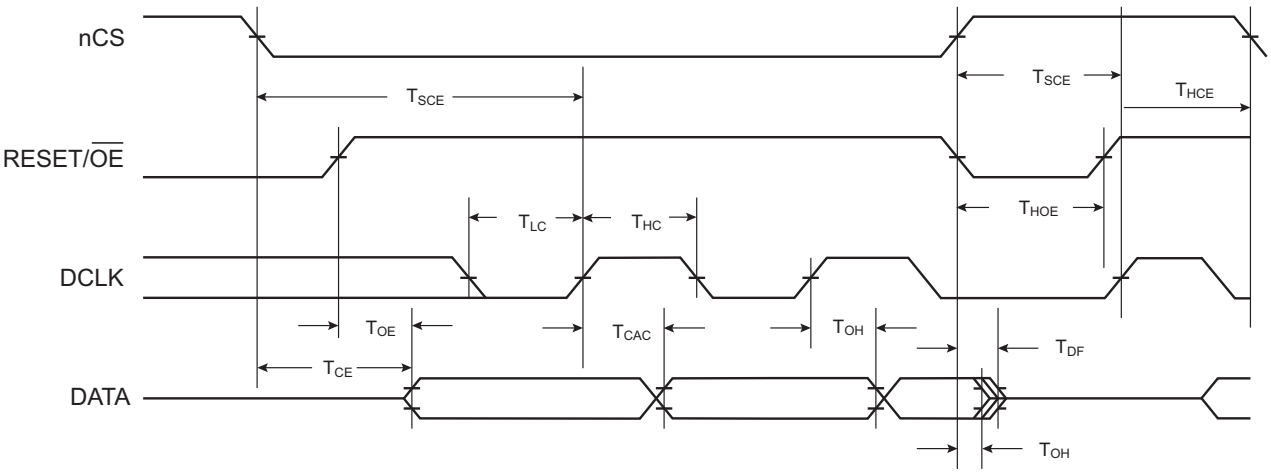
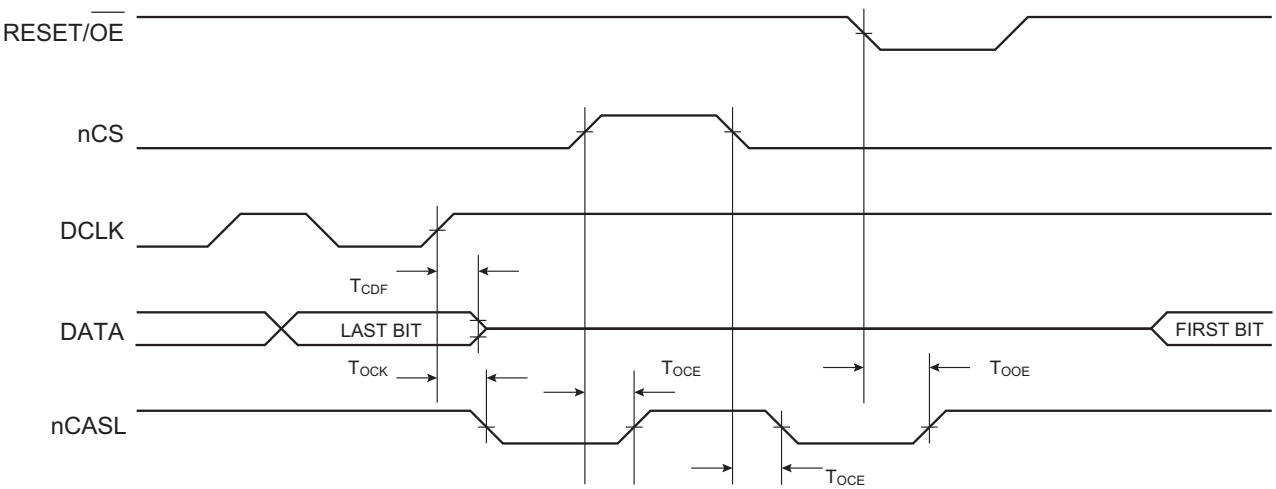


Figure 10-2. AC Waveforms when Cascading



10.5 Thermal Resistance Coefficients

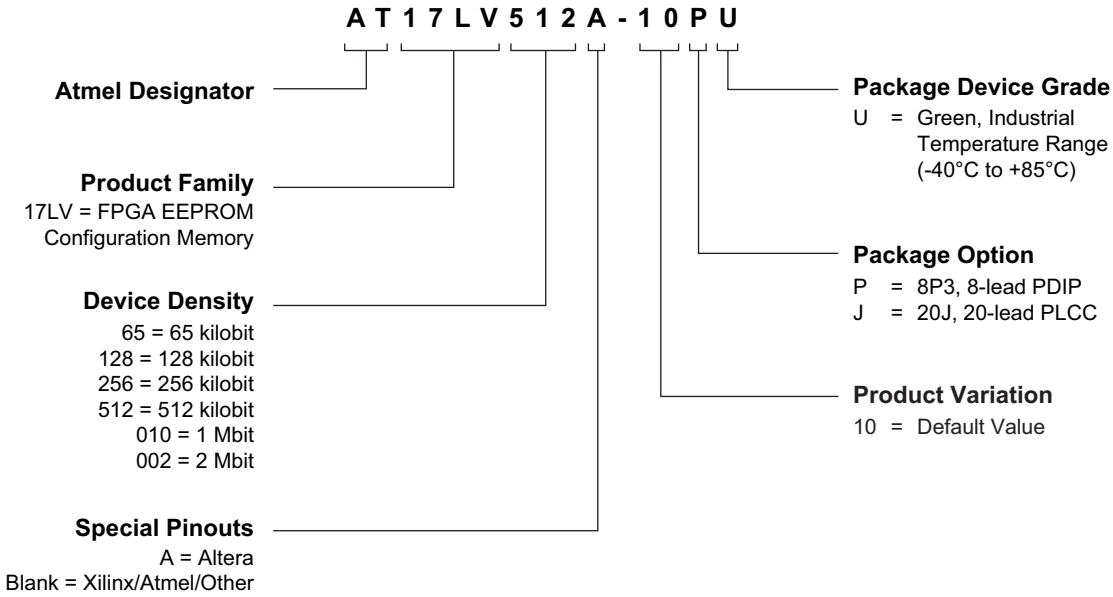
Table 10-8. Thermal Resistance Coefficients

Package Type			AT17LV65A/128A/256A[2]	AT17LV512A/010A	AT17LV002A
8P3	Plastic Dual Inline Package (PDIP)	θ_{JC} [°C/W]		37	
		θ_{JA} [°C/W][1]		107	
20J	Plastic Leaded Chip Carrier (PLCC)	θ_{JC} [°C/W]	35	35	35
		θ_{JA} [°C/W][1]	90	90	90

Notes: 1. Airflow = 0ft/min.
2. The AT17LV65A, AT17LV128A, and AT17LV256A are not recommended for new designs.

11. Ordering Information

11.1 Ordering Code Detail



11.2 Ordering Information

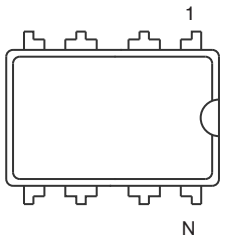
Memory Size	Atmel Ordering Code	Lead Finish	Package	Voltage	Operation Range
512-Kbit(1)(4)	AT17LV512A-10JU	Sn (Lead-free/Halogen-free)	20J	3.0V to 5.5V	Industrial (-40°C to 85°C)
	AT17LV512A-10PU		8P3		
1-Mbit(2)(4)	AT17LV010A-10JU	Sn (Lead-free/Halogen-free)	20J	3.0V to 5.5V	Industrial (-40°C to 85°C)
	AT17LV010A-10PU		8P3		
2-Mbit(1)(4)	AT17LV002A-10JU	Sn (Lead-free/Halogen-free)	20J	3.0V to 5.5V	Industrial (-40°C to 85°C)

Notes:
1. Use 512-Kbit density parts to replace Altera EPC1441.
2. Use 1-Mbit density parts to replace Altera EPC1
3. Use 2-Mbit density parts to replace Altera EPC2.
4. The AT17LVxxxA do not support JTAG programming. They use a 2-wire serial interface for in-system programming.

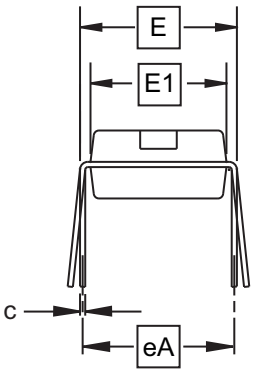
	Package Type
8P3	8-lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
20J	20-lead, Plastic J-leaded Chip Carrier (PLCC)

12. Packaging Information

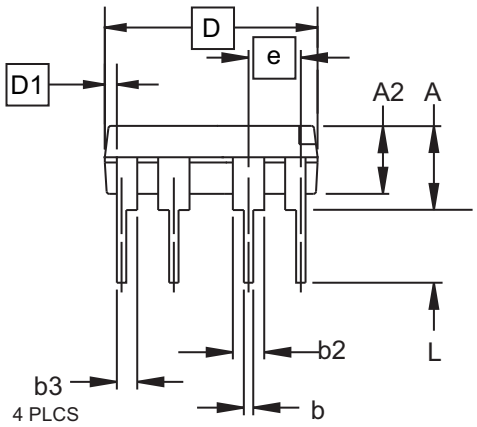
12.1 8P3 – PDIP



Top View



End View



Side View

COMMON DIMENSIONS
(Unit of Measure = inches)

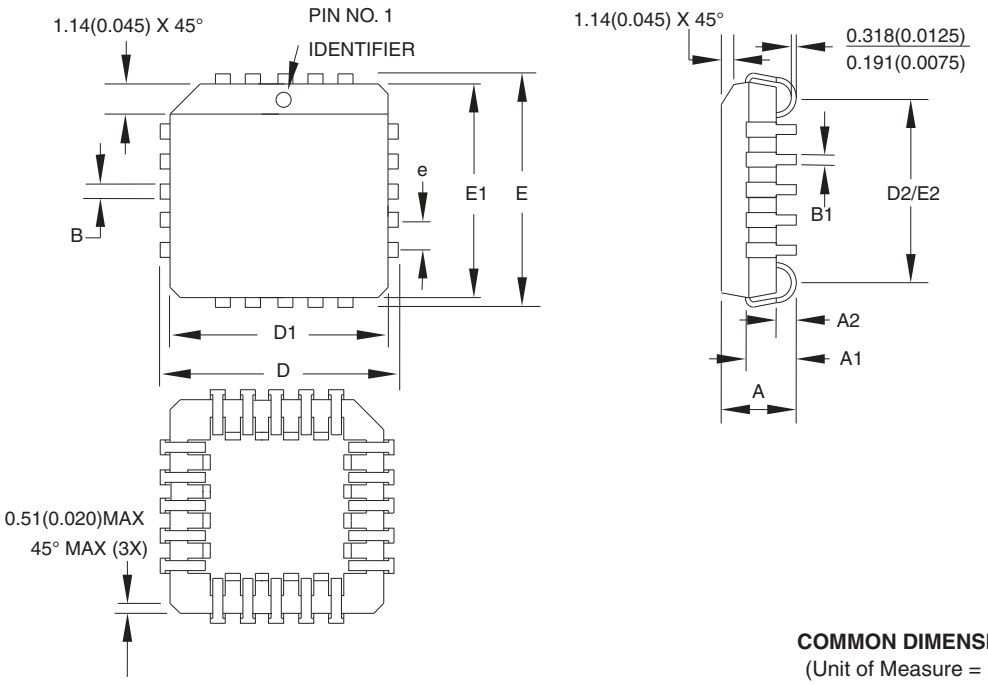
SYMBOL	MIN	NOM	MAX	NOTE
A			0.210	2
A2	0.115	0.130	0.195	
b	0.014	0.018	0.022	5
b2	0.045	0.060	0.070	6
b3	0.030	0.039	0.045	6
c	0.008	0.010	0.014	
D	0.355	0.365	0.400	3
D1	0.005			3
E	0.300	0.310	0.325	4
E1	0.240	0.250	0.280	3
e	0.100 BSC			
eA	0.300 BSC			4
L	0.115	0.130	0.150	2

Notes:
1. This drawing is for general information only; refer to JEDEC Drawing MS-001, Variation BA for additional information.
2. Dimensions A and L are measured with the package seated in JEDEC seating plane Gauge GS-3.
3. D, D1 and E1 dimensions do not include mold Flash or protrusions. Mold Flash or protrusions shall not exceed 0.010 inch.
4. E and eA measured with the leads constrained to be perpendicular to datum.
5. Pointed or rounded lead tips are preferred to ease insertion.
6. b2 and b3 maximum dimensions do not include Dambar protrusions. Dambar protrusions shall not exceed 0.010 (0.25 mm).

06/21/11

Atmel Package Drawing Contact: packagedrawings@atmel.com	TITLE 8P3, 8-lead, 0.300” Wide Body, Plastic Dual In-line Package (PDIP)	GPC PTC	DRAWING NO. 8P3	REV. D

12.2 20J – PLCC



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	4.191	–	4.572	
A1	2.286	–	3.048	
A2	0.508	–	–	
D	9.779	–	10.033	
D1	8.890	–	9.042	Note 2
E	9.779	–	10.033	
E1	8.890	–	9.042	Note 2
D2/E2	7.366	–	8.382	
B	0.660	–	0.813	
B1	0.330	–	0.533	
e	1.270 TYP			

Notes:
1. This package conforms to JEDEC reference MS-018, Variation AA
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .010"(0.254mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
3. Lead coplanarity is 0.004" (0.102mm) maximum

10/04/01

Atmel	Package Drawing Contact: packagedrawings@atmel.com	TITLE	DRAWING NO.	REV.
		20J, 20-lead, Plastic J-leaded Chip Carrier (PLCC)	20J	B

13. Revision History

Rev. No.	Date	History
2322I	10/2014	The AT17LV65A, AT17LV128A, and AT17LV256A are not recommended for new designs. Removed the commercial and TQFP options. Updated the 8P3 package outline drawing, ordering code details, ordering code table, document's template, Atmel logos, disclaimer page.

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