TPS7A63xxEVM Evaluation Module

1 Introduction

The Texas Instruments TPS7A63xxQPWP EVM evaluation module (EVM) helps designers evaluate the operation and performance of the TPS7A63xxQPWP linear regulator.

The EVM contains one linear regulator (see Table 1).

Table 1. Device and Package Configurations

CONVERTER	IC	PACKAGE
U1	TPS7A63xxQPWPRQ1(1)	PWP-14

(1) where xx is 01 for adjustable output voltage, 33 for 3.3V output and 50 for 5.0V output.

2 Setup

This section describes the jumpers and connectors on the EVM as well and how to properly connect, set up and use the TPS7A63xxQPWP EVM.

2.1 Input/Output Connector Description

VBAT is the protected power input for the regulator. The test point provides a power (Vbat) connection and a reverse battery protection diode to allow the user to power the EVM.

GND is the ground return for the regulator. The EVM provides four GND test points to allow the user to power the EVM, connect the load and attach an oscilloscope ground lead.

VOUT is power output for the regulator. The test point provides a connection to attach a load to the EVM.

The TPS7A6301QPWP EVM is setup to provide a 5V output voltage, but the feedback resistors can be changed to set the output voltage to a value between 2.5V and 7V using Equation 1

Feedback Resistor Calculation

$$V_{OUT} = 1.23 * (1 + \frac{R5}{R4}) \quad (1)$$

The TPS7A6333QPWP has a fixed outputvoltage of 3.3V without external resistors. R4 and R5 are not populated on the TPS7A6333QPWP EVM.

The TPS7A6350QPWP has a fixed outputvoltage of 5.0V without external resistors. R4 and R5 are not populated on the TPS7A6350QPWP EVM.

EN is a test point to monitor the Enable input to the device. It can also be used to provide an enable signal to the device from an outside source, if the EN jumper is left open. The EN jumper will disable the regulator when removed and enable the regulator when installed.

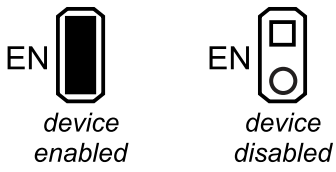

Figure 1. Enable Jumper

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nRST is test point to monitor the reset output pin. It is going to a high-level after power-up and the set DELAY, and is only triggered for a low-pulse in case of an undervoltage-condition on Vout.

DELAY Jumper allows selection of the reset delay timer using an external capacitor (CDLY) to ground. Connecting more jumpers adds the respective delay times.

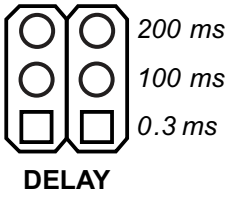

Figure 2. Delay Jumper

WD_EN This Jumper enables the watchdog. With the Jumper installed it is disabled, open is enabled.

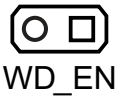

Figure 3. Watchdog-Enable Jumper

WD is the Service pin to provide a trigger signal to the Watchdog-timer. The left pin is connected to GND, the right pin can be connected to a signal generator.

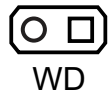

Figure 4. Watchdog-Service Pin

The Watchdog needs to get serviced with a frequency calculated per Equation 2:

$$t_{WD} = 10\text{-}6 \; x \; R_{OSC} = 5000 \; x \; 1/f_{OSC}$$

$$t_{WD\_HOLD} = 3x \; t_{WD\_OUT}$$

$$t_{WD\_OUT} = 1/f_{OSC}$$

$$t_{CW} = t_{OW} = 1/2 \; t_{WD} \quad (2)$$

Where

t_{WD} = width of watchdog window
R_{OSC} = resistor connected at ROSC pin
t_{WD_OUT} = width of fault output
f_{OSC} = frequency of internal oscillator
t_{CW} = width of close window
t_{OW} = width of open window

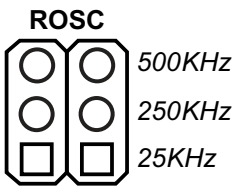

Figure 5. Watchdog-Oscillator Jumper

The frequency set by the ROSC represents the internal clocking of the watchdog. The service frequency needs to be ~3500 times lower. If all jumpers are left open, the device defaults to approximately 30kHz.

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The options given by the EVM (changing resistors gives more) are listed in Table 2, indicating the range of the service-frequency.

Table 2. Watchdog Setting

SETTING (kHz)	ROSC (kΩ)	SERVICE FREQUENCY MIN (Hz)	SERVICE FREQUENCY MAX (Hz)
25.0	200	6	9
250.0	20	60	90
500.0	10	120	180
Open Jumper	open	7	12

WD_FLT is the output of the watchdog. If properly triggered, it stays high. If not or improperly triggered, it will provide a low-pulse. The duration of the pulse equals 1/fOSC and can be used to verify the internal clock frequency. If the jumpers are changed on ROSC, a power-cycle is required, since their value is only recognized during power-up.

2.2 Setup

The input voltage range for the converter is (V_{OUT} + 0.3V) volts to 40 volts. The EVM can support up to 300mA of load current.

2.3 Operation

The TPS7A63xxQPWP will power-up after the V_{BAT} voltage has exceeded the Power-On Reset threshold.

In this configuration, the device will power up when power is applied.

3 Board Layout

Figure 6, Figure 7, and Figure 8 show the board layout for the TPS7A63xxQPWP EVM PCB.

The PowerPAD™ package offers an exposed thermal pad to enhance thermal performance. This must be soldered to the copper landing on the PCB for optimal performance. The PCB provides 2 oz copper planes on the top and bottom to dissipate heat.

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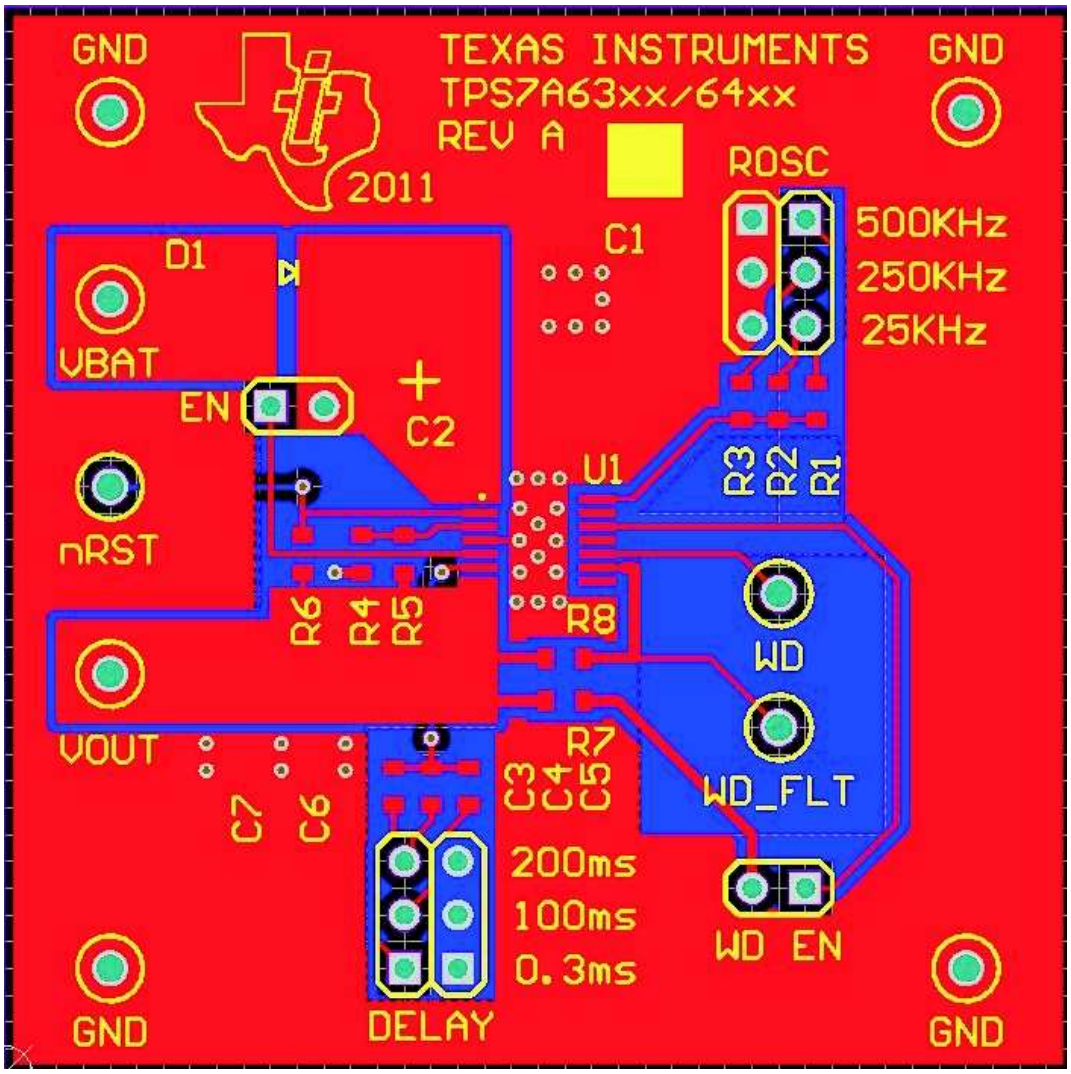

Figure 6. Top Assembly Layer

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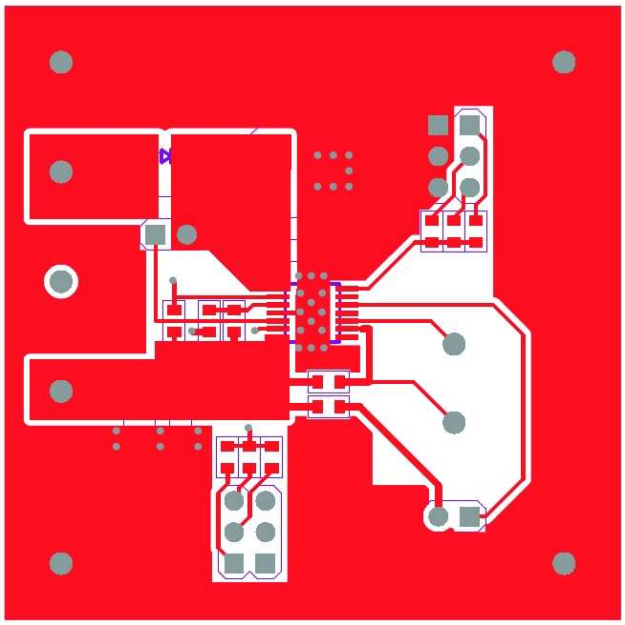

Figure 7. Top Layer Routing

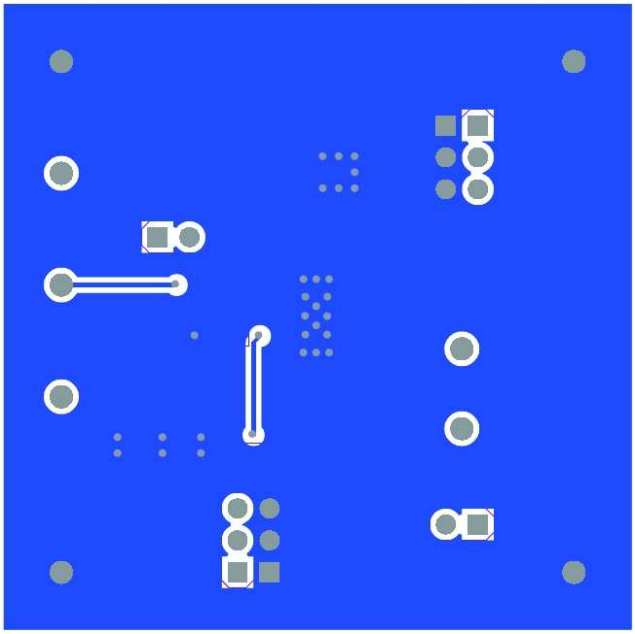

Figure 8. Bottom Layer Routing

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4 Schematic and Bill of Materials

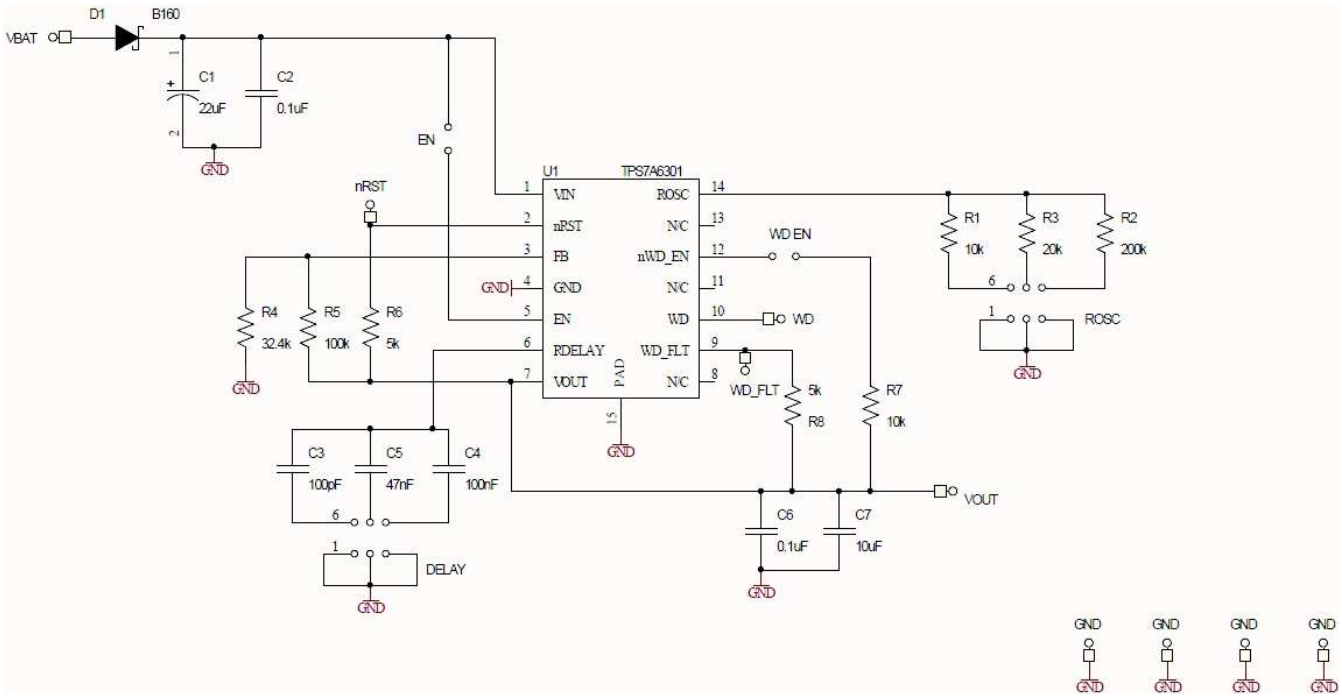

Figure 9. TPS7A63xxQPWP EVM Schematic

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Table 3. Bill of Materials

COUNT	REF DES	DESCRIPTION	SIZE	MFR	PART NUMBER
1	C1	Capacitor, electrolytic, 22uF, 50V	6.3mm x 5.8mm	Panasonic	EEV-FK1H220P
2	C2, C6	Capacitor, ceramic, 0.1uF, 50V, 10%	603	muRata	GCM188R71H104KA57
1	C7	Capacitor, ceramic, 10uF, 16V, 10%	1206	muRata	GRM31CR71C106KAC7
1	C3	Capacitor, ceramic, 100pF, 50V, 5%	603	muRata	GCM1885C1H101JA16
1	C5	Capacitor, ceramic, 33nF, 50V, 10%	603	muRata	GRM188R71H333KA61
1	C4	Capacitor, ceramic, 68nF, 50V, 10%	603	muRata	GRM188R71H683KA93
1	D1	Diode, Schottky, 1A, 60V	SMA	Diodes	B160-13-F
8	GND (x4), nRST, VBAT, VOUT, WD_FLT/	Test point, 52-mil	0.052	Kobiconn	151-103-RC
2	DELAY, ROSC	Header, 6-pin, 100-mil spacing, (36-pin strip)	0.100 x 3	Sullins	PEC03DAAN
3	EN, WD_EN, WD_FLT	Connector jumper, shorting, 100-mil spacing	0.1	Sullins	SPC02SYAN
2	R1, R7	Resistor, chip, 10-kΩ, 1/10W, 1%	603	Panasonic	ERJ-3GEYJ103V
1	R2	Resistor, chip, 200-kΩ,1/10W, 1%	603	Panasonic	ERJ-3GEYJ204V
1	R3	Resistor, chip, 20-kΩ,1/10W, 1%	603	Panasonic	ERJ-3EKF2002V
1	R4	Resistor, chip, 32.4-kΩ, 1/10W, 1% (Not Populated on TPS7A6333 EVM and TPS7A6350 EVM)	603	Panasonic	ERJ-3EKF3242V
1	R5	Resistor, chip, 100-kΩ, 1/10W, 1% (Not Populated on TPS7A6333 EVM and TPS7A6350 EVM)	603	Panasonic	ERJ-3GEYJ104V
2	R6, R8	Resistor, chip, 4.99-kΩ, 1/10W, 1%	603	Panasonic	ERJ-3EKF4991V
1	R9	do not populate			
1	U1	IC, TPS7A63xxQPWPQ1		TI	TPS7A63xxQPWPQ1
	-	PCB, 2-inch x 2-inch x 0.062		Any	TPS7A63xx_64xx, REV A

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EVM Warnings and Restrictions

It is important to operate this EVM within the input voltage range of 4 V to 40 V and the output voltage range of 5 V .

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 85°C. The EVM is designed to operate properly with certain components above 60°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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