



HARRIS

IRFF9120, IRFF9121 IRFF9122, IRFF9123

**Avalanche Energy Rated
P-Channel Power MOSFETs**

January 1994

Features

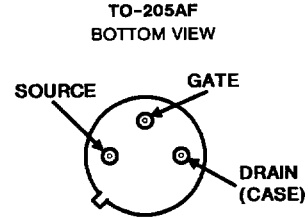
- -3.5A and -4A, -80V and -100V
- $r_{DS(ON)} = 0.60\Omega$ and 0.80Ω
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

Description

The IRFF9120, IRFF9121, IRFF9122 and IRFF9123 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are p-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

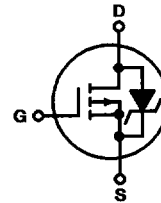
The IRFF types are supplied in the JEDEC TO-205AF (Low Profile TO-39) metal package.

Package



Terminal Diagram

P-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings ($T_C = 25^\circ\text{C}$) Unless Otherwise Specified

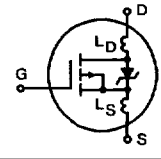
	IRFF9120	IRFF9121	IRFF9122	IRFF9123	UNITS	
Drain-Source Voltage (1)	V_{DS}	-100	-80	-100	-80	V
Drain-Gate Voltage ($R_{GS} = 20k\Omega$) (1)	V_{DGR}	-100	-80	-100	-80	V
Continuous Drain Current						
$T_C = 25^\circ\text{C}$	I_D	-4	-4	-3.5	-3.5	A
Pulsed Drain Current (3)	I_{DM}	-16	-16	-14	-14	A
Gate-Source Voltage	V_{GS}	± 20	± 20	± 20	± 20	V
Maximum Power Dissipation	P_D	20	20	20	20	W
(See Figure 14)						
Linear Derating Factor		0.16	0.16	0.16	0.16	W/ $^\circ\text{C}$
(See Figure 14)						
Single Pulse Avalanche Energy Rating (4)	E_{AS}	370	370	370	370	mJ
Operating and Storage Junction	T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	$^\circ\text{C}$
Temperature Range						
Maximum Lead Temperature for Soldering	T_L	300	300	300	300	$^\circ\text{C}$
(0.063" (1.6mm) from case for 10s)						

NOTES:

1. $T_J = +25^\circ\text{C}$ to $+150^\circ\text{C}$
2. Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. $V_{DD} = 25\text{V}$, Start $T_J = +25^\circ\text{C}$, $L = 34.7\text{mH}$, $R_G = 25\Omega$, Peak $I_L = 4.0\text{A}$
(See Figures 15 and 16)

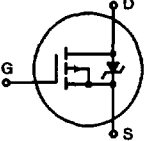
Specifications IRFF9120, IRFF9121, IRFF9122, IRFF9123

Electrical Characteristics $T_C = +25^\circ\text{C}$, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS			UNITS	
			MIN	TYP	MAX		
Drain-Source Breakdown Voltage IRFF9120, IRFF9122	BV _{DSS}	V _{GS} = 0V, I _D = -250μA	-100	-	-	V	
IRFF9121, IRFF9123			-80	-	-	V	
Gate Threshold Voltage	V _{GS(TH)}	V _{DS} = V _{GS} , I _D = -250μA	-2.0	-	-4.0	V	
Gate-Source Leakage Forward	I _{GSS}	V _{GS} = -20V	-	-	-100	nA	
Gate-Source Leakage Reverse	I _{GSS}	V _{GS} = 20V	-	-	100	nA	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = Max Rating, V _{GS} = 0V	-	-	-250	μA	
		V _{DS} = Max Rating x 0.8, V _{GS} = 0V, T _C = +125°C	-	-	-1000	μA	
On-State Drain Current (Note 2) IRFF9120, IRFF9121	I _{D(ON)}	V _{DS} > I _{D(ON)} x r _{DS(ON)} Max, V _{GS} = -10V	-4	-	-	A	
			IRFF9122, IRFF9123	-3.5	-	-	A
Static Drain-Source On-State Resistance (Note 2) IRFF9120, IRFF9121	r _{DS(ON)}	V _{GS} = -10V, I _D = -2A	-	0.5	0.6	Ω	
			IRFF9122, IRFF9123	-	0.8	0.8	Ω
Forward Transconductance (Note 2)	g _{fs}	V _{DS} > I _{D(ON)} x r _{DS(ON)} Max, I _D = -2A	1.25	2	-	S(Ω)	
Input Capacitance	C _{ISS}	V _{GS} = 0V, V _{DS} = -25V, f = 1.0MHz See Figure 10	-	300	-	pF	
Output Capacitance	C _{OSS}	See Figure 10	-	200	-	pF	
Reverse Transfer Capacitance	C _{RSS}		-	50	-	pF	
Turn-On Delay Time	t _{d(ON)}	V _{DD} = 0.5 BV _{DSS} , I _D = -4A, R _G = 9.1Ω	-	25	50	ns	
Rise Time	t _r	See Figure 17. (MOSFET switching times are essentially independent of operating temperature.)	-	50	100	ns	
Turn-Off Delay Time	t _{d(OFF)}	See Figure 17. (MOSFET switching times are essentially independent of operating temperature.)	-	50	100	ns	
Fall Time	t _f		-	50	100	ns	
Total Gate Charge (Gate-Source + Gate-Drain)	Q _g	V _{GS} = -10V, I _D = -4A, V _{DS} = 0.8 Max Rating. See Figure 18 for test circuit. (Gate charge is essentially independent of operating temperature.)	-	16	22	nC	
Gate-Source Charge	Q _{gs}	(Gate charge is essentially independent of operating temperature.)	-	9	-	nC	
Gate-Drain ("Miller") Charge	Q _{gd}		-	7	-	nC	
Internal Drain Inductance	L _D	Measured from the drain lead, 5mm (0.2") from header to center of die.	Modified MOSFET symbol showing the internal device inductances. 	-	5.0	-	nH
Internal Source Inductance	L _S	Measured from the source lead, 5mm (0.2") from header to source bonding pad.		-	15	-	nH
Junction-to-Case	R _{θJC}		-	-	6.25	°C/W	
Junction-to-Ambient	R _{θJA}	Typical socket mount	-	-	175	°C/W	

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Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I _S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	-	-	-4	A
Pulse Source Current (Body Diode) (Note 3)	I _{SM}		-	-	-16	A
Diode Forward Voltage (Note 2)	V _{SD}	T _C = +25°C, I _S = -4A, V _{GS} = 0V	-	-	-1.5	V
Reverse Recovery Time	t _{rr}	T _J = +150°C, I _F = 4A, dI _F /dt = 100A/μs	-	230	-	ns
Reverse Recovered Charge	Q _{RR}	T _J = +150°C, I _F = -4A, dI _F /dt = 100A/μs	-	1.3	-	μC
Forward Turn-on Time	t _{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L _S + L _D .	-	-	-	-

NOTES: 1. T_J = +25°C to +150°C
 2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
 3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
 4. V_{DD} = 25V, Start T_J = +25°C, L = 34.7mH, R_G = 25Ω, Peak I_L = 4A (See Figures 15 and 16)

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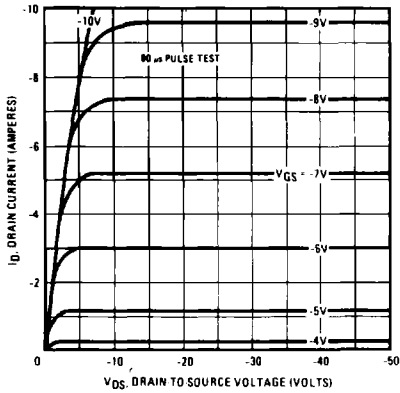


Fig. 1 - Typical output characteristics.

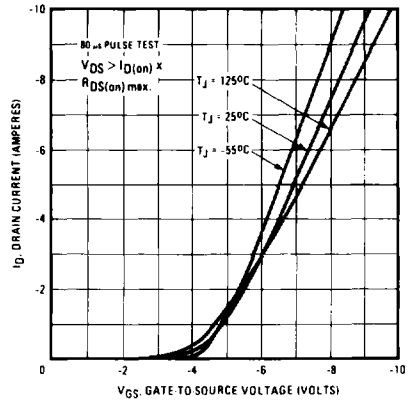


Fig. 2 - Typical transfer characteristics.

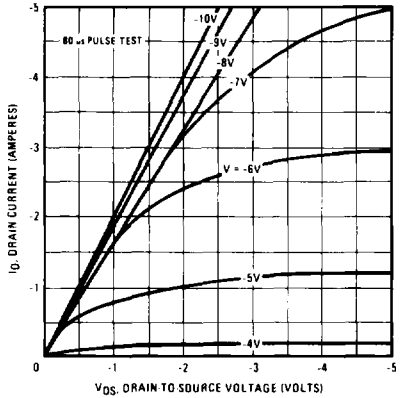


Fig. 3 - Typical saturation characteristics.

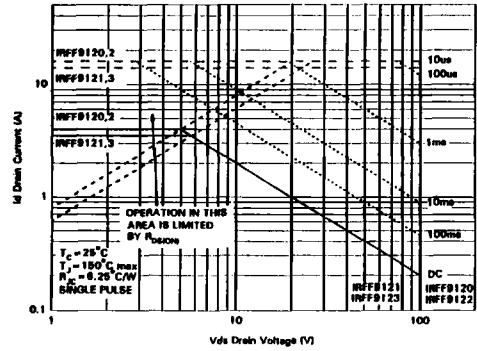


Fig. 4 - Maximum safe operating area.

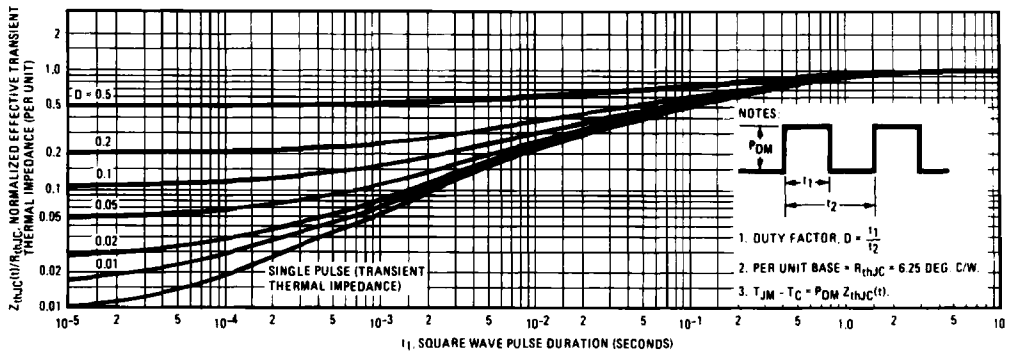


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

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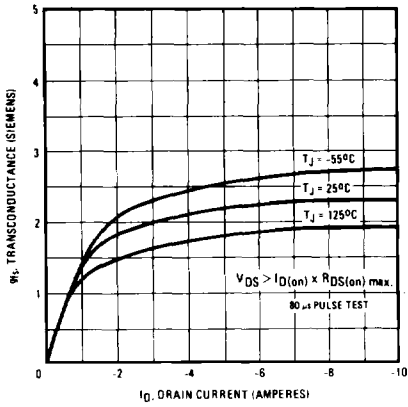


Fig. 6 - Typical transconductance vs. drain current.

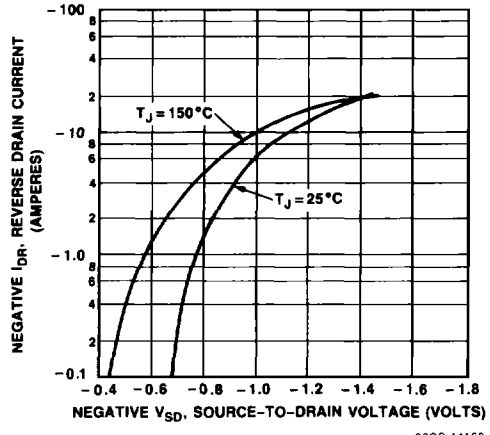


Fig. 7 - Typical source-drain diode forward voltage.

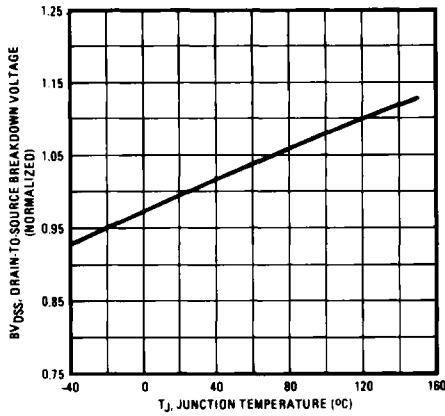


Fig. 8 - Breakdown voltage vs. temperature.

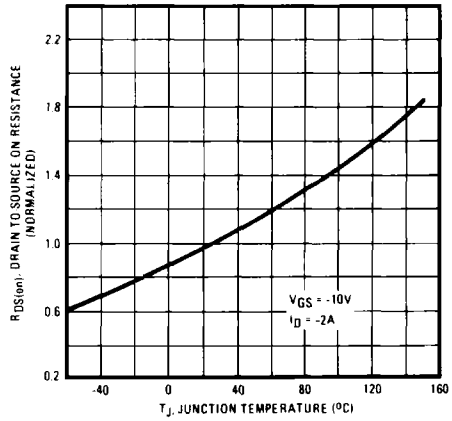


Fig. 9 - Normalized on-resistance vs. temperature.

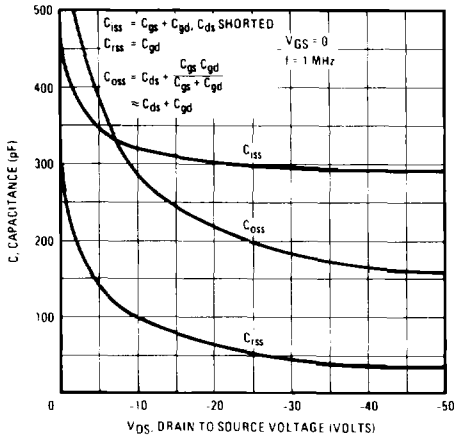


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

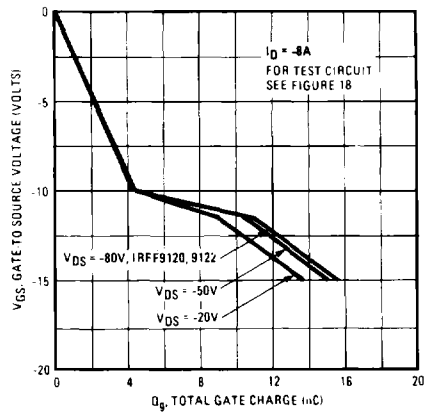


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

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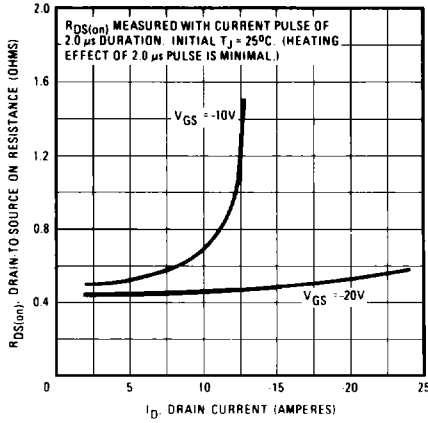


Fig. 12 - Typical on-resistance vs. drain current.

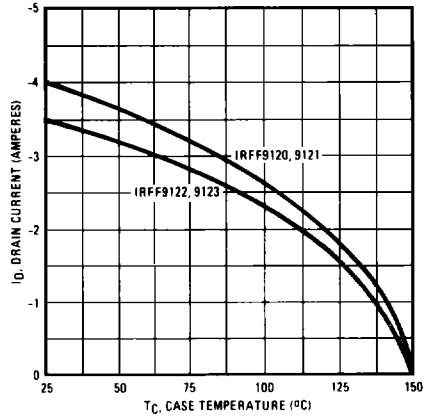


Fig. 13 - Maximum drain current vs. case temperature.

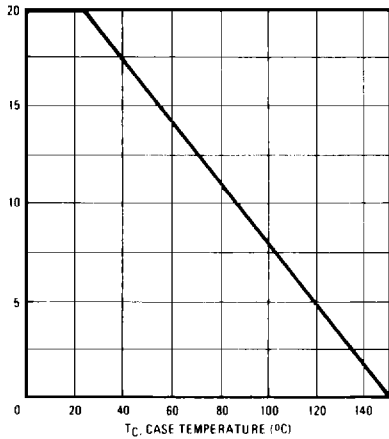


Fig. 14 - Power vs. temperature derating curve.

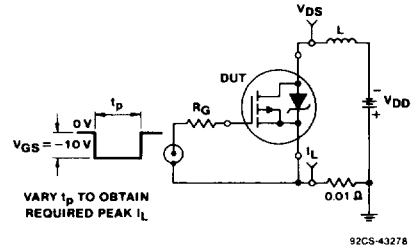


Fig. 15 - Unclamped inductive test circuit.

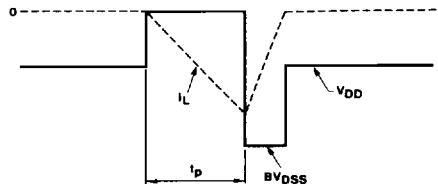


Fig. 16 - Unclamped inductive waveforms.

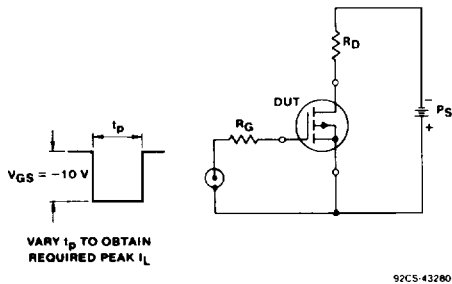


Fig. 17 - Switching time test circuit.

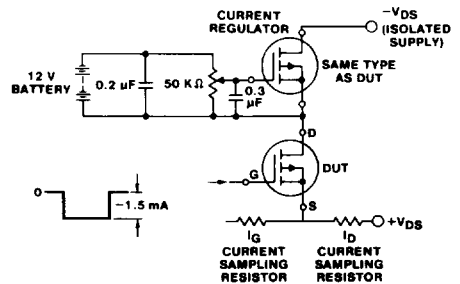


Fig. 18 - Gate charge test circuit.