# TLE9855QX Evaluation Kit User Manual

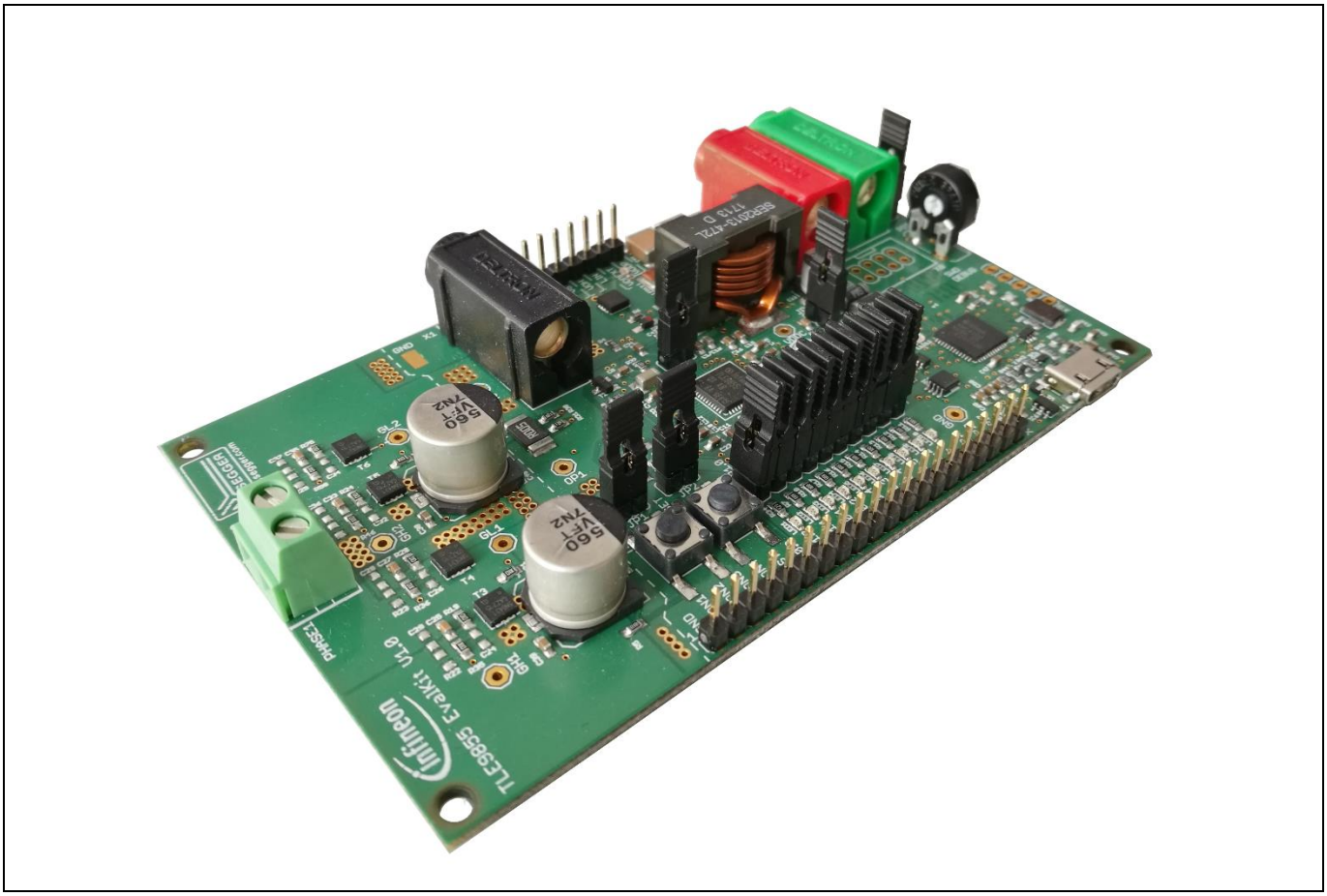

**Figure 1 TLE9855QX Evaluation Kit**

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# 1 Concept

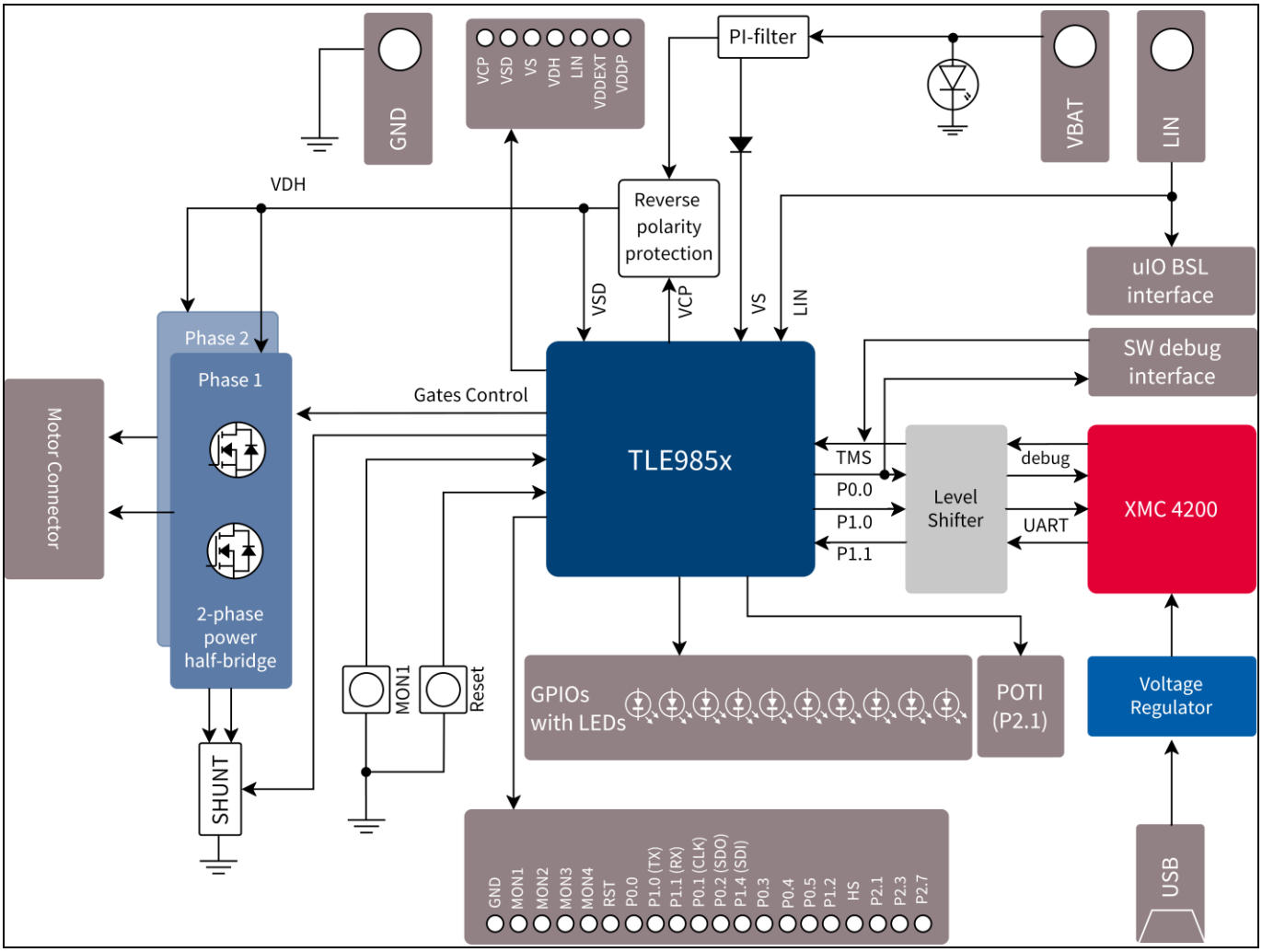


**Figure 2 Board Concept**

This board is intended to provide a simple, easy-to-use tool for getting familiar with Infineon's Embedded Power H-Bridge driver IC. It contains the TLE9855QX and its typical application circuit. This includes two MOSFET half bridges to drive a DC motor.

The MOSFET halfbridges have a scew terminal to directly connect a DC motor to the Evalkit.

GPIOs and MON PINs are accessable through pin headers at the edge of the board. Two push buttons trigger a PIN reset or a MON1-Input. A Potentiometer is connected to one ADC input.

The evaluation board can be supplied via 4mm banana jacks. An on-board Segger J-Link (XMC4200) provides a SWD interface and a virtual COM port, which can be used for serial communication with the board.

A battery LED indicates power supply connection. Typically, the board is supplied by 12V. An applied reverse polarity protection circuit secures the board from damage.

# 2 Interconnects

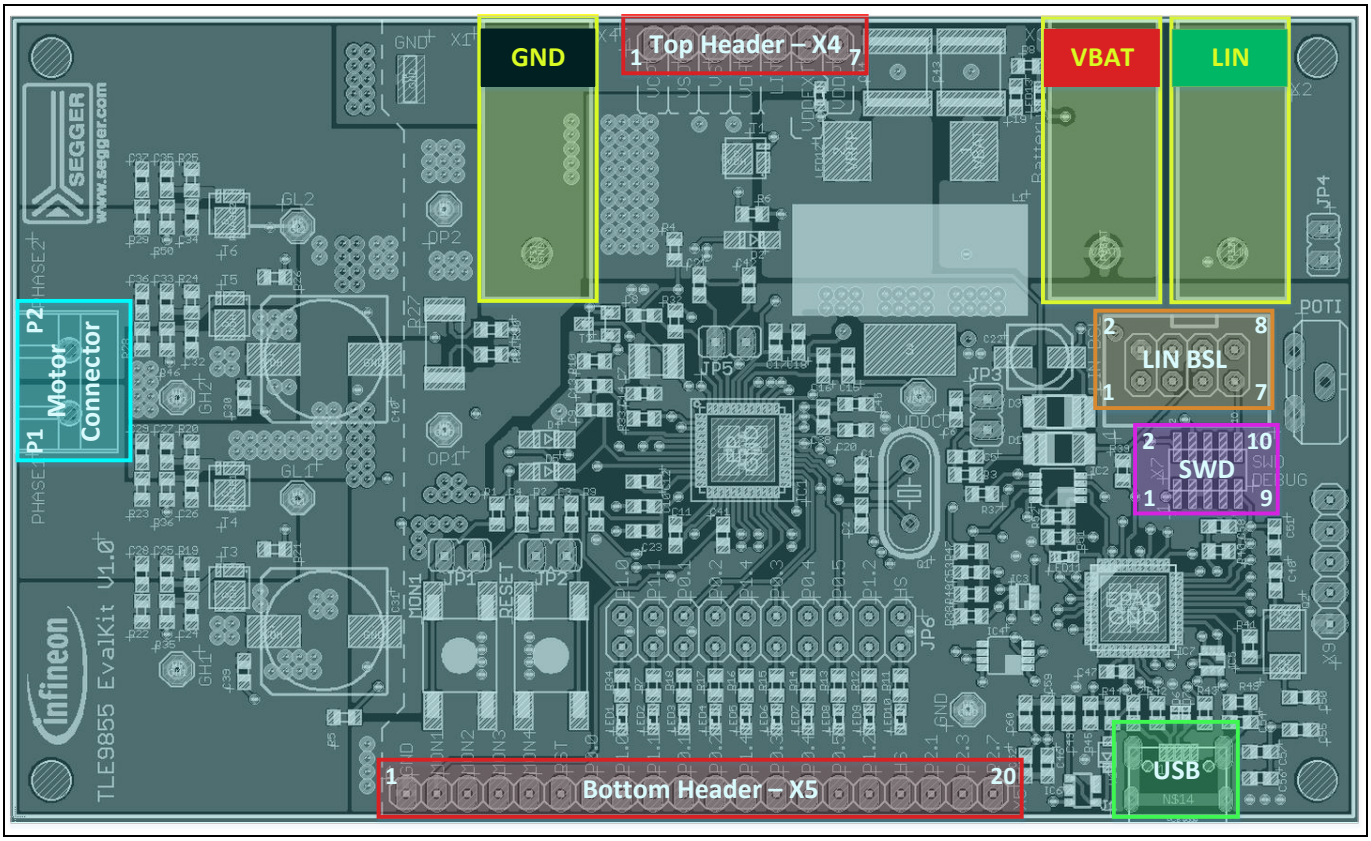


**Figure 3 Interconnects**

**Banana jacks** (marked yellow)

The jacks have different colors for GND (black), VBAT (red) and LIN (green).

**Top Pin Header X4 and Bottom Pin Header X5** (marked red)

Soldering pin headers with 2,54mm pitch for X4 (1x7) and X5(1x20) yields test points for the TLE9855QX pins. Following signals are connected to the pins:

**Table 1 Top Pin Header X4 Pinout**

| 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|
| VCP | VSD | VS | VDH | LIN | VDDEXT | VDDP |

**Table 2 Bottom Pin Header X5 Pinout**

| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 |
|---|---|---|---|---|---|---|---|---|---|
| GND | MON1 | MON2 | MON3 | MON4 | RST | P0.0 | P1.0 (TX) | P1.1 (RX) | P0.1 (CLK) |

| 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 |
|---|---|---|---|---|---|---|---|---|---|
| P0.2 (SDO) | P1.4 (SDI) | P0.3 | P0.4 | P0.5 | P1.2 | HS | P2.1 | P2.3 | P2.7 |

**Terminal block for connecting the motor** (marked cyan)

The two pins of the terminal block provide access to the two half bridges and are intended to connect a DC motor.

**USB for UART and Debugging** (marked green)

With this Micro USB PC and evaluation board can get connected.

**uIO BSL Pin Header X8 for LIN** (marked orange)

This uiO bootstrap loader is an 8 pin header (2x4) with 2,54mm pitch. It is intended to connect additional hardware for bootstrap loading. For programming the TLE9855QX via LIN this uIO interface can be used (see www.infineon.com/cms/en/product/evaluation-boards/uio-stick/).

**Table 3 uIO Pin Header X8 Pinout**

| | | | |
|---|---|---|---|
| n.c. | **1** | **2** | GND |
| n.c. | **3** | **4** | n.c. |
| LIN | **5** | **6** | VS |
| RESET | **7** | **8** | n.c. |

**Software Debug (SWD) SMD Pin Header X7** (marked purple)

There is a 10 pin SMD header (2x5) with 1,27mm pitch on the Evaluation Kit. For debugging with another ISP than the on board Segger this interface can be used. DBPRE will be implicity connected to GND by connecting the external ISP. This keeps the XMC4200 in reset state to prevent interferences of the SWD communication.

**Table 4 SWD Pin Header X7 Pinout**

| | | | |
|---|---|---|---|
| 5V | **1** | **2** | SWDIO (TMS) |
| GND | **3** | **4** | SWCLK (P0.0) |
| GND | **5** | **6** | n.c. |
| n.c. | **7** | **8** | n.c. |
| DBPRE | **9** | **10** | RESET |

# 3 Test Points

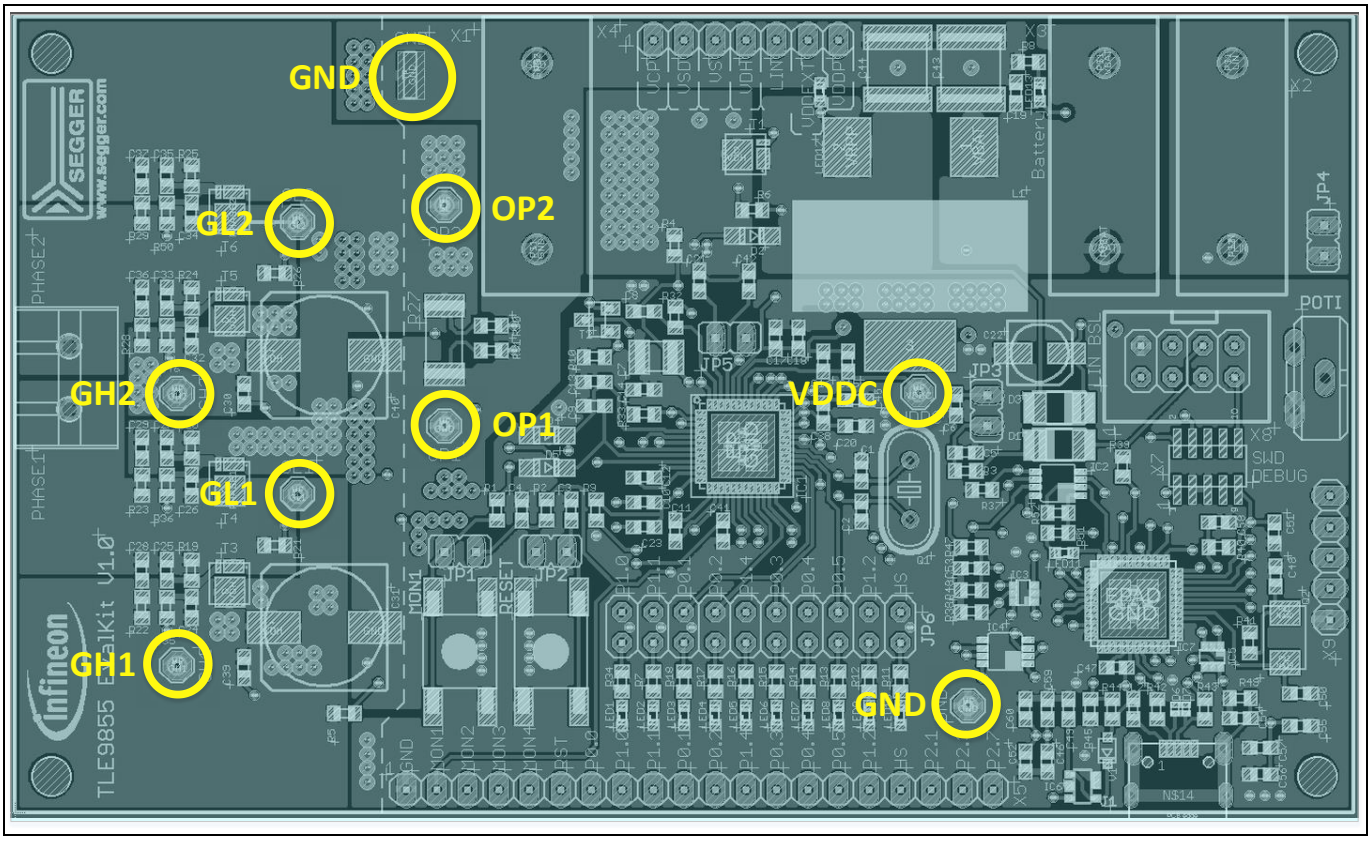


**Figure 4 Test Points**

The 2-phase power half-bridge is controlled by four gate driver pins, driving the gates of High side MOSFET and Low side MOSFET for each phase. Each gate has an intended test point to measure the respective signals at High side gates and Low side gates (GL1, GL2, GH1, GH2).

Test points OP1 and OP2 are provided at both sides of the shunt, which is 5mR.

Additionally there is an intended test point for VDDC and various ground points.

All test points marked in figure 4 except the SMD GND point at the top are not populated. In order to use these pins they have to be soldered in the designated solder holes.

# 4 Jumper Settings

The following table summarizes the jumpers' options. More detailed information can be found in the text below.

**Table 5 Jumpers' functionalities**

| | |
|---|---|
| **JP1** | Enable or disable MON1 button |
| **JP2** | Enable or disable RESET button |
| **JP3** | Select TLE9855QX as LIN Master or LIN Slave |
| **JP4** | Enable or disable POTI |
| **JP5** | Replace by an ampere meter to measure input current |
| **JP6** | Enable or disable LED for respective GPIO |

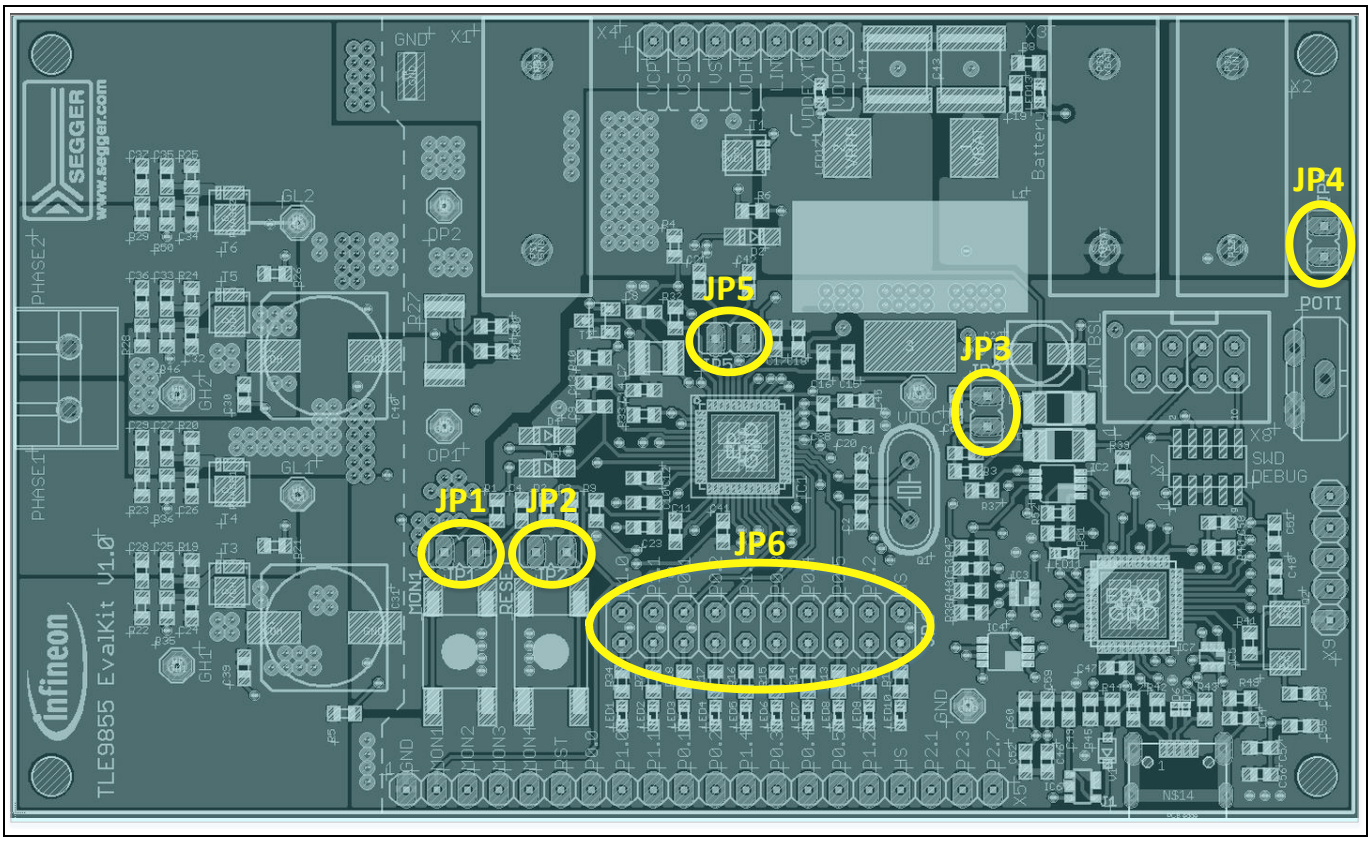


**Figure 5 Jumpers**

**JP1:** Close this jumper to connect MON1 button to MON1 input. Open it to disconnect MON1 button from MON1 input.

**JP2:** Close this jumper to connect RESET button to RESET input. Open it to disconnect RESET button from RESET input.

**JP3:** Close this jumper to connect an additional 1k pull-up resistor. This is intended for LIN master communication. Open the jumper to use the TLE9855QX as slave in a LIN network. Software for LIN low level driver can be found at on the IHR website.

**JP4:** Close this jumper to connect the 10k potentiometer to P2.1. Open this jumper to disconnect the potentiometer.

**JP5:** This jumper is closed by default. If this jumper is left open the device is not supplied. It is intended to open the VS line in order to measure the current flowing into the TLE9855QX.

**JP6:** Jumper 6 provides one individual jumper per LED in order to connect or disconnect the respective LED to the pin port.

**Table 6 Combinations of GPIOs and LEDs**

| P1.0 | P1.1 | P0.1 | P0.2 | P1.4 | P0.3 | P0.4 | P0.5 | P1.2 | HS |
|---|---|---|---|---|---|---|---|---|---|
| LED1 | LED2 | LED3 | LED4 | LED5 | LED6 | LED7 | LED8 | LED9 | LED10 |

# 5 Communication Interfaces

## 5.1 LIN (via banana jack an uIO BSL)

The device integrated LIN transceiver is connected to a banana jack and additionally to the uIO BSL interface. To integrate the device in a LIN network it is sufficient to use the single wire banana interface. The BSL interface is intended to program the device via LIN. For further information about the uIO interface see www.infineon.com/cms/en/product/evaluation-boards/uio-stick/.

## 5.2 UART (via USB)

A virtual COM port provided by Segger driver enables a PC – board – communication via UART. The UART2 module of TLE9855QX uses the pins P1.0 (transmit) and P1.1 (receive). Those are connected to the XMC4200, which emulates RX and TX on PC side with Segger firmware. Though they cannot be disconnected physically, bidirectional level shifters ensure that the XMC pins are hi-Z in case the virtual COM port is not used.

By connecting the evaluation board to the PC a virtual COM port gets emulated by the Segger driver automatically. The port used will show up in the Microsoft® Windows® device manager.

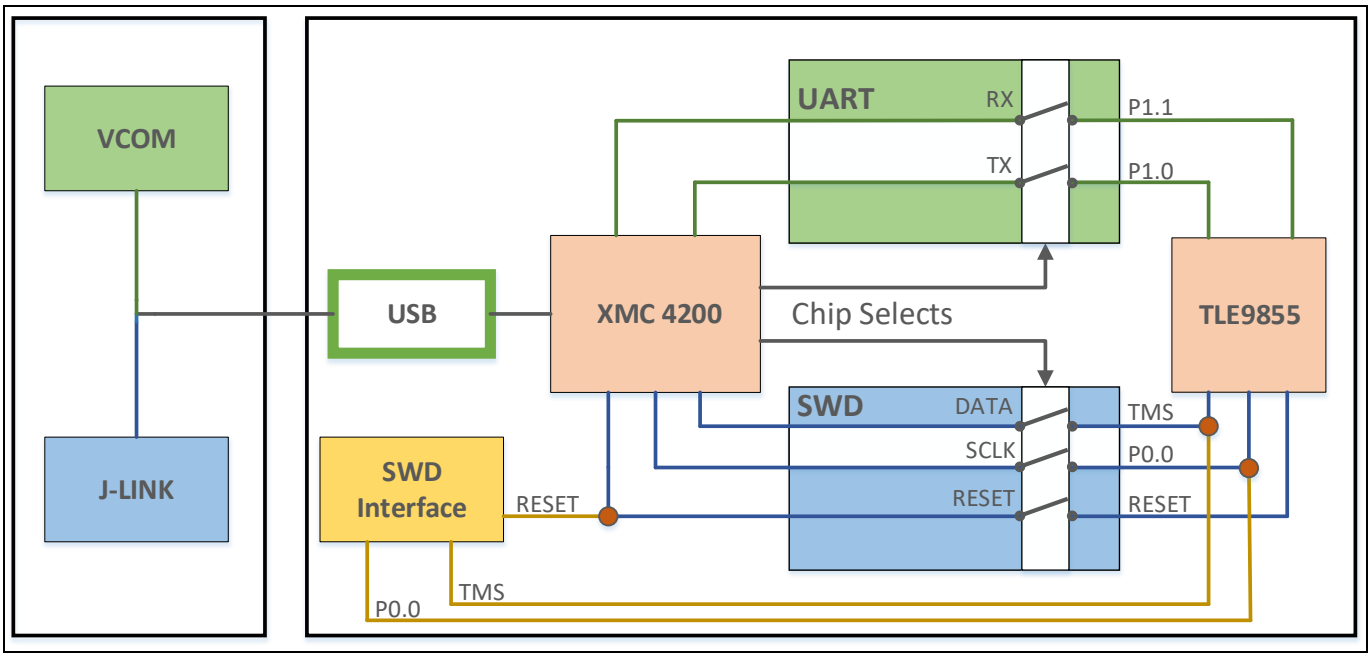


**Figure 6 UART and Debugging**

*Note: Only one of the interfaces USB or SWD can be used at one time. While using the SWD interface the XMC is hold in reset. As long as a debugger is connected with the SWD interface it eliminates therefore debugging or UART via USB.*

## 5.3 Debugging (via USB or SWD Interface)

For serial wire debug the TLE9855QX uses the pins TMS (data) and P0.0 (clock). Level shifters between XMC4200 and TLE9855QX allow using P0.0, while it is not used for debugging.

The Segger J-Link module on board allows serial wire debugging via USB. Alternative debugging via SWD interface is possible to debug with another ISP than the onboard Segger e.g. U-Link2. Therefore the signals are routed through the 10 pin header SWD interface between the XMC4200 and the TLE9855QX. The pin

configuration makes sure that the XMC is hold in reset while another debugger is physically connected as DBPRE will be implicitly connected to GND by connecting the external ISP (see Table 5).

Information regarding the software installation for editor, compiler and debugger can be found on Infineon website .

# 6 Technical Data

Platine Size: (110x66) mm

Voltage Supply: 5,5 V (min.) to 28,0 V (max.)

Motor Current: max. 10A

Pin Ports: 5V (GPIOs of TLE9855QX)

# 7 Optional Additional Placements

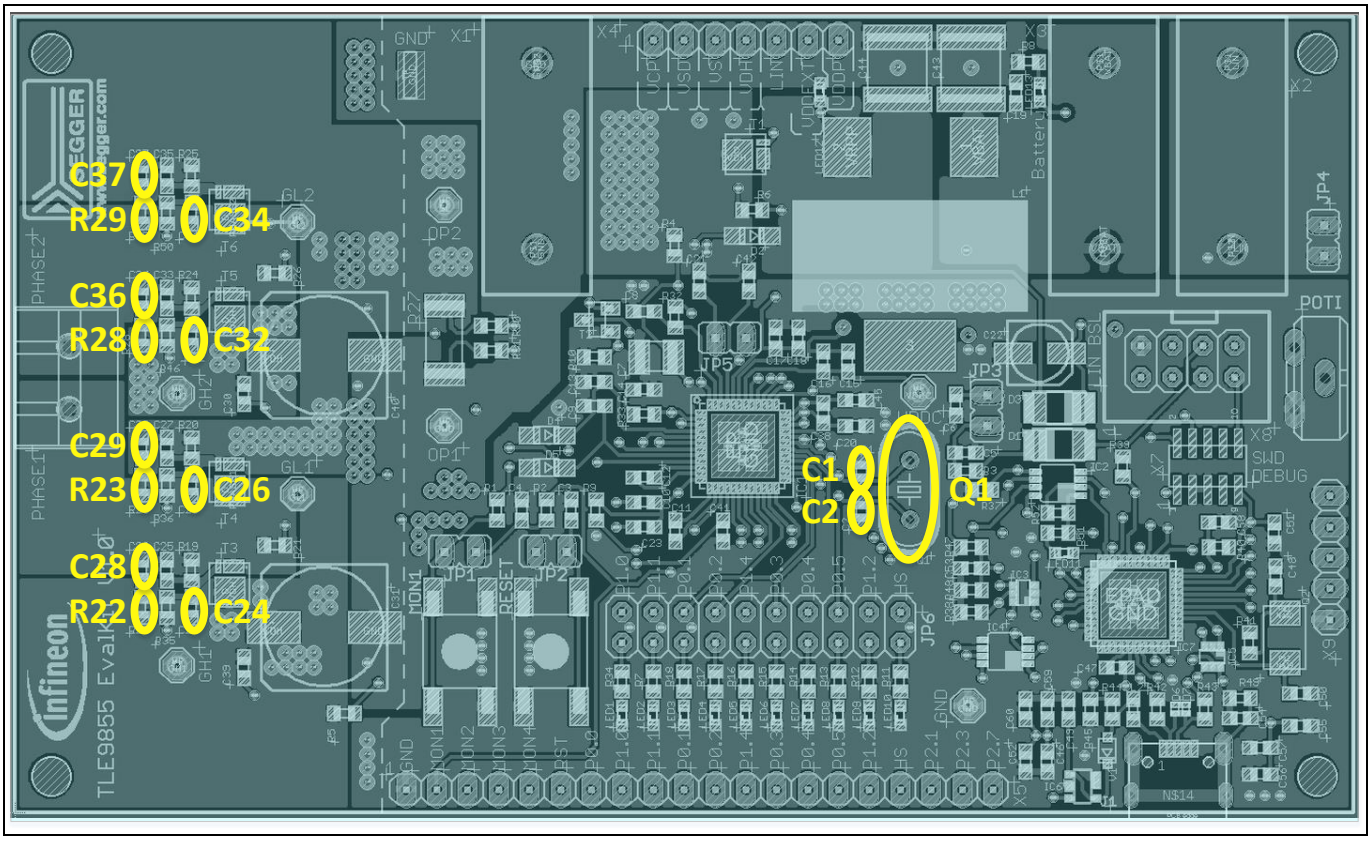


**Figure 7 Additional Placements' positions**

Values for these optional additional placements have to be determined depending on application.

**Table 7 Additional Placements**

| Name | Purpose | Possible Value |
|---|---|---|
| Q1 | External Oscillator | - |
| C1 | Oscillator Capacity | - |
| C2 | Oscillator Capacity | - |
| R22 | Resistance Snubber High side MOSFET Phase 1 | 2 R |
| C28 | Capacity Snubber High side MOSFET Phase 1 | 10 nF |
| C24 | Gate-Drain-Capacity High side MOSFET Phase 1 | 33 pF |
| R23 | Resistance Snubber Low side MOSFET Phase 1 | 2 R |
| C29 | Capacity Snubber Low side MOSFET Phase 1 | 10 nF |
| C26 | Gate-Drain-Capacity Low side MOSFET Phase 1 | 33 pF |
| R28 | Resistance Snubber High side MOSFET Phase 2 | 2 R |
| C36 | Capacity Snubber High side MOSFET Phase 2 | 10 nF |
| C32 | Gate-Drain-Capacity High side MOSFET Phase 2 | 33 pF |
| R29 | Resistance Snubber Low side MOSFET Phase 2 | 2 R |
| C37 | Capacity Snubber Low side MOSFET Phase 2 | 10 nF |
| C34 | Gate-Drain-Capacity Low side MOSFET Phase 2 | 33 pF |

# 8 Schematics and Layout

## 8.1 Schematics

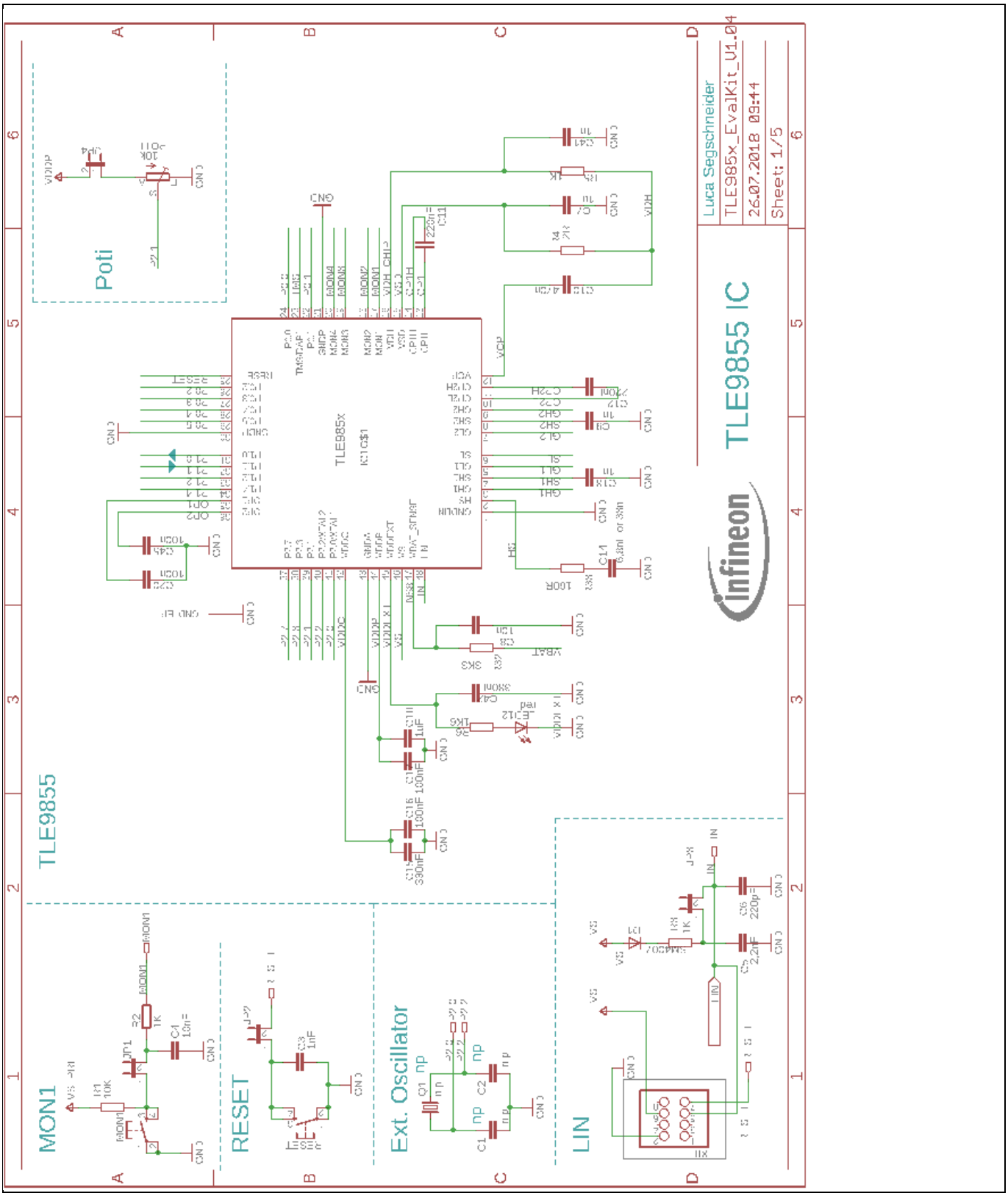


**Figure 8 Schematic Sheet 1**

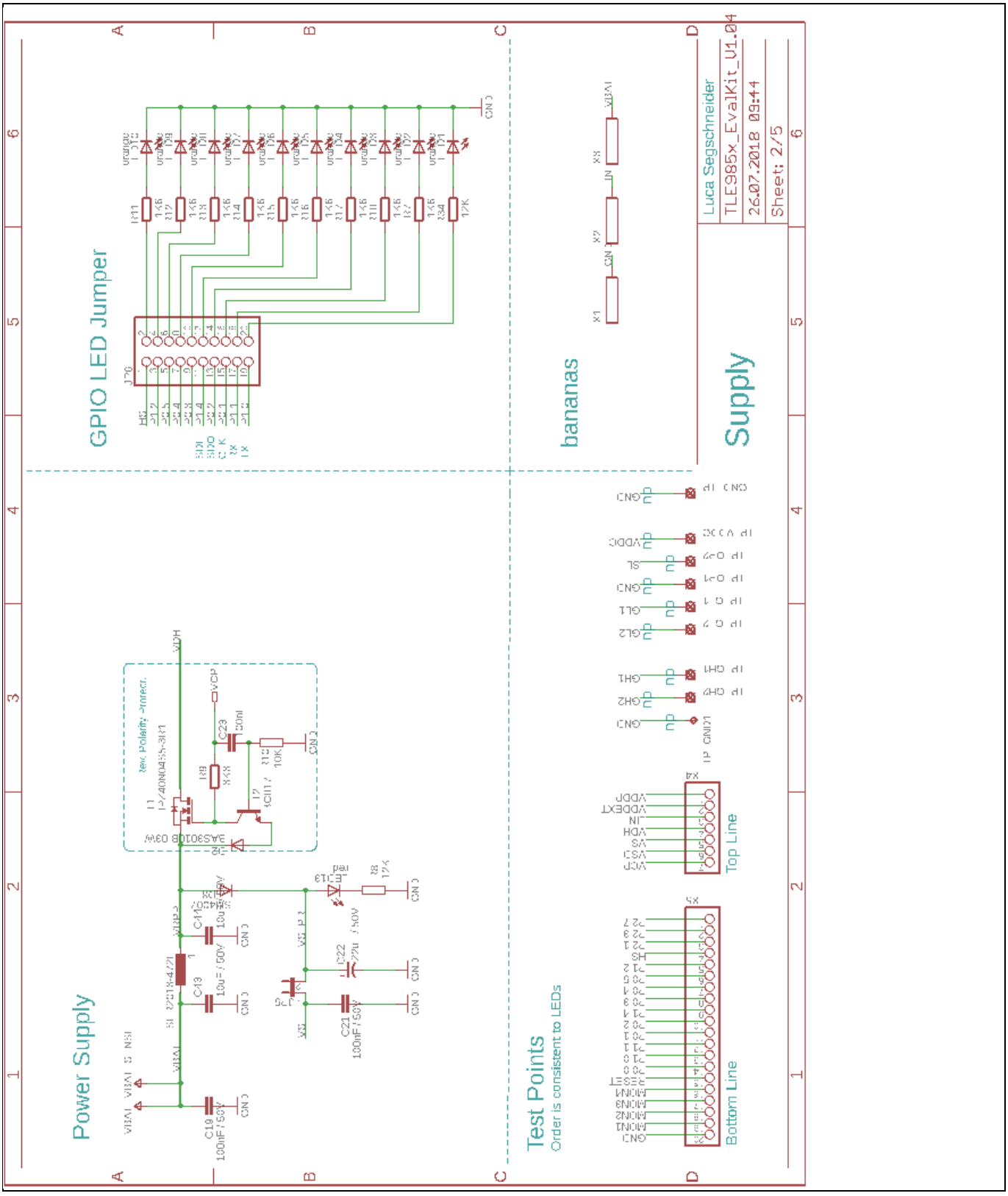


**Figure 9 Schematic Sheet 2**

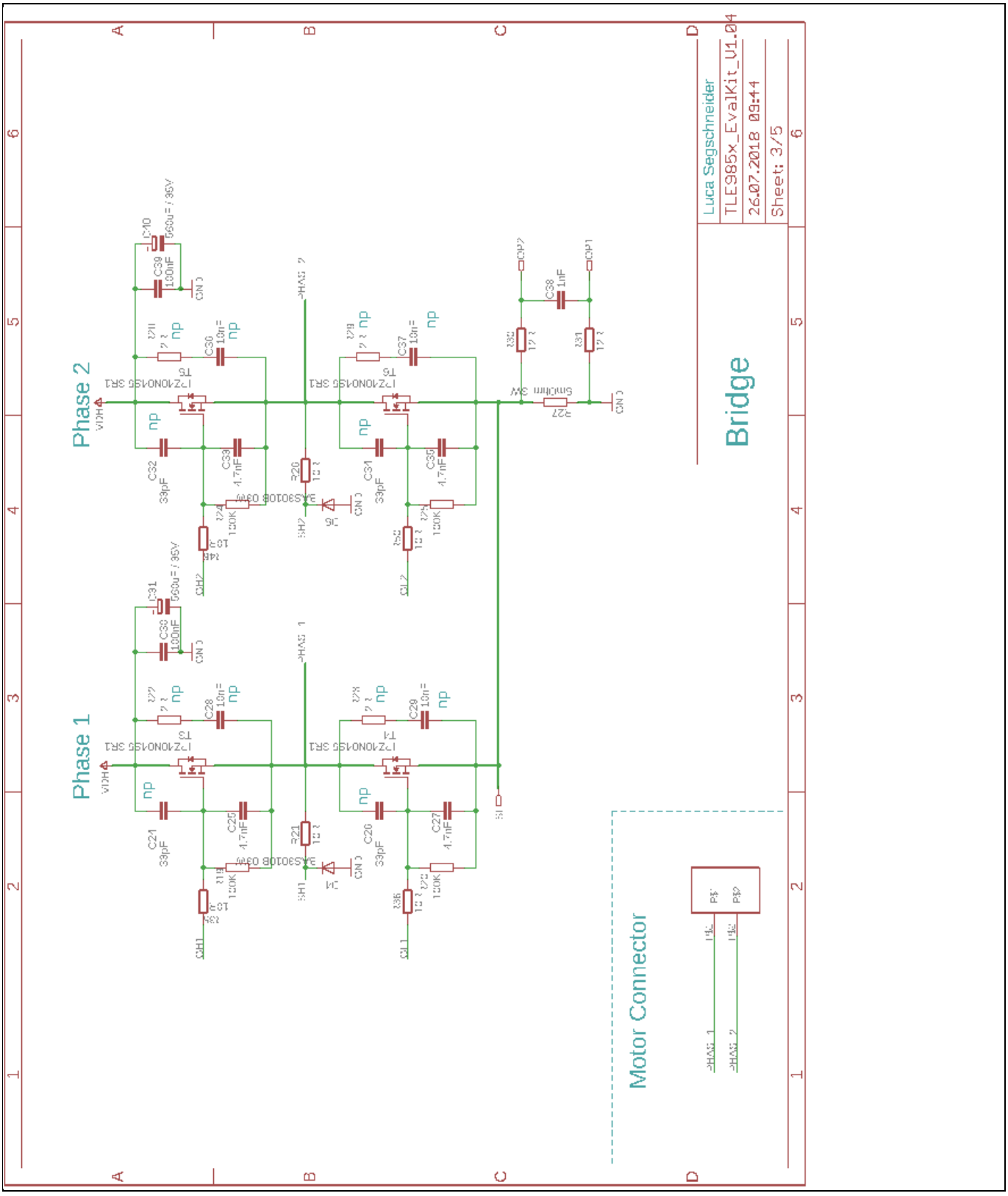


**Figure 10 Schematic Sheet 3**

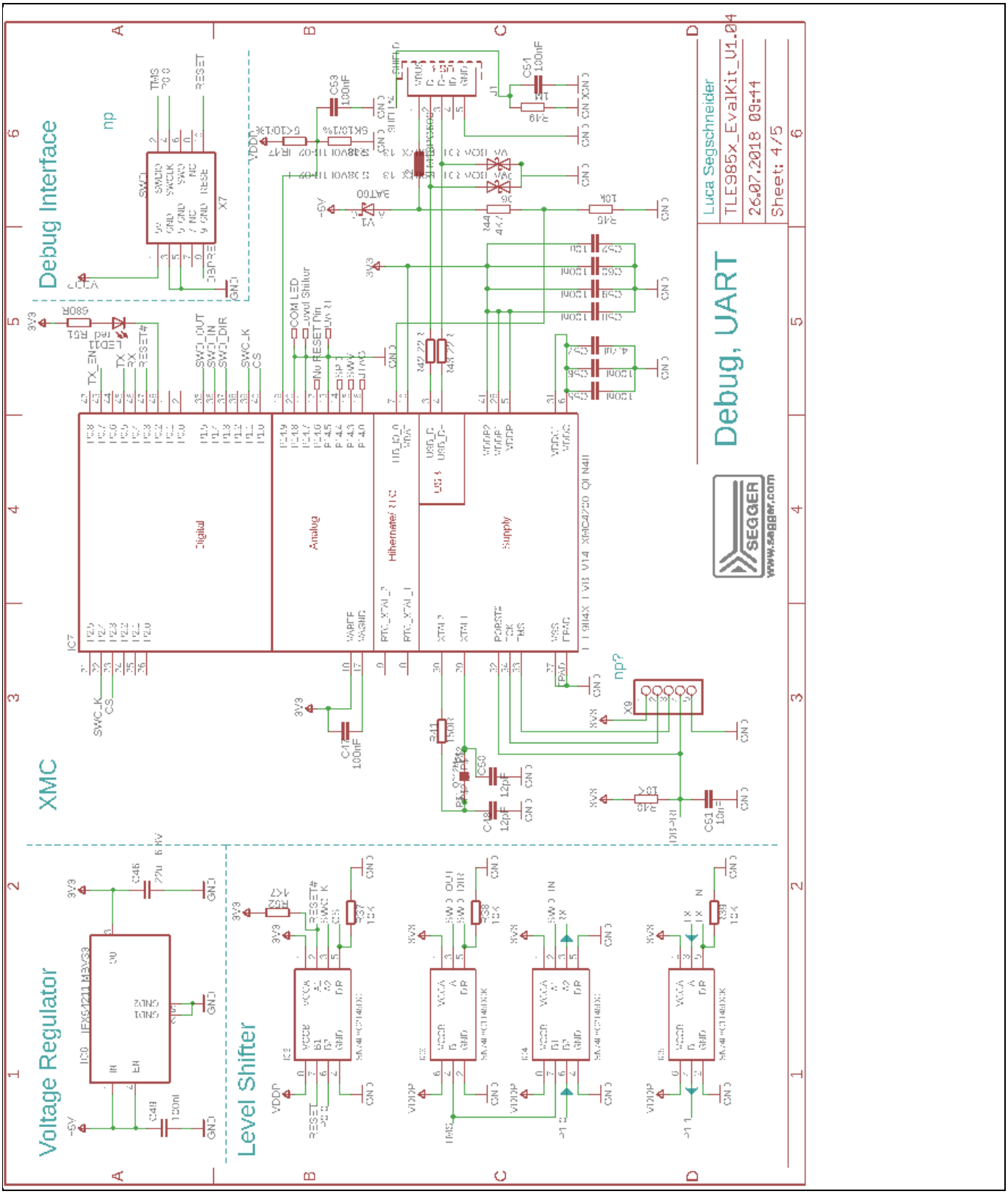


**Figure 11 Schematic Sheet 4**

## 8.2 Layout

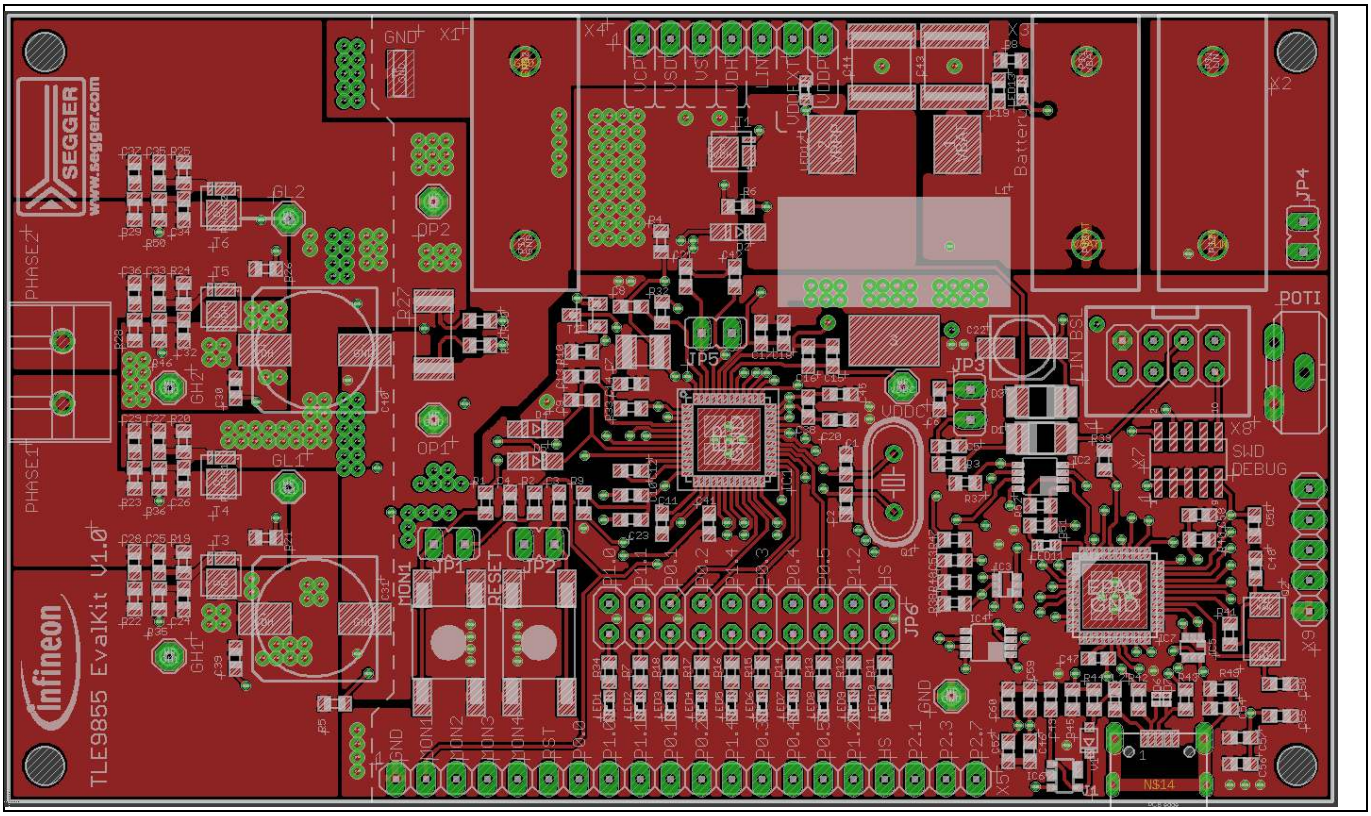


**Figure 12 Layout Top Layer**

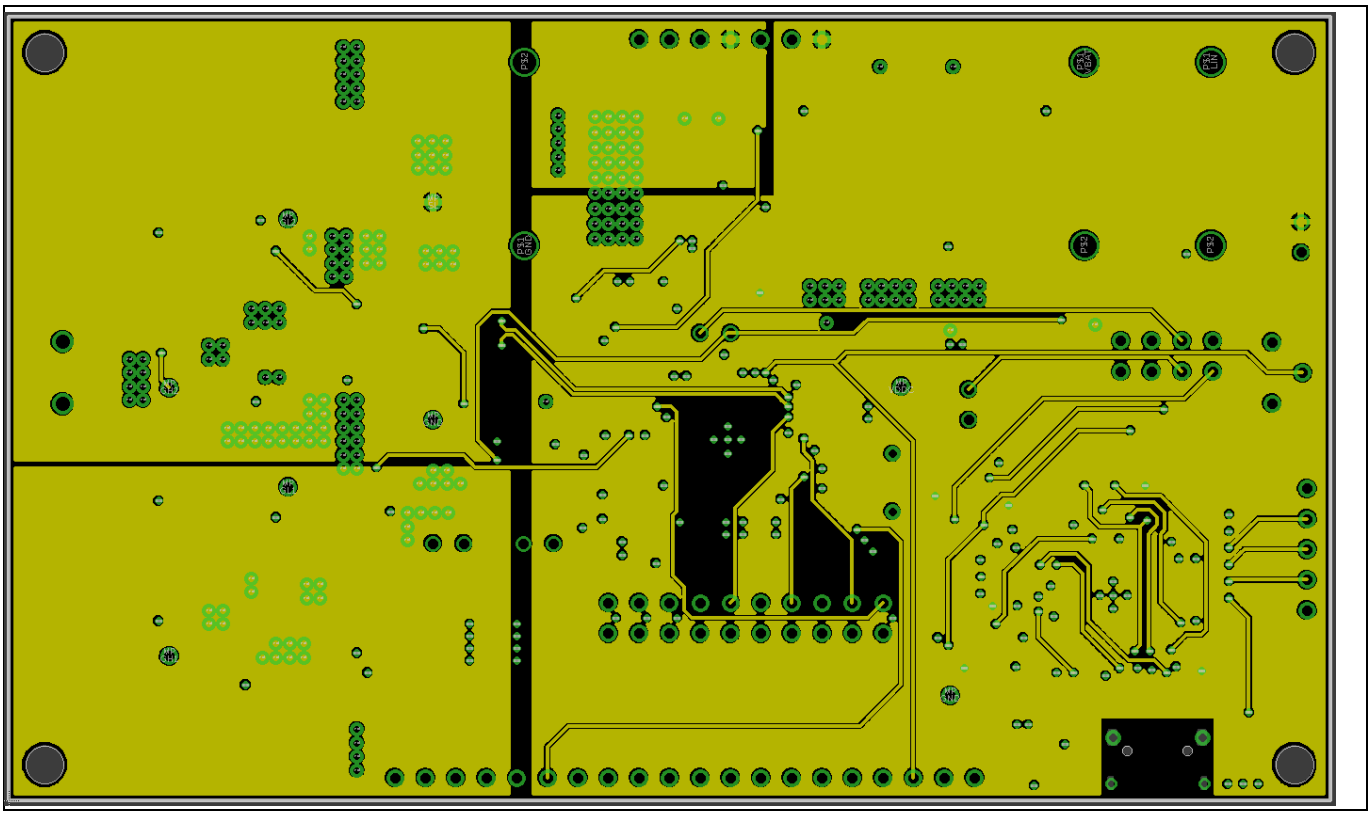

**Figure 13 Layout Layer 2**

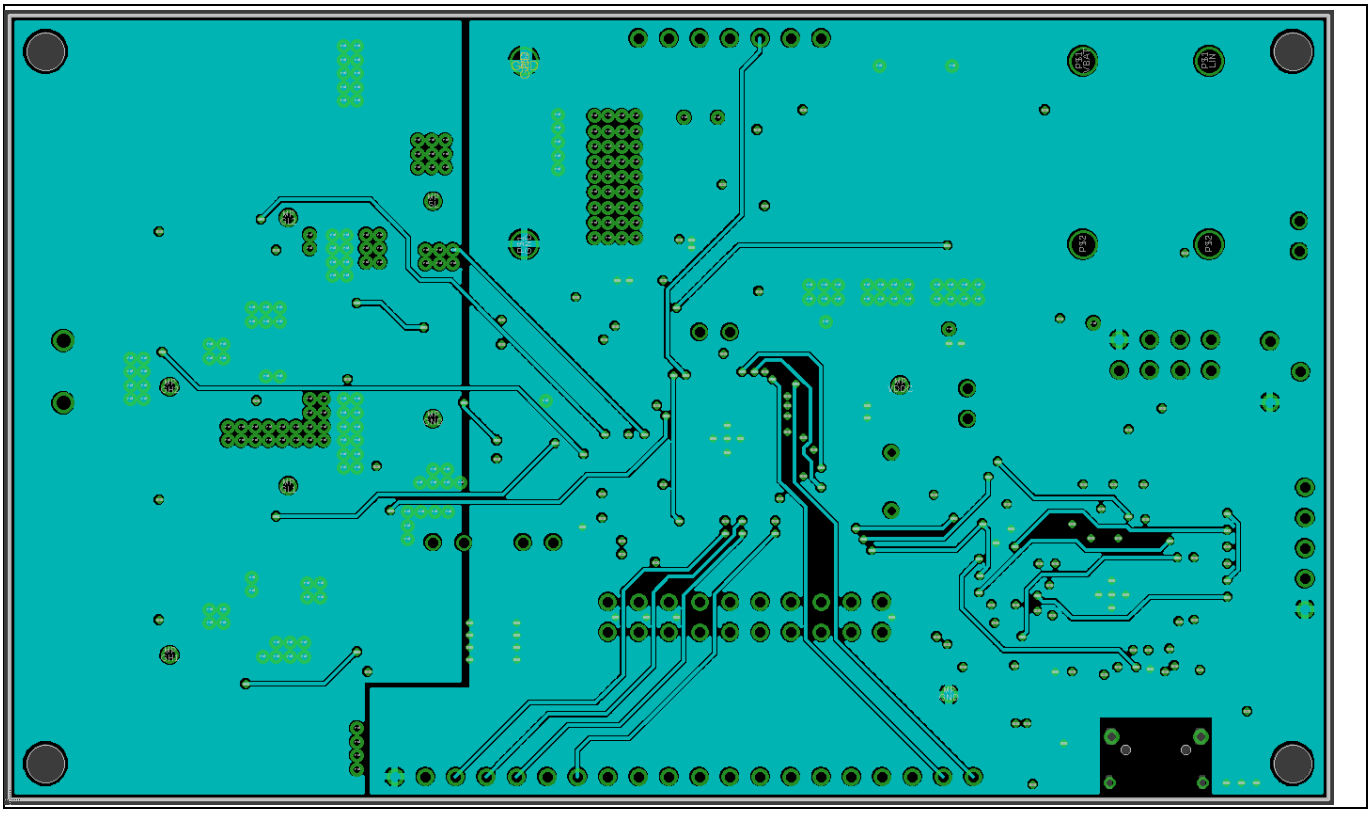

**Figure 14 Layout Layer 3**

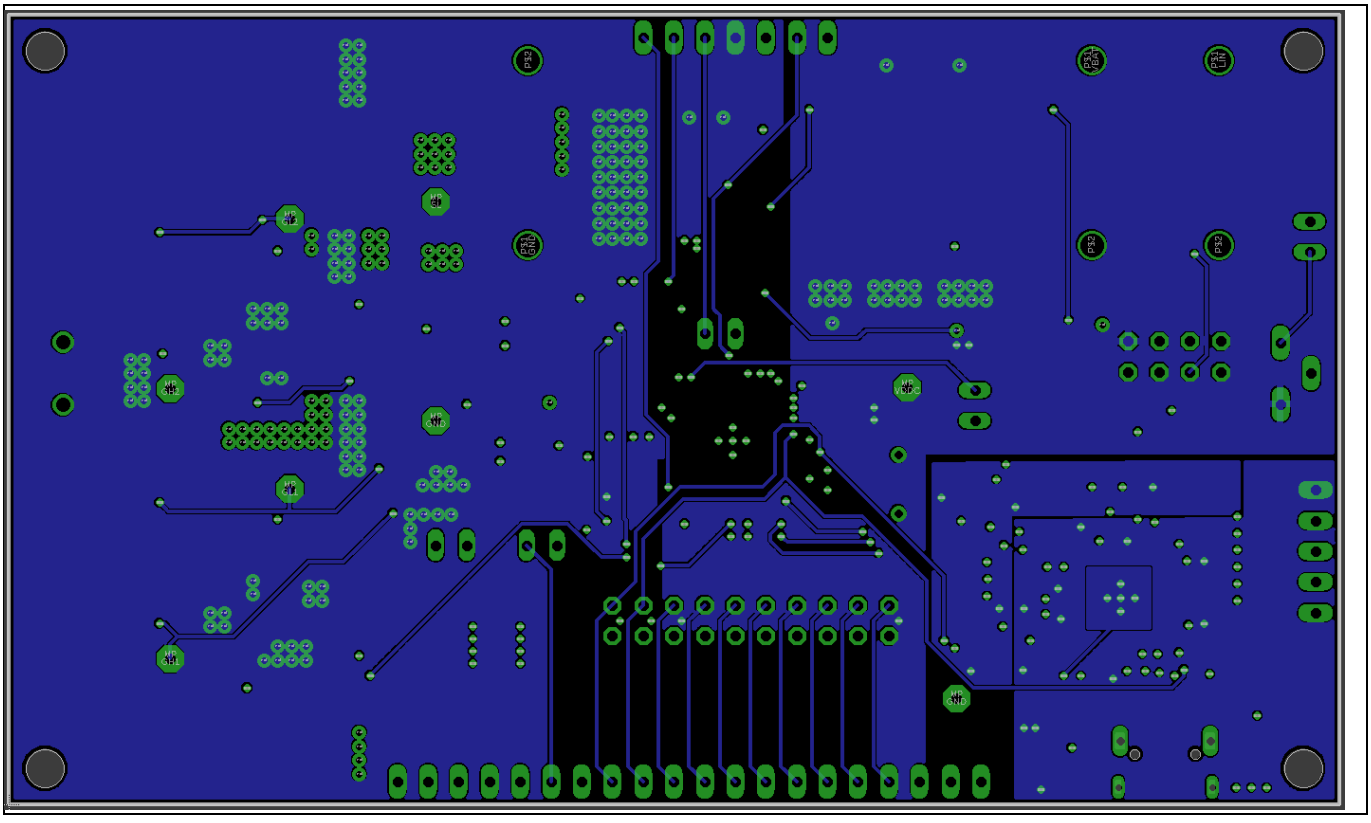

**Figure 15 Layout Bottom Layer**

# 9 Revision History

**Major changes since the last revision**

| Page or Reference | Description of change |
|---|---|
| Rev. 1.0 | Initial Version |
| | |
| | |
| | |

## Abbreviations

**Table 8 Abbreviations**

| | |
|---|---|
| BLDC | Brushless Direct Current |
| BSL | Bootstrap Loader |
| GH1,2 | Gate High side MOSFET for Phases 1, 2 |
| GL1,2 | Gate Low side MOSFET for Phase 1, 2 |
| GPIO | General Purpose Input / Output |
| ISP | In-System Programmer |
| LIN | Local Interconnect Network |
| MON | Monitor |
| n.c. | not connected |
| n/u | not used |
| OP1 | Negative Operational Amplifier Input |
| OP2 | Positive Operational Amplifier |
| RST | Reset |
| SL | Source Low side MOSFET |
| SMD | Surface Mounted Device |
| SPI | Serial Peripheral Interface |
| SWD | Arm® Serial Wire Debug |
| TMS | Test Mode Select |
| UART | Universal Asynchronous Receiver Transmitter |
| VBAT | Battery Voltage Supply |
| VCOM | Virtual COM-Port |
| VCP | Voltage Charge Pump |
| VDDC | Core Supply |
| VDDEXT | External Voltage Supply Output |
| VDDP | I/O Port Supply |
| VDH | Voltage Drain High side MOSFET |
| VS | Battery Supply Input |
| VSD | Battery Supply Input for MOSFET Driver |

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**Edition 13.02.2019**
**Published by**
**Infineon Technologies AG**
**81726 Munich, Germany**

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