

# DS2155DK/DS2156DK T1/E1/J1 Single-Chip Transceiver Design Kit Daughter Cards

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## GENERAL DESCRIPTION

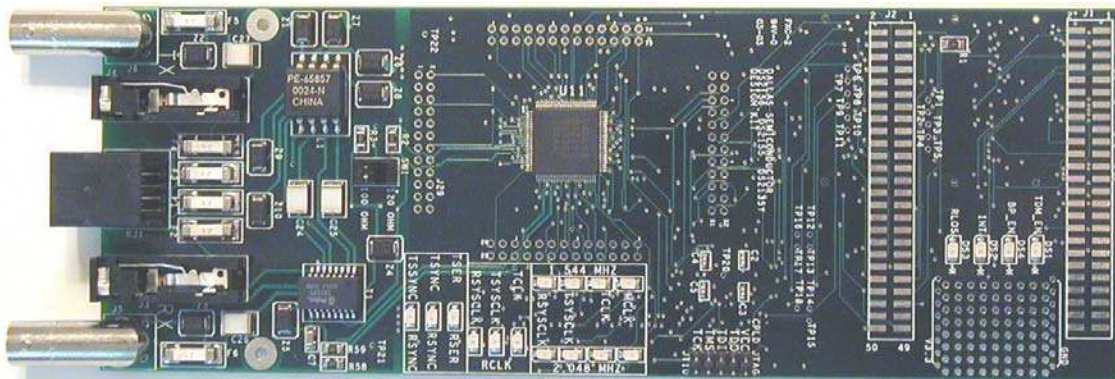
The DS2155/DS2156 design kits are evaluation boards for the DS2155 and DS2156. The DS2155/DS2156 design kits are intended to be used as daughter cards with either the DK2000 or the DK101 motherboards. The boards are complete with a single-chip transceiver (SCT), transformers, termination resistors, configuration switches, line protection circuitry, network connectors, and an interface to the motherboard.

## ORDERING INFORMATION

PART	DESCRIPTION
DS2155DK	DS2155 Design Kit Daughter Card
DS2156DK	DS2156 Design Kit Daughter Card

## FEATURES

- **Expedites New Designs by Eliminating First-Pass Prototyping**
- **Interfaces Directly to the DK101 or DK2000 Motherboards**
- **Demonstrates Key Functions of the DS2156 and DS2155**
- **High-Level Software Provides Visual Access to Registers**
- **Software-Controlled (Register Mapped) Configuration Switches to Facilitate Clock and Signal Routing**
- **BNC Connections for 75Ω E1**
- **Bantam and RJ48 Connectors for 120Ω E1 and 100Ω T1**
- **Multitap Transformer to Facilitate True Impedance Matching for 75Ω and 120Ω/100Ω Paths**
- **Network Interface Protection for Overvoltage and Overcurrent Events**
- **UTOPIA II Bus Connection for MPC8260 (DS2156 Only)**
- **UTOPIA II Prototype Connectors (DS2156 Only)**
- **Test Points and Prototype Area Available for Further Customization**



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**COMPONENT LIST**

DESIGNATION	QTY	DESCRIPTION	SUPPLIER	PART
C1–C5, C8–C12, C15–C19, C21, C22, C29–C34	23	0.1 $\mu$ F 10%, 16V ceramic capacitors (0603)	Digi-Key	311-1088-1-ND
C7, C36	2	1 $\mu$ F 10%, 16V ceramic capacitors (1206)	Digi-Key	PCC1882CT-ND
C13, C14	2	0.1 $\mu$ F 10%, 16V ceramic capacitors (0805)	Digi-Key	311-1142-1-ND
C23	1	0.1 $\mu$ F 10%, 25V ceramic capacitor (1206)	Digi-Key	PCC1883CT-ND
C24–C27	4	0.22 $\mu$ F, 50V ceramic capacitors	Digi-Key	UNK
C35	1	10 $\mu$ F 20%, 16V tantalum capacitor (B case)	Digi-Key	PCS3106CT-ND
DS1, DS4–DS18	16	LED, green, SMD	Digi-Key	P501CT-ND
DS2, DS3	2	LED, red, SMD	Digi-Key	P500CT-ND
F1–F6	6	250V, 1.25A fuse, SMT	Teccor Electronics	F1250T
J1, J2	2	Male 0.1, SMD, 50-pin, dual-row vertical	Samtec	TSM-125-01-T-DV
J3, J4	2	Bantam connectors	SWK	RTT34B02
J5, J6	2	Connector BNC RA 5-pin	Kruvand	UCBJR220
J7–J9	3	Socket, SMD, 50-pin, dual-row vertical	Samtec	TFM-125-02-S-D-LC
JT10	1	Connector, 10-pin, dual-row vertical	Digi-Key	S2012-05-ND
L1	1	Choke, dual 4-line 24 $\mu$ H, 8-pin SO	Pulse Engineering	PE-65857
R1, R14, R21	3	51.1 $\Omega$ 1%, 1/8W resistors (1206)	Digi-Key	P51.1FCT-ND
R2, R3, R58, R59	4	0 $\Omega$ 5%, 1/8W resistors (1206)	Digi-Key	P0.0ETR-ND
R4, R5, R60	3	51.1 $\Omega$ 1%, 1/10W resistors (0805)	Digi-Key	P51.1CCT-ND
R6, R9, R10, R13, R15–R19, R22, R23, R25–R29, R32, R37, R38, R44, R47–R49, R61	24	10k $\Omega$ 1%, 1/10W resistors (0805)	Digi-Key	P10.0KCCT-ND
R7, R8, R11, R12, R30, R31, R35, R36, R39–R43, R45, R50–R53	18	330 $\Omega$ 0.1%, 1/10W MF resistors (0805)	Digi-Key	P330ZCT-ND
R24	1	1.0k $\Omega$ 1%, 1/10W resistor (0805)	Digi-Key	P1.00KCCT-ND
R33, R34	2	NOPOP	—	NOPOP
R46	1	4.7k $\Omega$ 1%, 1/8W resistor (0805)	Digi-Key	9C08052A4701FK HFT
R54, R55	2	61.9 $\Omega$ 1%, 1/8W resistors (1206)	Digi-Key	P61.9FCT-ND
R56, R57	2	49.9 $\Omega$ 1%, 1/8W resistors (1206)	Digi-Key	P49.9FCT-ND
RJ1	1	RJ48 connector	Molex	43223
SW1	1	Switch DPDT slide 6-pin TH	Avnet	SSA22
T1	1	XFMR 16-pin SMT	Pulse Engineering	TX1099
U11	1	T1/E1/J1 XCVR 100-pin QFP, 0°C to +70°C	Dallas Semiconductor	DS2156L
U1–U4, U6	5	BBUS switch 10-bit CMOS, 150-mil, 24-pin SO	IDT	IDTQS3R861Q
U5	1	144-pin macrocell CPLD	Avnet	XC95144XL- 10TQ100C
U7–U10	4	Quad bus switch, 150-mil, 16-pin SO	IDT	IDTQS3125Q
Z1, Z6–Z8	4	160V, 500A Sidactor	Teccor Electronics	P1800SCMC
Z2, Z3	2	58V, 500A Sidactor	Teccor Electronics	P0640SCMC
Z4, Z5	2	6V, 50A Sidactor	Teccor Electronics	P0080SAMC
Z9, Z10	2	25V, 500A Sidactor	Teccor Electronics	P0300SCMC

## BASIC OPERATION

This design kit relies upon several supporting files, which can be downloaded from our website at [www.maxim-ic.com/DS2155DK](http://www.maxim-ic.com/DS2155DK).

### Hardware Configuration

#### *Using the DK101 processor board:*

- Connect the daughter card to the DK101 processor board.
- Supply 3.3V to the banana-plug receptacles marked GND and VCC\_3.3V. (The external 5V connector and the TIM 5V supply headers are unused.)
- All processor board DIP switch settings should be in the ON position with exception for the flash programming switch, which should be OFF.
- From the Programs menu launch the host application named ChipView.exe. Run the ChipView application. If the default installation options were used, click the Start button on the Windows toolbar and select Programs→ChipView→ChipView.

#### *Using the DK2000 processor board:*

- Connect the daughter card to the DK2000 processor board.
- Connect J1 to the power supply that is delivered with the kit. Alternately, a PC power supply can be connected to connector J2.
- From the Programs menu launch the host application named ChipView.exe. Run the ChipView application. If the default installation options were used, click the Start button on the Windows toolbar and select Programs→ChipView→ChipView.

#### *General:*

- Upon power-up the RLOS LED is lit, as well as the MCLK-2.048MHz and TCLK-2.048MHz LEDs.
- Due to the dual winding transformer, only the 120Ω line build-out configuration setting is needed to cover 75Ω E1 and 120Ω E1.

### Quick Setup (Demo Mode)

- The PC loads the program, offering a choice among Demo Mode, Register View, and Terminal Mode. Select Demo Mode.
- The program requests a configuration file, then select between the displayed files. (DS2155\_E1\_DSNCOM\_DRV.R.cfg or DS2155\_T1\_DSNCOM\_DRV.R.cfg).
- The Demo Mode screen appears. Upon external loopback, the LOS and OOF indicators extinguish.

### Quick Setup (Register View)

- The PC loads the program, offering a choice among Demo Mode, Register View, and Terminal Mode. Select Register View.
- The program requests a definition file, then select DS2155.def.
- The Register View screen appears, showing the register names, acronyms, and values.
- Predefined register settings for several functions are available as initialization files.
  - INI files are loaded by selecting the menu File→Reg Ini File→Load Ini File.
  - Load the INI file DS2155\_T1\_BERT\_ESF.ini.
  - After loading the INI file the following may be observed:
    - The RLOS LED extinguishes upon external loopback.
    - The DS2155/DS2156 begins transmitting a Daly pattern. When external loopback is applied, the BERT bit-count registers BBC1–3 and BEC1–3 may be updated by clearing and setting BC1.LC and clicking the Read All button.

#### *Miscellaneous:*

- Clock frequencies and certain pin bias levels are provided by a register-mapped CPLD, which is on the DS2155/DS2156 daughter card.
- The definition file for this CPLD is named DS215x\_35x\_CPLD\_V2.def. See the [CPLD Register Map](#) section for definitions.
- All files referenced above are available for download at [www.maxim-ic.com/DS2155DK](http://www.maxim-ic.com/DS2155DK).

## Sample UTOPIA II Configuration (DS2156 Only)

The following register settings configure the DS2156 daughter card for UTOPIA II, single CLAV, 8-bit mode on PHY port 0. UTOPIA II bus connection is provided by header J1 (Tx) and header J2 (Rx).

After configuring the following registers toggle the MSTREG.URST bit to reset the UTOPIA II core.

### UTOPIA II Setup, Register Settings for daughter card CPLD

NAME	VALUE	NAME	VALUE
SWITCH 1	0x0F	SWITCH 4	0x0F
SWITCH 2	0x03	LEVELS	0x07
SWITCH 3	0x0F		

### UTOPIA II Setup, Register Settings for DS2156 E1 Configuration

NAME	VALUE	NAME	VALUE
MSTREG	0x02	LBCR	0x00
E1RCR1	0x68	TAF	0x9B
E1RCR2	0x00	TNAF	0xC0
E1TCR1	0x15	LIC1	0x11
E1TCR2	0x00	LIC2	0x90
CCR1	0x00	LIC3	0x00
CCR4	0x00	LIC4	0x00
IOCR1	0x00		
IOCR2	0x00		

### UTOPIA II Setup, Register Settings for DS2156 UTOPIA II Configuration

NAME	VALUE	NAME	VALUE
U_TCFR	0x01	U_RCR2	0x0
U_TCR1	0x05	U_TIUPB	0x0
U_TCR2	0x00	PCPR	0x22
U_RCFR	0x01	PCDR1, 2, 3, 4	0x0
U_RCR1	0x01		

## REGISTER MAP

The DK101 daughter card address space begins at 0x81000000.

The DK2000 daughter card address space begins at:

- 0x30000000 for slot 0
- 0x40000000 for slot 1
- 0x50000000 for slot 2
- 0x60000000 for slot 3

All offsets given in [Table 1](#) are relative to the beginning of the daughter card address space.

**Table 1. Daughter Card Address Map**

OFFSET	DEVICE	DESCRIPTION
0X0000 to 0X0015	CPLD	Board identification and clock/signal routing
0X1000 to 0X10ff	Single-Chip Transceiver	Board is populated with one of the following: DS2156, DS2155, DS21352, or DS21354. Please see data sheet for details.

Registers in the CPLD can be easily modified using the ChipView.exe, a host-based user interface software along with the definition file named *DS215x\_35x\_CPLD\_V2.def*. Definition files for the SCT are named *DS2155.def*, *DS21352.def*, or *DS21354.def*, depending on the board population option.

## CPLD Register Map

**Table 2. CPLD Register Map**

OFFSET	NAME	TYPE	DESCRIPTION
0X0000	BID	Read-Only	Board ID
0X0002	XBIDH	Read-Only	High-Nibble Extended Board ID
0X0003	XBIDM	Read-Only	Middle-Nibble Extended Board ID
0X0004	XBIDL	Read-Only	Low-Nibble Extended Board ID
0X0005	BREV	Read-Only	Board FAB Revision
0X0006	AREV	Read-Only	Board Assembly Revision
0X0007	PREV	Read-Only	PLD Revision
0X0011	SWITCH1	Read-Write	Pin to 1.544MHz
0X0012	SWITCH2	Read-Write	Pin to 2.048MHz
0X0013	SWITCH3	Read-Write	Pin-to-Pin Connect
0X0014	SWITCH4	Read-Write	Pin-to-Pin Connect
0X0015	LEVELS	Read-Write	Set Level On Pin 1 = 3.3V

## ID Registers

OFFSET	NAME	TYPE	VALUE	DESCRIPTION
0X0000	BID	Read-Only	0xD	Board ID
0X0002	XBIDH	Read-Only	0x0	High-Nibble Extended Board ID
0X0003	XBIDM	Read-Only	0x0	Middle-Nibble Extended Board ID
0X0004	XBIDL	Read-Only	0x5	Low-Nibble Extended Board ID
0X0005	BREV	Read-Only	Displays current FAB revision	Board FAB Revision
0X0006	AREV	Read-Only	Displays current assembly revision	Board Assembly Revision
0X0007	PREV	Read-Only	Displays current PLD firmware revision	PLD Revision

## Control Registers

The control registers are used primarily to control several banks of FET switches that route clocks and backplane signals. Please note that certain register settings cause line contention, e.g., setting SWITCH1.4 and SWITCH2.4 both to 0 would drive MCLK with both 1.544MHz and 2.048MHz.

### SWITCH1: PIN TO 1.544MHz (OFFSET = 0x0011) INITIAL VALUE = 0xF

(MSB)

(LSB)

—	—	—	—	MCLK	TCLK	RSYSCLK	TSYSCLK
---	---	---	---	------	------	---------	---------

NAME	POSITION	FUNCTION
MCLK	SWITCH1.3	0 = Connect MCLK to the 1.544MHz clock 1 = Open Switch 1.4
TCLK	SWITCH1.2	0 = Connect TCLK to the 1.544MHz clock 1 = Open Switch 1.3
RSYSCLK	SWITCH1.1	0 = Connect RSYSCLK to the 1.544MHz clock 1 = Open Switch 1.2
TSYSCLK	SWITCH1.0	0 = Connect TSYSCLK to the 1.544MHz clock 1 = Open Switch 1.1

**SWITCH2: PIN TO 2.048MHz (Offset = 0X0012) INITIAL VALUE = 0x3****(MSB)****(LSB)**

—	—	—	—	MCLK	TCLK	RSYSCLK	TSYSCLK
---	---	---	---	------	------	---------	---------

NAME	POSITION	FUNCTION
MCLK	SWITCH2.3	0 = Connect MCLK to the 2.048MHz clock 1 = Open Switch 2.4
TCLK	SWITCH2.2	0 = Connect TCLK to the 2.048MHz clock 1 = Open Switch 2.3
RSYSCLK	SWITCH2.1	0 = Connect RSYSCLK to the 2.048MHz clock 1 = Open Switch 2.2
TSYSCLK	SWITCH2.0	0 = Connect TSYSCLK to the 2.048MHz clock 1 = Open Switch 2.1

**SWITCH3: PIN-TO-PIN CONNECT (Offset = 0X0013) INITIAL VALUE = 0xF****(MSB)****(LSB)**

—	—	—	—	TSS_RS	TCL_RC	RSY_RC	TSY_RC
---	---	---	---	--------	--------	--------	--------

NAME	POSITION	FUNCTION
TSS_RS	SWITCH3.3	0 = Connect TSSYNC to RSYNC 1 = Open Switch 3.4
TCL_RC	SWITCH3.2	0 = Connect TCLK to RCLK 1 = Open Switch 3.3
RSY_RC	SWITCH3.1	0 = Connect RSYSCLK to RCLK 1 = Open Switch 3.2
TSY_RC	SWITCH3.0	0 = Connect TSYSCLK to RCLK 1 = Open Switch 3.1

**SWITCH4: PIN-TO-PIN CONNECT (Offset = 0X0014) INITIAL VALUE = 0x3****(MSB)****(LSB)**

—	—	—	—	UTCLK_2048	UT_CLK_2048	RSER_TSER	RSYNC_TSYNC
---	---	---	---	------------	-------------	-----------	-------------

NAME	POSITION	FUNCTION
URCLK_2048	SWITCH4.3	0 = Connect UR_CLK (TSSYNC) to 2.048MHz 1 = Open Switch 4.4
UTCLK_2048	SWITCH4.2	0 = Connect UT_CLK (TCHCLK) to 2.048MHz 1 = Open Switch 4.3
RSER_TSER	SWITCH4.1	0 = Connect RER to TSER 1 = Open Switch 4.2
RSYNC_TSYNC	SWITCH4.0	0 = Connect RSYNC to TSYNC 1 = Open Switch 4.1

**LEVELS: SET LEVEL ON PIN (Offset = 0X0015) INITIAL VALUE = 0x6**

(MSB)

(LSB)

—	—	—	—	—	BP_EN	PPCTDM_EN	TUSEL
---	---	---	---	---	-------	-----------	-------

NAME	POSITION	FUNCTION
—	LEVELS1.3	—
BP_EN	LEVELS1.2	0 = Enable IDT switches that connect the UTOPIA bus to daughter card header
PPCTDM_EN	LEVELS1.1	0 = Enable IDT switches that connect the TDM bus to the daughter card header
TUSEL	LEVELS1.0	0 = Set DS2156.TUSEL to enable TDM backplane 1 = Set DS2156.TUSEL to enable UTOPIA backplane

**Note:** When the UTOPIA backplane is enabled (LEVELS.TUSEL = 1) there is a possibility for contention between the UTOPIA bus master and TSYSClk, TSER, and RSER. To avoid this, the following switches should be opened when the UTOPIA backplane is enabled: SWITCH1.0, SWITCH2.0, SWITCH3.0, and SWITCH4.1

**DS2155/DS2156 INFORMATION**

For more information about the DS2155 and DS2156, please consult the DS2155 and DS2156 data sheets available on our website at [www.maxim-ic.com/DS2155](http://www.maxim-ic.com/DS2155) and [www.maxim-ic.com/DS2156](http://www.maxim-ic.com/DS2156). Software downloads are also available for this design kit.

**DS2155DK/DS2156DK INFORMATION**

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**TECHNICAL SUPPORT**

For additional technical support, please e-mail your questions to [telecom.support@dalsemi.com](mailto:telecom.support@dalsemi.com).

**SCHEMATICS**

The DS2155DK/DS2156DK schematics are featured in the following 13 pages.

**DOCUMENT REVISION HISTORY**

REVISION DATE	DESCRIPTION
032503	Initial DS2155DK/DS2156DK data sheet release.
060303	Updated the <i>Title, General Description, Features, and Basic Operation</i> sections; "TIM" replaced with "daughter card."
012705	Updated schematics (removed component values for Fuse and Sidactor; see <i>Component List</i> ).
110106	Updated schematics.



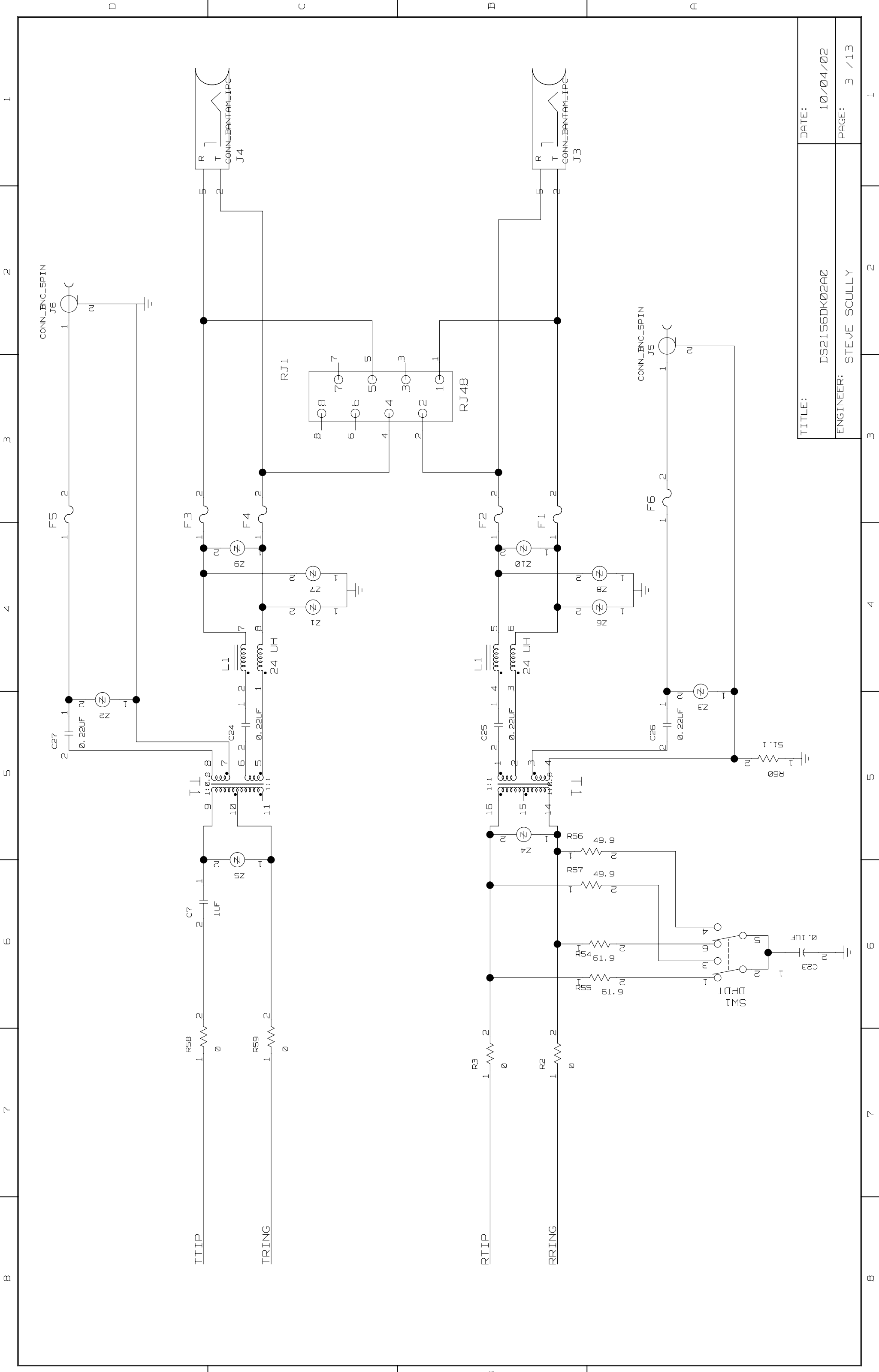
# DS2156, DS2155, DS2135Y DESIGN KIT

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13. PART CROSS-REFERENCE

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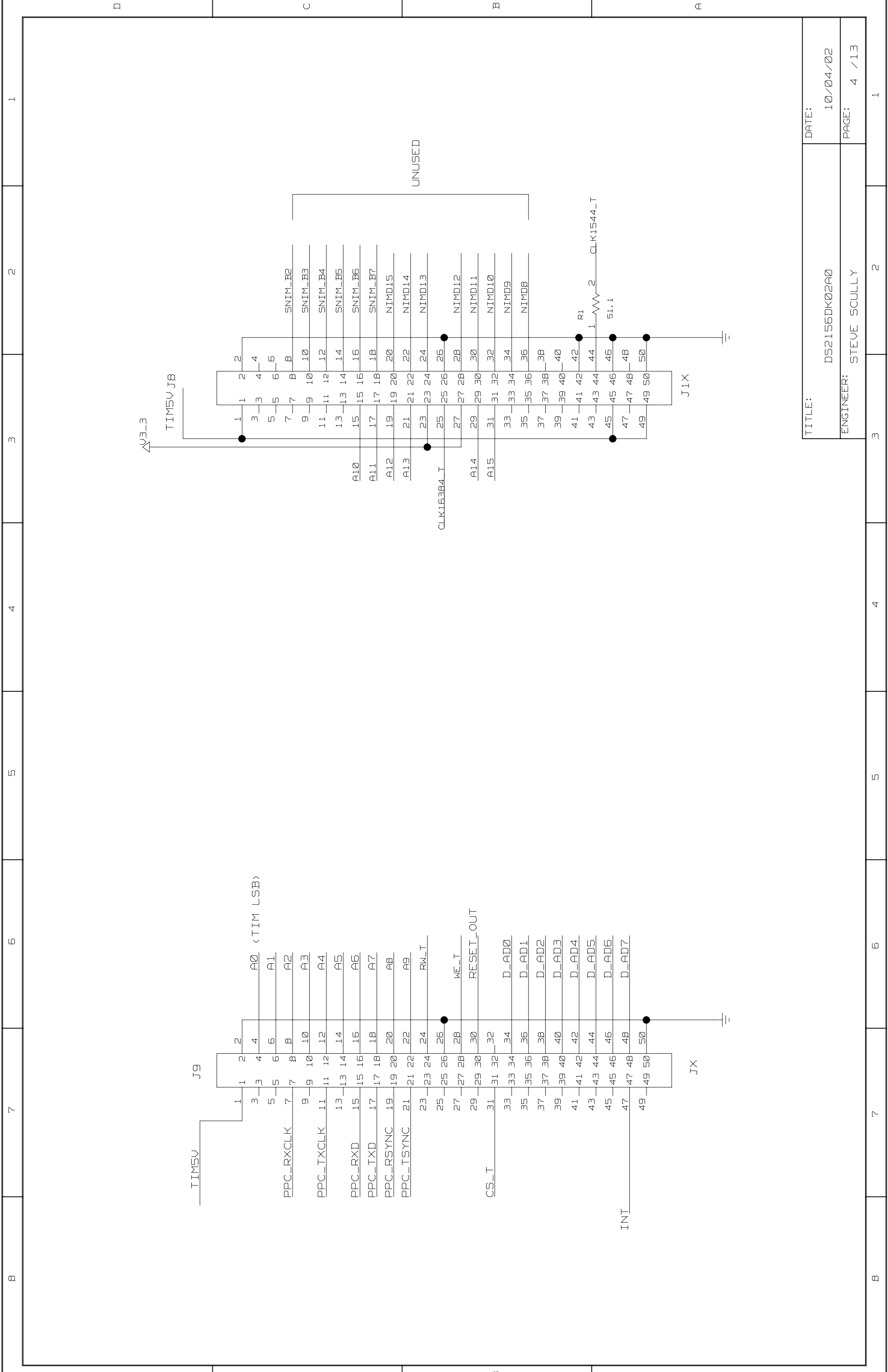




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D C B A



8 7 6 5 4 3 2 1

D C B A

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8 7 6 5 4 3 2 1





J1

CONN\_50P1

TXDATA_0	1	2	TXDATA_1
TXDATA_2	3	4	TXDATA_3
GND	5	6	TXDATA_4
TXDATA_5	7	8	TXDATA_6
TXDATA_7	9	10	GND
	11	12	
	13	14	
	15	16	
	17	18	
	19	20	GND
	21	22	TXSOC
TXADDR0	23	24	TXADDR1
GND	25	26	TXADDR2
TXADDR3	27	28	TXADDR4
TXCLAV0	29	30	GND
	31	32	
	33	34	TXENABLE
	35	36	R14 2 LUT_CLK
	37	38	
	39	40	
	41	42	
	43	44	
	45	46	
	47	48	
	49	50	

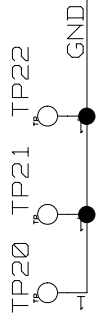
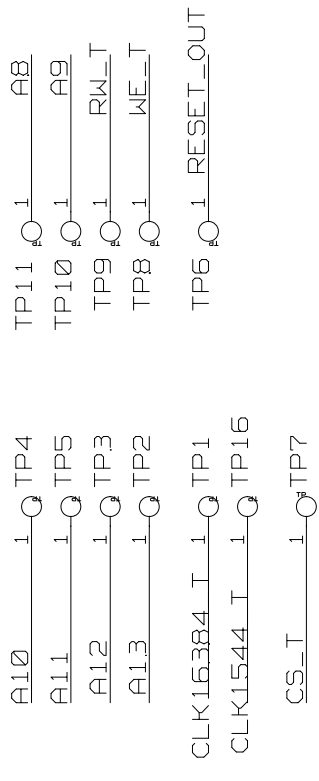
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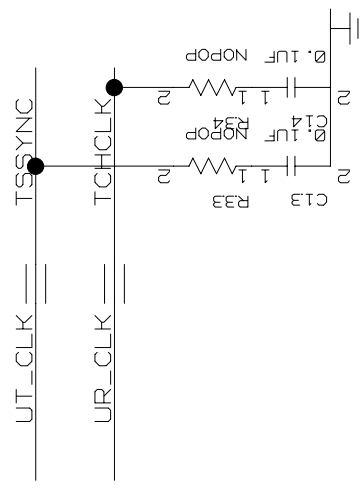
J2

CONN\_50P1

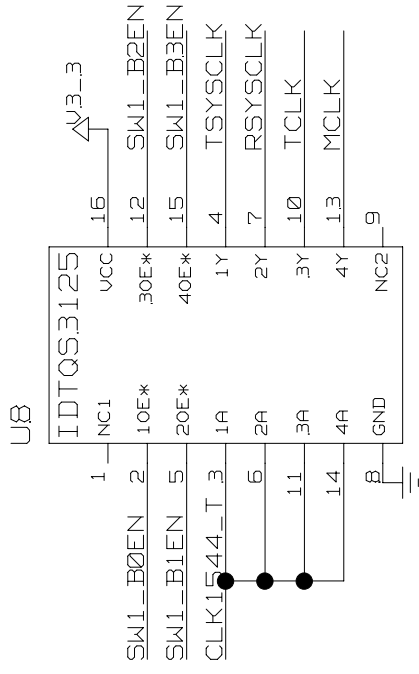
RXDATA_0	1	2	RXDATA_1
RXDATA_2	3	4	RXDATA_3
GND	5	6	RXDATA_4
RXDATA_5	7	8	RXDATA_6
RXDATA_7	9	10	GND
	11	12	
	13	14	
	15	16	
	17	18	
	19	20	GND
	21	22	RXSOC
	23	24	
	25	26	
	27	28	
	29	30	
	31	32	
	33	34	
	35	36	
RXADDR0	37	38	RXADDR1
RXADDR2	39	40	GND
RXADDR3	41	42	RXADDR4
RXCLAV0	43	44	
GND	45	46	
	47	48	RXENB
UR_CLK_1	49	50	
	51		

ADTECH RX

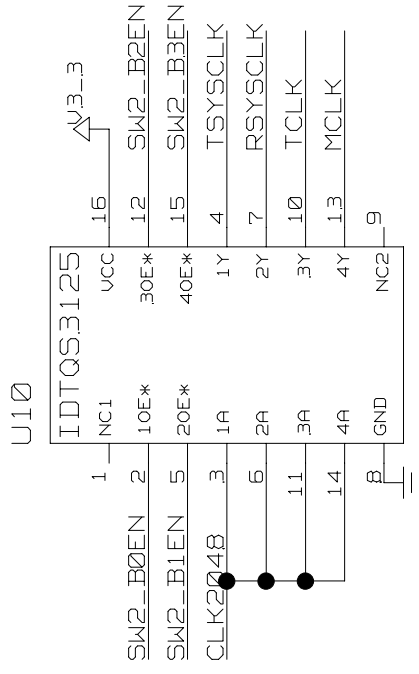


8	7	6	5	4	3	2	1
D	D	C	B	A			
RXADDR0 == RXA_0 == UR_ADDR0 == RCHCLK == RXADDR1 == RXA_1 == UR_ADDR1 == RSIGF == RXADDR2 == RXA_2_RXCLAV_1 == UR_ADDR2 == RSIG == RXADDR3 == RXA_3_RXCLAV_2 == UR_ADDR3 == RMSYNC == RXADDR4 == RXA_4_RXCLAV_3 == UR_ADDR4 == RFSYNC == RXCLAV0 == RXCLAV_0 == UR_CLAV == RSER == RXDATA_0 == RXDATA_0 == UR_DATA0 == RLINK == RXDATA_1 == RXDATA_1 == UR_DATA1 == RLCLK == RXDATA_2 == RXDATA_2 == UR_DATA2 == RPOSI == RXDATA_3 == RXDATA_3 == UR_DATA3 == RNEGI == RXDATA_4 == RXDATA_4 == UR_DATA4 == RCLKI == RXDATA_5 == RXDATA_5 == UR_DATA5 == RCLKO == RXDATA_6 == RXDATA_6 == UR_DATA6 == RNEGO == RXDATA_7 == RXDATA_7 == UR_DATA7 == RPOSO ==	RXENB == RXENA == UR_ENB == BPCLK == RXSOC == RXSOC == UR_SOC == RCHBLK == TXADDR0 == TXA_0 == UT_ADDR0 == UOP3 == TXADDR1 == TXA_1 == UT_ADDR1 == TCHBLK == TXADDR2 == TXA_2_TXCLAV_1 == UT_ADDR2 == TLCLK == TXADDR3 == TXA_3_TXCLAV_2 == UT_ADDR3 == TLINK == TXADDR4 == TXA_4_TXCLAV_3 == UT_ADDR4 == TPOSI == TXCLAV0 == UT_CLAV == TXCLAV_0 == LIUC == TXDATA_0 == TXDATA_0 == UT_DATA0 == TNEGI == TXDATA_1 == TXDATA_1 == UT_DATA1 == TCLKI == TXDATA_2 == TXDATA_2 == UT_DATA2 == TCLKO == TXDATA_3 == TXDATA_3 == UT_DATA3 == TNEGO == TXDATA_4 == TXDATA_4 == UT_DATA4 == TPOSO == TXDATA_5 == TXDATA_5 == UT_DATA5 == TSEI ==	TXDATA_6 == TXDATA_6 == UT_DATA6 == TSIG == TXDATA_7 == TXDATA_7 == UT_DATA7 == TSYSCLK == TXENABLE == TXENA == UT_ENB == UOP1 == TXSOC == TXSOC == UT_SOC == UOP0 ==	UT_CLK == TSSYNC UR_CLK == TCHCLK 				
D	C	B	A				
TITLE:	DS2156DK02A0	DATE:	10/04/02	ENGINEER:	STEVE SCULLY	PAGE:	8 / 13
8	7	6	5	4	3	2	1

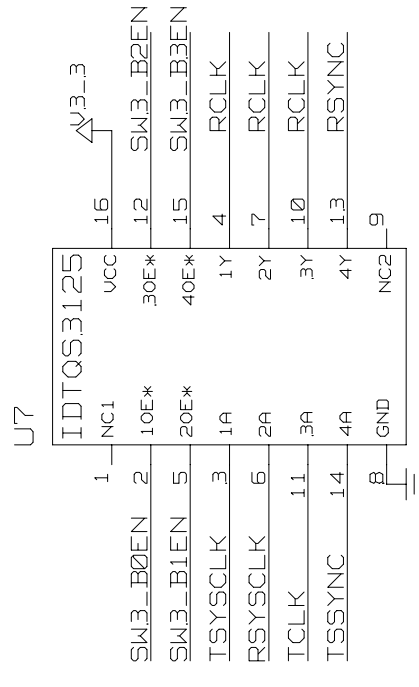




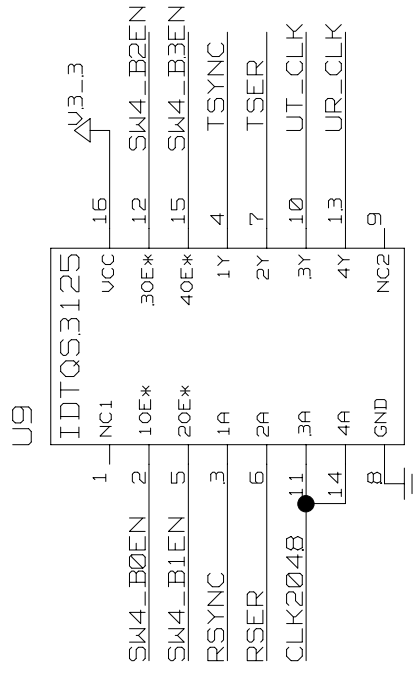
SWITCH 1 IS MEMORY MAPPED TO PLD REGISTER 0X11 LOGIC 0 CLOSES SWITCH LOGIC 1 OPENS SWITCH



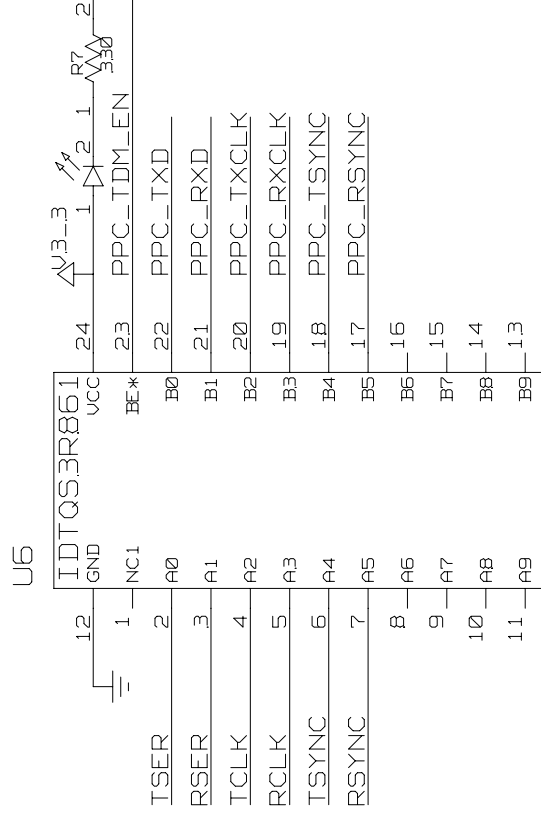
SWITCH 2 IS MEMORY MAPPED TO PLD REGISTER 0X12 LOGIC 0 CLOSES SWITCH LOGIC 1 OPENS SWITCH



SWITCH 3 IS MEMORY MAPPED TO PLD REGISTER 0X13 LOGIC 0 CLOSES SWITCH LOGIC 1 OPENS SWITCH



SWITCH 4 IS MEMORY MAPPED TO PLD REGISTER 0X14 LOGIC 0 CLOSES SWITCH LOGIC 1 OPENS SWITCH



PPC\_TDM\_EN IS BIT MAPPED TO PLD ADDRESS 0X15 BIT 1 LOGIC 0 CLOSES SWITCHES

TITLE:

DS2156DK02A0

DATE:

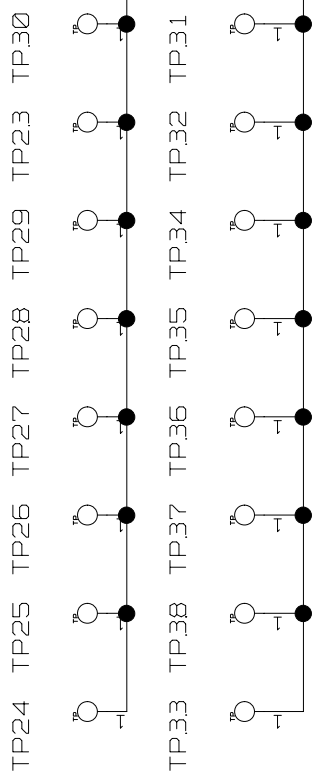
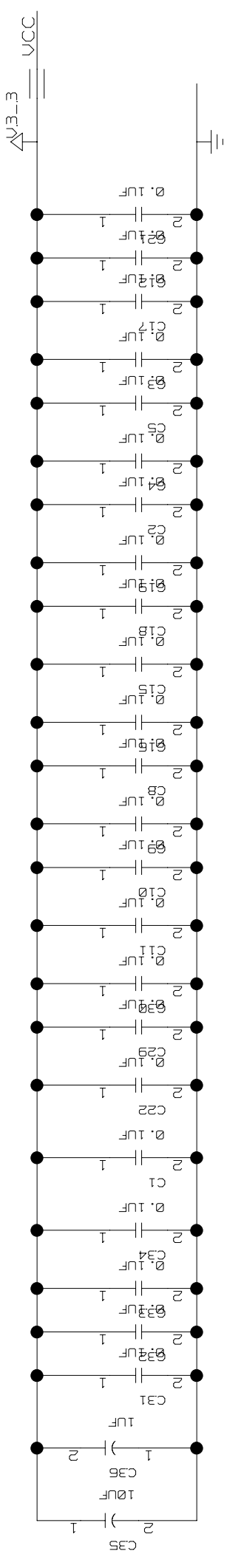
10/04/02

ENGINEER:

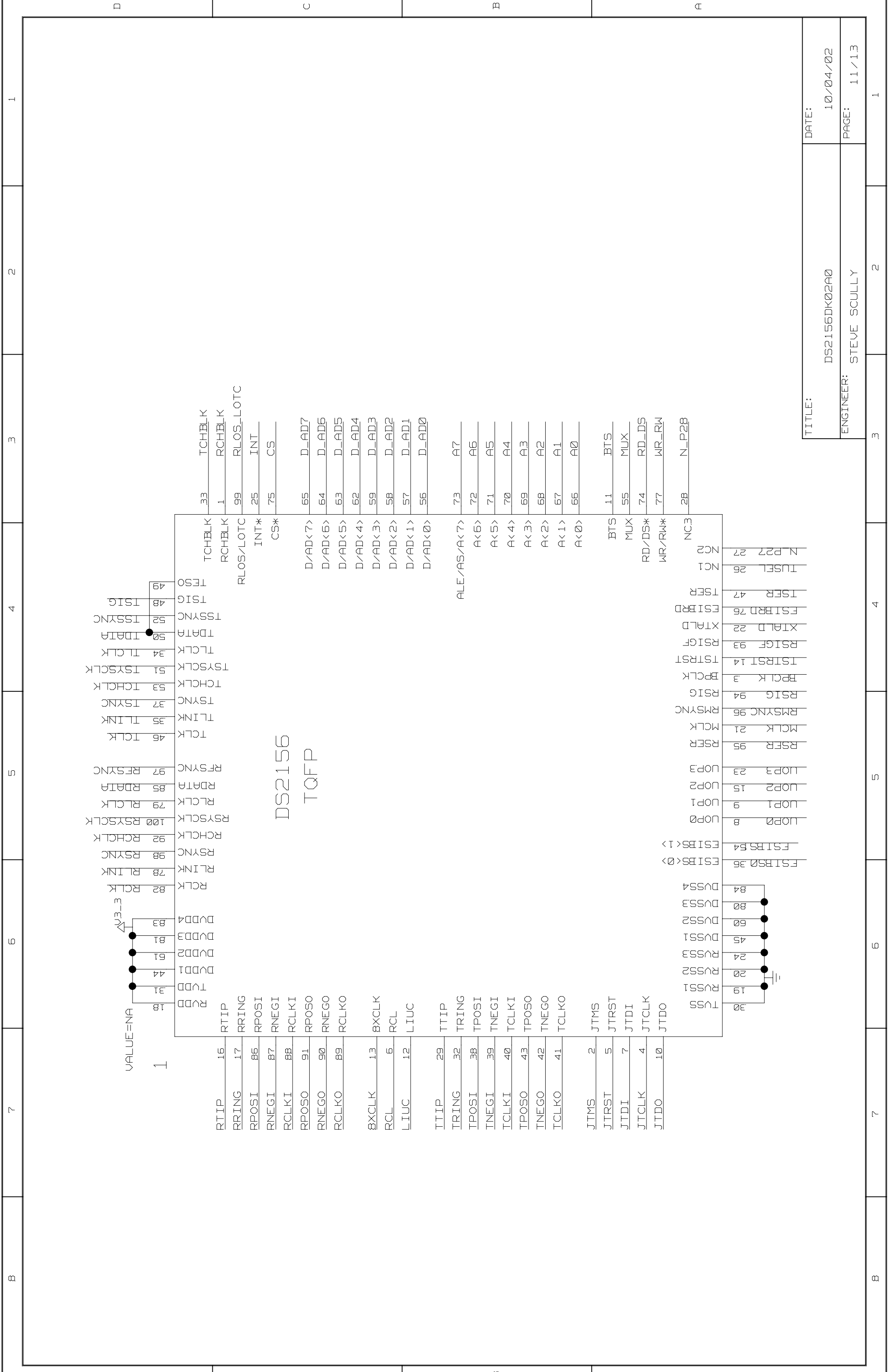
STEVE SCULLY

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DS2156  
TQFP

VALUE=NA  
1

TITLE: DS2156DK02A0  
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ENGINEER: STEVE SCULLY  
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*** Signal Cross-Reference for the entire design ***
BXCLK      2CB<> 11C7>
A0         4CB<> 5C4<> 2B3<> 11B3<>
A1         4C6<> 5C4<> 2B3<> 11B3<>
A2         4C6<> 5C4<> 2B3<> 11B3<>
A3         4C6<> 5C4<> 2B3<> 11B3<>
A4         4C6<> 5C4<> 2B3<> 11B3<>
A5         4C6<> 5C4<> 2B3<> 11B3<>
A6         4C6<> 5C4<> 2B3<> 11B3<>
A7         4C6<> 5C4<> 2B3<> 11B3<>
A8         4C6<> 7B1<>
A9         4B6<> 7B1<>
A10        4C3<> 7C3<>
A11        4C3<> 5C1<> 7C3<>
A12        4C3<> 5C1<> 7B3<>
A13        4B3<> 7B3<>
A14        4B3<>
A15        4B3<>
BPCLK      2A5<> BD4<> 11A4>
BP_EN      5C1<> 6B2<> 6B6<> 6C2<> 6C6<>
BTS        5D4<> 2B3<> 5A6<> 11A3<>
CLK1544_T  7B3<> 9DB<> 4B2<>
CLK204B    5D3<> 9B3<> 9B8<>
CLK163B4_T 4B4<> 5D3<> 7B3<>
CS         5B4<> 2C3<> 11C3<>
CS_T       4B8<> 5B1<> 7B3<>
D_AD0      2B3<> 4B6<> 5C1<> 11B3<>
D_AD1      2C3<> 4B6<> 5C1<> 11B3<>
D_AD2      2C3<> 4B6<> 5C1<> 11C3<>
D_AD3      2C3<> 4B6<> 5C1<> 11C3<>
D_AD4      2C3<> 4B6<> 5C1<> 11C3<>
D_AD5      2C3<> 4B6<> 5C1<> 11C3<>
D_AD6      2C3<> 4A6<> 5C1<> 11C3<>
D_AD7      2C3<> 4A6<> 5D1<> 11C3<>
ESI8B0     2A5<> 11A4<> 5A8<>
ESI8B1     2A6<> 11A6<>
ESI8B5     2A6<> 11A5<>
INT         2C3<> 4A8<> 5A2<> 11C3> 5A6<>
INT_INDICATOR
JTCLK      2A8<> 11A7<>
JTDI       2A8<> 11A7<>
JTDO       2A8<> 11A7>
JTMS       2B8<> 11B7<>
JT_RST     2B8<> 5A8<> 11A7<>
LIUC       B84> 2CB<> 5A6<> 11B7<>
MCLK       9B6<> 9C6<> 2A5<> 11A5<>
MUX        5C4<> 2A3<> 5A8<> 11A3<>
NIMDB      4B2<>
NIMD9      4B2<>
NIMD10     4B2<>
NIMD11     4B2<>
NIMD12     4B2<>
NIMD13     4B2<>
NIMD14     4B2<>
NIMD15     4C2<>
NLP27      2A4<> 11A4<>
NLP28      2A3<> 11A3<>
PPC_RSYN   4CB<> 9A4<>
PPC_RXCLK  4CB<> 9A4<>
PPC_RXD    4CB<> 9A4<>
PPC_TDMEN  5C1<> 9A4<>
PPC_TSYN   4B8<> 9A4<>
PPC_TXCLK  4CB<> 9A4<>
PPC_TXD    4CB<> 9A4<>
RCHCLK     2C3> BD4> 11C3>
RCHCLK     2D6> BD7> 11D5>
RCL        2CB> 11C7>
RCLK       2D6> 9A6<> 9C1<> 9C1<> 9D1<> 11D6>
RCLKI      B87> 2CB<> 5A8<> 11C7<>
RCLKO      2CB> B87> 11C7>
RDATA      2D6> 11D5>
RD_DS      5C4<> 2A3<> 11A3<>
RESET_OUT  4B6<> 5B1<> 7B1<>
RFSYN      2D6> B87> 11D5>
RCLK       2D6> B87> 11D5>

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RLINK      2D6> B87> 11D6>
RLOS_LOTC  2C3> 5B2<> 11C3>
RLOS_LOTC_INDICATOR 5A2<>
RMSYN      2A5> B87> 11A5>
RNEG1      B87> 2CB<> 5A8<> 11C7<>
RNEG0      2CB> B87> 11C7>
RPOS1      B87> 2CB<> 5A8<> 11C7<>
RPOS0      2CB> B87> 11C7>
RRING      2CB<> 3B8<> 11C7<>
RSE1       2A5> B87> 11A5>
RSE2       2A5> B87> 11A5>
RSIG        2A5> B87> 11A5>
RSIGF      2A5> B87> 11A4>
RSYN        2D6<> 9A6<> 9B3<> 9C1<> 11D5<>
RSYNCLK    9B6<> 9C3<> 9D6<> 2D6<> 5A8<> 11D5<>
RTIP        2CB<> 3B8<> 11C7<>
RWLT        4B6<> 5B1<> 7B1<>
RXADDR0    7B8<> BDB
RXADDR1    7B8<> BDB
RXADDR2    7B8<> BDB
RXADDR3    7B8<> BDB
RXADDR4    7B8<> BDB
RXA_0      6B2<> B07>
RXA_1      6B7<> B07>
RXA_2_RXCLAV_1 6A7<> 6B2<> B07>
RXA_3_RXCLAV_2 6A7<> 6C7<> B07>
RXA_4_RXCLAV_3 6A7<> 6B2<> B07>
RXCLAV0    7A8<> BCB
RXCLAV_0   6A7<> B07>
RXCLAV_1   6A7<> 7C8<> B87> B8B
RXDATA_0   6A2<> 7C6<> B87> B8B
RXDATA_1   6B7<> 7CB<> B87> B8B
RXDATA_2   6B2<> 7C6<> B87> B8B
RXDATA_3   6B7<> 7C6<> B87> B8B
RXDATA_4   6B2<> 7C8<> B87> B8B
RXDATA_5   6B7<> 7C6<> B87> B8B
RXDATA_6   6B2<> 7C8<> B87> B8B
RXDATA_7   6B7<> 7C6<> B87> B8B
RXENA      6A2<> B04>
RXPRTY     7A6<> B05
RXSOC      6B5<>
SNIM_B2    6B7<> 7B6<> BD4> B05
SNIM_B3    4C2<>
SNIM_B4    4C2<>
SNIM_B5    4C2<>
SNIM_B6    4C2<>
SNIM_B7    4C2<>
SW1_B0EN  5A4<> 9DB<>
SW1_B1EN  5A4<> 9DB<>
SW1_B2EN  5A3<> 9D6<>
SW1_B3EN  5A3<> 9D6<>
SW2_B0EN  5A3<> 9B8<>
SW2_B1EN  5A3<> 9B8<>
SW2_B2EN  5A3<> 9B6<>
SW2_B3EN  5A3<> 9B6<>
SW3_B0EN  5A3<> 9D3<>
SW3_B1EN  5A3<> 9D3<>
SW3_B2EN  5A3<> 9D1<>
SW3_B3EN  5A3<> 9D1<>
SW4_B0EN  5B4<> 9B3<>
SW4_B1EN  5B4<> 9B3<>
SW4_B2EN  5B4<> 9B2<>
SW4_B3EN  5B4<> 9B2<>
TCHCLK     2D3> B84> 11C3>
TCHCLK     2D5> 11D4> B81<>
TCK        5B8<> 5DB<>
TCLK       9A6<> 9B6<> 9C3<> 9C6<> 2D5<> 5A6<>
          11D5<>
TCLKI      B84> 2B8<> 5A8<> 11B7<>
TCLKO      2B8> B84> 11B7>
TDATA      2D5<> 11D4<>
TDI        5B8<> 5D7<>
TDO        5B8<> 5C7<>
TIMEV      4D3<> 4DB<>
TLCLK      2D5> B84> 11D4>
TLINK      B84> 2D5<> 5B6<> 11D5<>
TMS        5B8<> 5C7<>

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TNEG1      B84> 2B8<> 5A8<> 11B7<>
TNEG0      2B8> B84> 11B7>
TPOS0      8C4> 2B8<> 5A8<> 11B7<>
TPOS1      2B8> B84> 11B7>
TRING      2B8> 11B7> 3CB<>
TRSER      B84> 9A6<> 9B2<> 2A5<> 5A8<> 11A4<>
TSIG       B01> 2D5<> 5B6<> 11D4<>
TSSYN      9C3<> 2D5<> 5B6<> B81<> 11D4<>
TSTRST     2A5<> 5A8<> 11A4<>
TSYN       2D5<> 9A6<> 9B2<> 11D5<> 5A6<>
TSYNCLK    B01> 9B6<> 9D3<> 9D6<> 2D5<> 5A8<>
          11D4<>
TTIP       2B8> 11B7> 3CB<>
TUSEL      5D2<> 2A4<> 11A4<>
TXADDR0    7B5<> B05
TXADDR1    7B4<> B05
TXADDR2    7B4<> B05
TXADDR3    7B5<> B05
TXADDR4    7B4<> B05
TXA_0      6C2<> B04>
TXA_1      6C7<> B04>
TXA_2_TXCLAV_1 6B2<> 6C2<> B04>
TXA_3_TXCLAV_2 6C7<> 6C7<> B04>
TXA_4_TXCLAV_3 6C2<> 6C2<> B04>
TXCLAV0    7B5<> B05
TXCLAV_0   6C7<> B05
TXDATA_0   6C7<> 7C5<> B84> B85
TXDATA_1   6C2<> 7C4<> B84> B85
TXDATA_2   6C7<> 7C5<> B84> B85
TXDATA_3   6C2<> 7C4<> B84> B85
TXDATA_4   6C7<> 7C4<> B84> B85
TXDATA_5   6C2<> 7C5<> B84> B85
TXDATA_6   6C7<> 7C4<> B01> B02
TXDATA_7   6C2<> 7C5<> B01> B02
TXENA      6C2<> B01>
TXENABLE   7B4<> B02
TXPRTY     6C5<>
TXSOC      6C7<> 7B4<> B81> B82
UOP0       2A6> B81> 11A5>
UOP1       2A6> B01> 11A5>
UOP2       2A6> 11A5>
UOP3       2A6> B04> 11A5>
UR_ADDR0   BDB
UR_ADDR1   BDB
UR_ADDR2   BDB
UR_ADDR3   BCB
UR_ADDR4   BCB
UR_CLAV    BCB
UR_CLK     9B2<> 6A1<> 7A8<> B82<>
UR_DATA0   B8B
UR_DATA1   B8B
UR_DATA2   B8B
UR_DATA3   B8B
UR_DATA4   B8B
UR_DATA5   B8B
UR_DATA6   B8B
UR_DATA7   B8B
UR_ENB     B05
UR_SOC     B05
UR_ADDR0   B05
UR_ADDR1   B05
UR_ADDR2   B05
UR_ADDR3   B05
UR_ADDR4   B05
UR_CLAV    B84>
UR_CLK     9B2<> 6C1<> 7B4<> B82<>
UT_DATA0   B85
UT_DATA1   B85
UT_DATA2   B85
UT_DATA3   B85
UT_DATA4   B85
UT_DATA5   B85
UT_DATA6   B02
UT_DATA7   B02
UT_ENB     B02
UT_SOC     B02
WE_T       4B6<> 5B1<> 7B1<>

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WR_RA      5C4<> 2A3<> 11A3<>
XTALD      2A5> 11A4>

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TITLE: DS2156DK02A0  
ENGINEER: STEVE SCULLY  
DATE: 10/04/02

\*\*\* Part Cross-Reference for the entire design \*\*\*

1	DS2156_TQFP 11D7
C1	CAP 10B5
C2	CAP 10B3
C3	CAP 10B2
C4	CAP 10B2
C5	CAP 10B2
C7	CAP 3D6
C8	CAP 10B4
C9	CAP 10B4
C10	CAP 10B4
C11	CAP 10B4
C12	CAP 10B2
C13	CAP 8A1
C14	CAP 8A1
C15	CAP 10B3
C16	CAP 10B3
C17	CAP 10B2
C18	CAP 10B3
C19	CAP 10B3
C21	CAP 10B2
C22	CAP 10B5
C23	CAP 3A6
C24	CAP 3C5
C25	CAP 3B5
C26	CAP 3A5
C27	CAP 3D5
C29	CAP 10B4
C30	CAP 10B4
C31	CAP 10B6
C32	CAP 10B5
C33	CAP 10B5
C34	CAP 10B5
C35	CAP 10B5
C36	CAP 10B6
DS1	LED 9B4
DS2	LED 5A2
DS3	LED 5A2
DS4	LED 6D5
DS5	LED 5A3
DS6	LED 5A4
DS7	LED 5A3
DS8	LED 5A4
DS9	LED 5A4
DS10	LED 5A3
DS11	LED 5A4
DS12	LED 5A3
DS13	LED 5A3
DS14	LED 5A3
DS15	LED 5A3
DS16	LED 5B5
DS17	LED 5B5
DS18	LED 5A3
F1	FUSE 3B4
F2	FUSE 3B4
F3	FUSE 3D4
F4	FUSE 3C4
F5	FUSE 3D4
F6	FUSE 3A3
J1	CONN_50P1 7D5
J2	CONN_50P1 7D7
J3	CONN_BANTAM_IPC 3B1
J4	CONN_BANTAM_IPC 3C1
J5	CONN_BNC_SPIN 3A3
J6	CONN_BNC_SPIN 3D2
J7	CONN_50P2 6D4
J8	CONN_50P2 4D3
J9	CONN_50P2 4D7
JT10	CONN_10P 5C8
L1	CHOKE_DUAL-T1 3B4 3C4
R1	RES1 4B2
R2	RES 3B7
R3	RES 3B7
R4	RES 6A2
R5	RES 6C2
R6	RES1 5A7

R7	RES 9B4
R8	RES1 5A2
R9	RES1 5A7
R10	RES1 5A7
R11	RES1 5A2
R12	RES 6D5
R13	RES1 5B6
R14	RES1 7B4
R15	RES1 5B6
R16	RES1 5A7
R17	RES1 5B6
R18	RES1 5A6
R19	RES1 5A6
R21	RES1 7A8
R22	RES1 5A7
R23	RES1 5A7
R24	RES1 5B8
R25	RES1 5D7
R26	RES1 5D8
R27	RES1 5D8
R28	RES1 5A7
R29	RES1 5A6
R30	RES 5A3
R31	RES 5A3
R32	RES1 5A6
R33	RES1 8A1
R34	RES1 8A1
R35	RES 5A3
R36	RES 5A3
R37	RES1 5A6
R38	RES 5A7
R39	RES 5A3
R40	RES 5A4
R41	RES 5A3
R42	RES 5A4
R43	RES 5A3
R44	RES1 5A7
R45	RES 5A3
R46	RES1 5B7
R47	RES1 5A7
R48	RES1 5A6
R49	RES1 5A7
R50	RES 5A3
R51	RES 5B4
R52	RES 5B4
R53	RES 5A3
R54	RES1 3B6
R55	RES1 3B6
R56	RES 3B5
R57	RES 3B6
R58	RES 3D7
R59	RES 3C7
R60	RES 3A5
R61	RES1 5A7
RJ1	RJ4B_CON 3C3
SW1	SWITCH_DPDT_SLIDE_6P 3A6
T1	XFMR_2IN_4OUT_U 3B5 3D5
TP1	TSTPNT_SNG 7B2
TP2	TSTPNT_SNG 7B2
TP3	TSTPNT_SNG 7B2
TP4	TSTPNT_SNG 7C2
TP5	TSTPNT_SNG 7C2
TP6	TSTPNT_SNG 7B2
TP7	TSTPNT_SNG 7B2
TP8	TSTPNT_SNG 7B2
TP9	TSTPNT_SNG 7B2
TP10	TSTPNT_SNG 7B2
TP11	TSTPNT_SNG 7B2
TP12	TSTPNT_SNG 5D2
TP13	TSTPNT_SNG 5D2
TP14	TSTPNT_SNG 5A6
TP15	TSTPNT_SNG 5A6
TP16	TSTPNT_SNG 7B2
TP17	TSTPNT_SNG 5D2
TP18	TSTPNT_SNG 5A6
TP20	TSTPNT_SNG 7B2
TP21	TSTPNT_SNG 7B1

TP22	TSTPNT_SNG 7B1
TP23	TSTPNT_SNG 10A7
TP24	TSTPNT_SNG 10A8
TP25	TSTPNT_SNG 10A7
TP26	TSTPNT_SNG 10A7
TP27	TSTPNT_SNG 10A7
TP28	TSTPNT_SNG 10A7
TP29	TSTPNT_SNG 10A7
TP30	TSTPNT_SNG 10A7
TP31	TSTPNT_SNG 10A4
TP32	TSTPNT_SNG 10A4
TP33	TSTPNT_SNG 10A5
TP34	TSTPNT_SNG 10A5
TP35	TSTPNT_SNG 10A5
TP36	TSTPNT_SNG 10A5
TP37	TSTPNT_SNG 10A5
TP38	TSTPNT_SNG 10A5
U1	IDT053R861_U 6B3
U2	IDT053R861_U 6D3
U3	IDT053R861_U 6B6
U4	IDT053R861_U 6D6
U5	XILINX_XC9572XL 5D4 5D7
U6	IDT053R861_U 9B5
U7	IDT053125_U 9D3
U8	IDT053125_U 9D7
U9	IDT053125_U 9B3
U10	IDT053125_U 9B7
U11	DS2156_TQFP 2D7
Z1	SIDACTOR_2 3C4
Z2	SIDACTOR_2 3D5
Z3	SIDACTOR_2 3A5
Z4	SIDACTOR_2 3B5
Z5	SIDACTOR_2 3C6
Z6	SIDACTOR_2 3A4
Z7	SIDACTOR_2 3C4
Z8	SIDACTOR_2 3A4
Z9	SIDACTOR_2 3C4
Z10	SIDACTOR_2 3B4