2ASC-12A2HP – 1200V Dual-Channel Augmented High Performance SiC Core 2

Production Optimized for Silicon Carbide (SiC) MOSFET Modules

Overview

The AgileSwitch® 2ASC-12A2HP – 1200V Dual-Channel Augmented High Performance SiC Core 2 enables better control and protection of most SiC MOSFET-based power systems. The 2ASC-12A2HP provides up to 10A of peak current. This advanced gate drive core includes an isolated DC/DC converter and low capacitance isolation barrier for PWM signals and fault feedback. The Intelligent Configuration Tool (ICT) will allow users to configure the Gate Driver Parameters to their application without having to worry about changing hardware.

Configurable Features

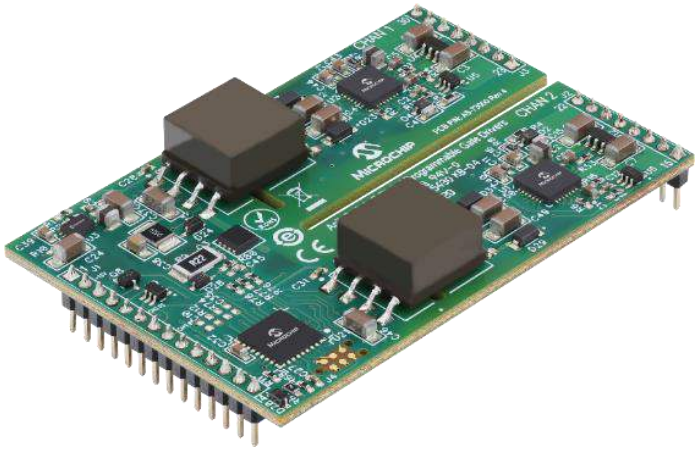
- Augmented Switching™ (Patented)
  - Turn-on
  - Turn-Off
- ± V_{GS} Gate Voltages
  - Vgs Pos from +15V to +21V
  - Vgs Neg from -5V to 0V
- Power supply under-voltage lockout (UVLO)
- Power supply over-voltage lockout (OVLO)
- Desaturation detection settings
- Dead time
- Fault lockout & reset settings

Key Driver Features

- MTBF per MIL-STD-883-1
- Shock & Vibration per IEC60068-2-6
- Temperature Cycling per JEDS22-A104
- UL Compliant - 1200V SiC MOSFET Modules
- Robust High-Noise-Immunity Design
- Isolated Temperature Monitoring, PWM
- Isolated High Voltage Monitoring, PWM
- Compact 40x61mm form factor
- 2 X 3W output power
- RoHS compliant
- Up to 7 Unique fault conditions

Applications

- Heavy Duty Vehicles
- Induction Heating
- Auxiliary Power Units
- Battery Storage
- Inverters
- Wireless Charging



Required Accessory*

Part Number: **ASBK-014** (Device Programmer Kit)
Includes: Microchip PICKIT4, Adapter, Cables, and Intelligent Configuration Tool (ICT) Software
*Not included

Contents

System Overview

The basic topology of the driver core is shown in Figure 1.

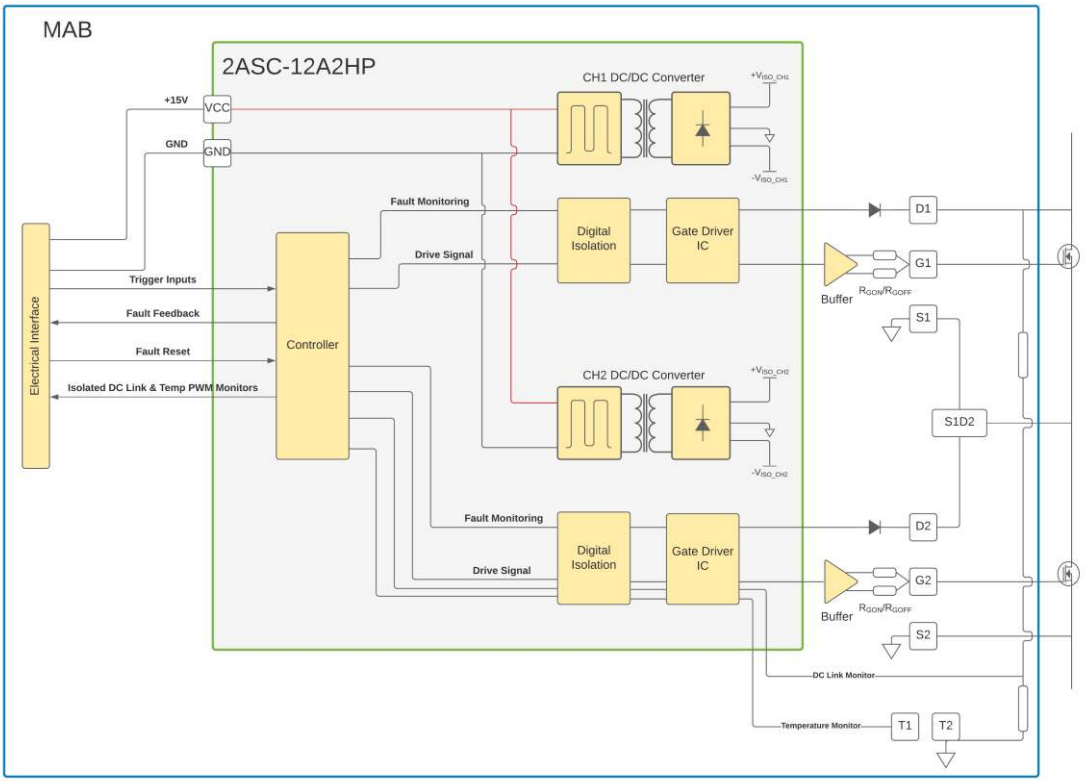


Figure 1: 2ASC-12A2HP Block Diagram

Absolute Maximum Ratings

Interaction of maximum ratings is dependent on operating conditions

Parameter	Description	Min	Max	Unit
Supply Voltage	VCC to GND	0	16.5	V
5V Output	Regulated 5V Power Supply Output		50	mA
Peak Gate Current	Note 2	-10	10	A
Input Logic Levels	To GND	-0.5	5	V
Isolation Voltage	Primary to Secondary VAC RMS 1 min		3750	V
Working Voltage	Primary to Secondary sides Secondary to Secondary sides		1200	V
Creepage Distance	Primary to Secondary sides	8		mm
CMTI	Common-mode transient immunity	100		kV/µs
Operating Temperature	Ambient Operating Temperature	-40	+85	°C
Storage Temperature		-40	+90	°C

Electrical Characteristics

Conditions: V_{SUP} = +15.0 V, V_{IN_LOGIC} = 5V, MOSFET (Ciss = 11.7nF; Qg = 1025nC)

Power Supply	Description	Min	Typ	Max	Unit
Supply Voltage	VCC to GND	14	15	16	V
Supply Current	Without Load		50		mA
Supply Current	With Load, Note 2		250		mA
UVLO Level-HI and LO*	Primary Side low voltage detect fault level	13.2	13.5		V
UVLO Level-HI and LO*	Secondary Side low voltage detect fault level, Note 2	20.2	20.5		V
OVLO Level-HI and LO*	Primary Side high voltage detect fault level		16	16.5	V
OVLO Level-HI & LO*	Secondary Side high voltage fault detect level, Note 2	24.4	24.65		V

Signal I/O	Description	Min	Typ	Max	Unit
Input Impedance	5V - HI and LO side input	1			MΩ
V_{IN} Low	5V - Turn-off threshold			1.25	V
V_{IN} High	5V – Turn-on Threshold	3.5			V
Gate Output Voltage Low*	Note 4	-6		-4	V
Gate Output Voltage High*	Note 4	+17		+21	V
Fault Output Voltage	Fault lines are open collector with 5mA load	0.3		24	V
Fault Output Current	Note 3			10	mA
DC Link & Temp Monitoring	High Voltage (HV) & Temp Monitoring Output	0		5	V
DC Link & Temp Monitoring	PWM Frequency		31.5		kHz
DC Link & Temp Monitoring	Output Impedance, User defined on Adapter Board		510		Ω
DC Link Voltage Trip*	Note 4	0		1100	V
Temperature Trip*	Note 4	25		165	°C

MOSFET Short Protection	Description	Min	Typ	Max	Unit
Desat Monitor Voltage*	Between Drain and Sink of MOSFET, Note 2, Note 4	3	4.5	10	V
T_{DSAT}*	Activation after MOSFET Turn on, Note 4	500	730	1750	ns
Response Time after Fault				200	ns

Note 1: Input signal should not be activated until 20 ms after power is applied to allow on board DC-DC converter to stabilize.
Note 2: SiC MOSFET dependant, conditions listed above assume MOSFET with Ciss = 11.7nF; Qg = 1025nC operating at 50kHz
Note 3: Fault lines are open collector and require a pull-up resistor, 2kΩ recommended
Note 4: Software configurable
***Note:** For Software configurable parameters, the available range of values are listed in the table

Interconnects

Module Adapter to Driver Core Connectors

Ref	Connector	Type	Manufacturer Part Number
J1	Input	14 Pin, 2mm pitch spacing	NRPN141PAEN-RC
J2, J3	Ch 1, Ch 2	8 Pin, 2mm pitch spacing	NRPN081PAEN-RC

Core Programming Adapter

Ref	Connector	Type	Manufacturer Part Number
J4	Programming	6 Pin, 1.27mm pitch spacing	TC2030-IDC-NL

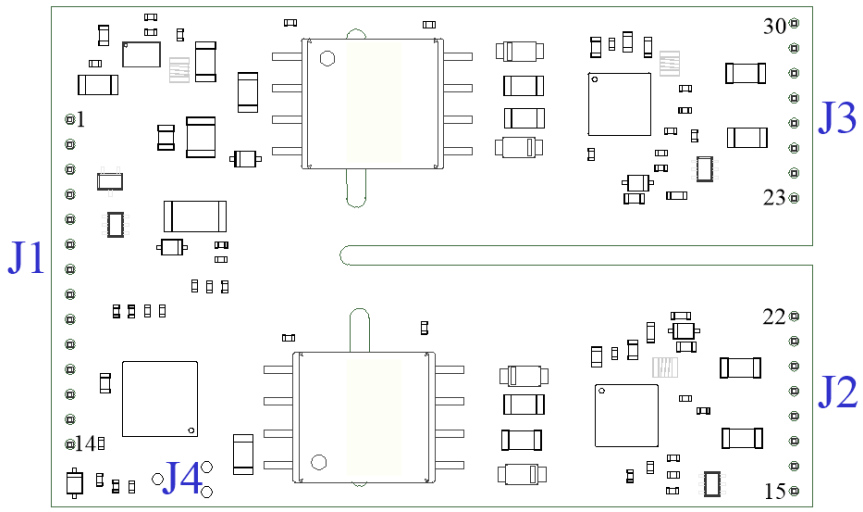


Figure 2: Interconnect Locations on PCB

Core Assembly on Adapter Board

Method 1 - Soldering

2ASC-12A2HP can be directly soldered onto an Adapter Board without the need for additional support.

Method 2 – Socket

2ASC-12A2HP can be plugged into female sockets on an Adapter Board.

Recommended Sockets

Ref	Connector	Type	Manufacturer Part Number
J1	Input	14 Pin, 2mm pitch spacing	NPPN141BFCN-RC
J2, J3	Ch 1, Ch 2	8 Pin, 2mm pitch spacing	NPPN081BFCN-RC

Pinout – Controller/Power to Driver Connection

14 PIN – J1 – Primary Side Connector

Pin No	Signal	Function
1	VCC	+15V Supply Voltage
2	VCC	+15V Supply Voltage
3	+5V Out	+5V Output to drive primary side electronics
4	AL-F	All Faults Output
5	CH2-F	Channel 2 Fault Output
6	CH2-Trig	Channel 2 Trigger Input
7	CH1-F	Channel 1 Fault Output
8	CH1-Trig	Channel 1 Trigger Input
9	TE-P	Non-Isolated Temperature Monitoring Input
10	HV-F	Isolated DC Link Voltage Monitoring Output
11	TE-F	Temperature Monitoring Output
12	F-RS	Fault Reset (Auto Reset Optional)
13	GND	Ground
14	GND	Ground

8 PIN – J2 – Channel 2 (CH2)

Pin No	Signal	Function
15	CH2_DC	Isolated DC Link Monitor Input
16	CH2_Temp	Isolated Temperature Monitor Input
17	CH2 – (-)V_Sec	Negative Secondary Voltage
18	CH2_Sink	Sink
19	CH2_Source	Source
20	CH2_GND	Ground
21	CH2 – (+)V_Sec	Positive Secondary Voltage
22	CH2 DSAT	Vds Monitor

8 PIN – J3 – Channel 1 (CH1)

Pin No	Signal	Function
23	CH1 DSAT	Vds Monitor
24	CH1 – (-)V_Sec	Negative Unregulated Voltage
25	CH1_GND	Ground
26	CH1_Sink	Sink
27	CH1_Source	Source
28	CH1 – (+)V_Sec	Positive Unregulated Voltage
29	CH1_DC	Isolated DC Link Monitor Input
30	CH1_Temp	Isolated Temperature Monitor Input

Recommended Interface Circuitry

Primary

Block Diagram

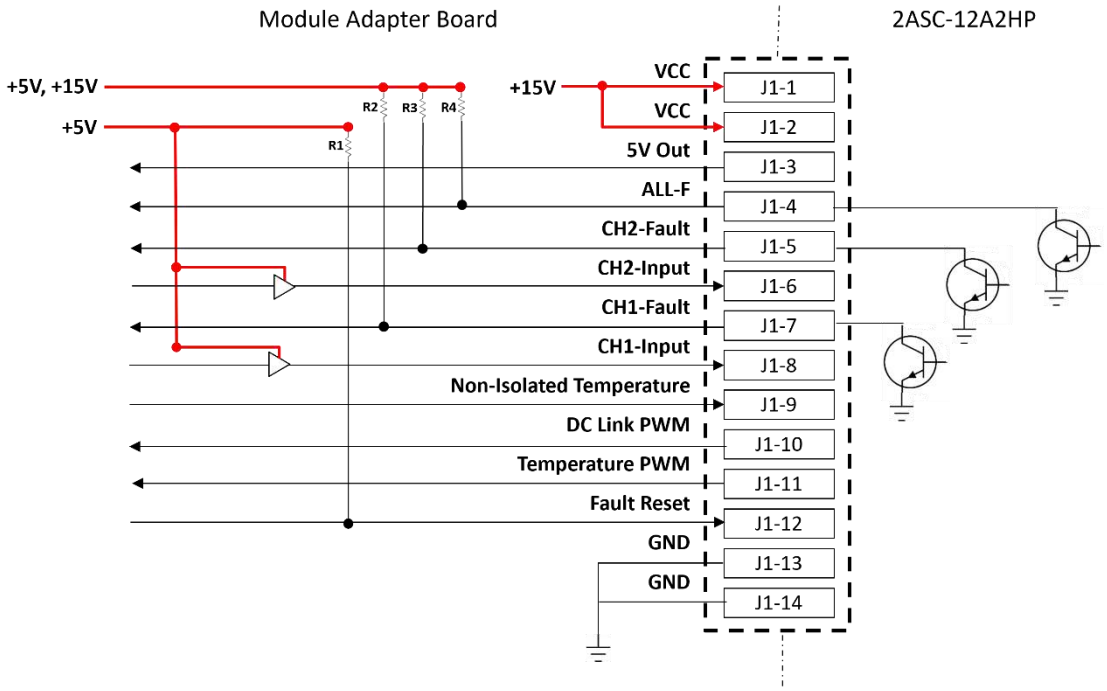


Figure 3 Input 14-Pin pinout diagram for 2ASC-12A2HP SiC Driver Core

Buffer Schematic for Inputs on the Module Adapter Board

The 2ASC-12A2HP is designed to accept only 5V single ended input logic. The Module Adapter Board can buffer other input logic levels to make them compatible with the 2ASC-12A2HP. Examples of 5V differential and 15V single ended buffer circuits are shown below.

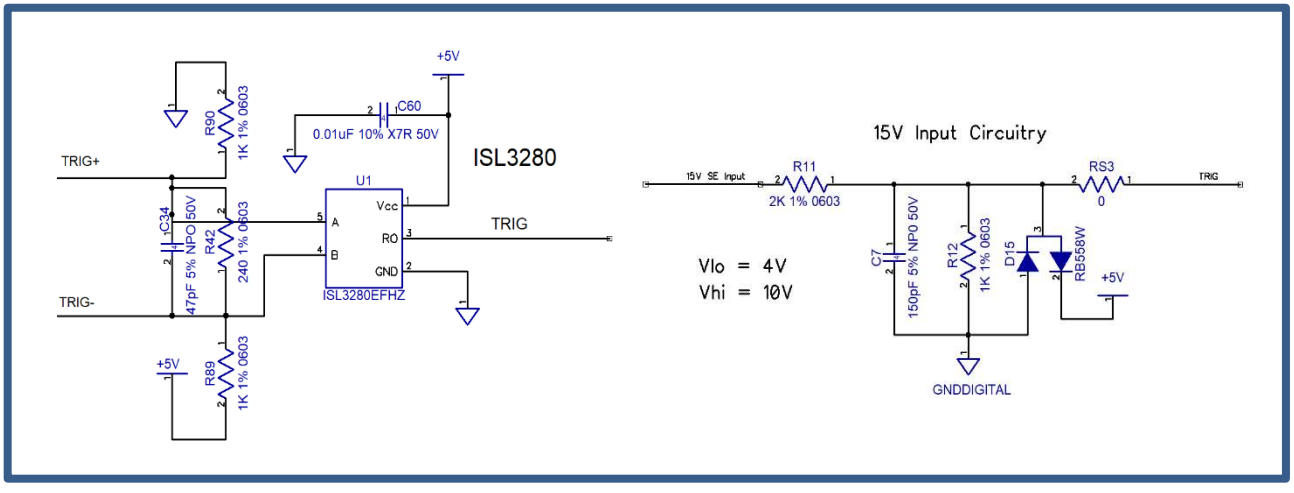


Figure 4 Input buffers on Module adapter board for differential & 15V Single Ended Inputs

Secondary

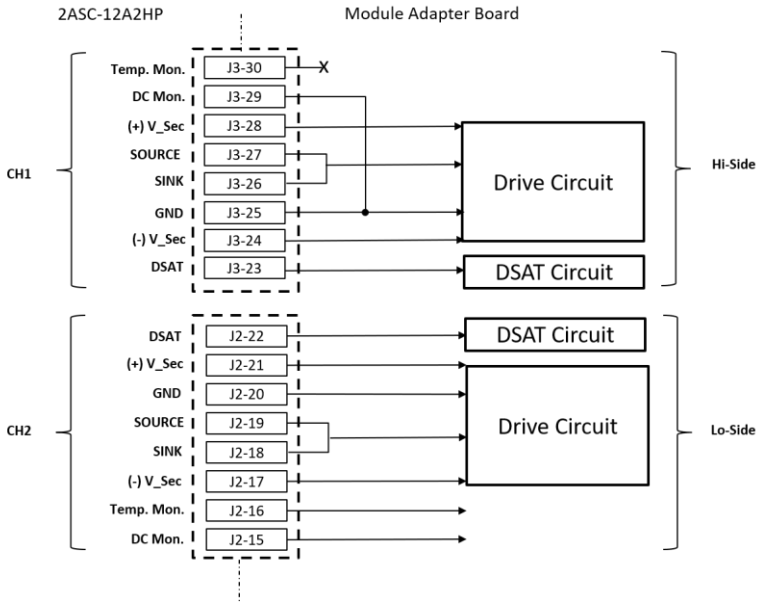


Figure 5 Output pinout diagram for 2ASC-12A2HP SiC Driver Core

Channels 1 & 2 can be used interchangeably as the HI or LO side.
On the Hi side temperature line should be floating & DC monitor should be grounded.

Drive Circuit

Gate Voltage (Vgs) limiting Zener diodes are recommend limiting the exposure of the SiC MOSFET Gate to high voltage transients. The Zener diodes should be chosen based on the Vgs ratings of the SiC MOSFET.

The 2ASC-12A2HP has separate Source & Sink outputs to separate the charging and discharging paths.

The below equation can be used to estimate the drive current required for a given SiC MOSFET module:

$$I_g peak = \frac{V_{gs+} + V_{gs-}}{Rg + RG}$$

$I_g peak$ – Peak Gate Current
V_{gs+} – Positive Gate Voltage recommended by the SiC MOSFET Manufacturer
V_{gs-} – Negative Gate Voltage recommended by the SiC MOSFET Manufacturer
Rg – SiC MOSFET Module Internal Gate Resistance
RG – External Gate Resistance on the Module Adapter Board

Note: $I_g peak$ is a strong function of the module gate charge
In the implementation shown below in Figure 6, a totem pole driver provides the 2ASC-12A2HP with ~10A peak current.

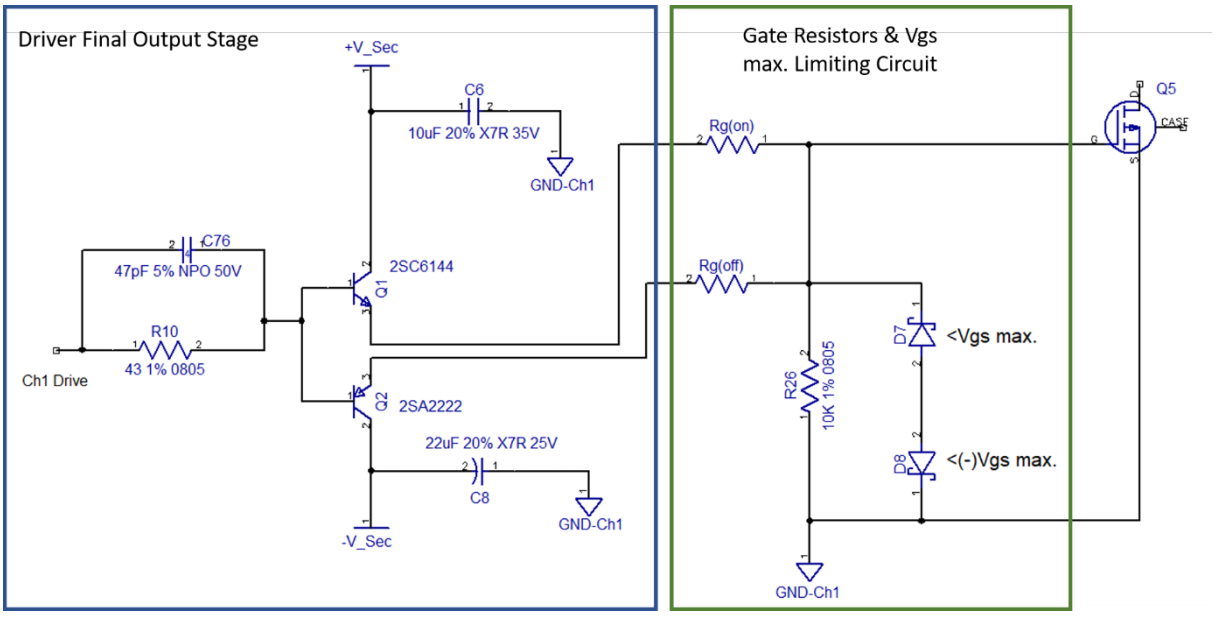


Figure 6 Recommended Hi-Side Drive Circuit for 2ASC-12A2HP SiC Driver Core

Short Circuit Protection - DSAT Circuit

SiC devices are limited in their Short Circuit withstand capability of 2-3us. It is therefore important to adopt the appropriate short circuit protection parameters for the Gate Driver.
DSAT Blanking time and DSAT threshold voltage are two such important parameters and are software configurable features on the 2ASC-12A2HP.

DSAT protection with sense diodes is the recommended method, shown below in Figure 7.
The DSAT lines are pulled up to +V_Sec via a 10kΩ pull up resistor on the 2ASC-12A2HP.

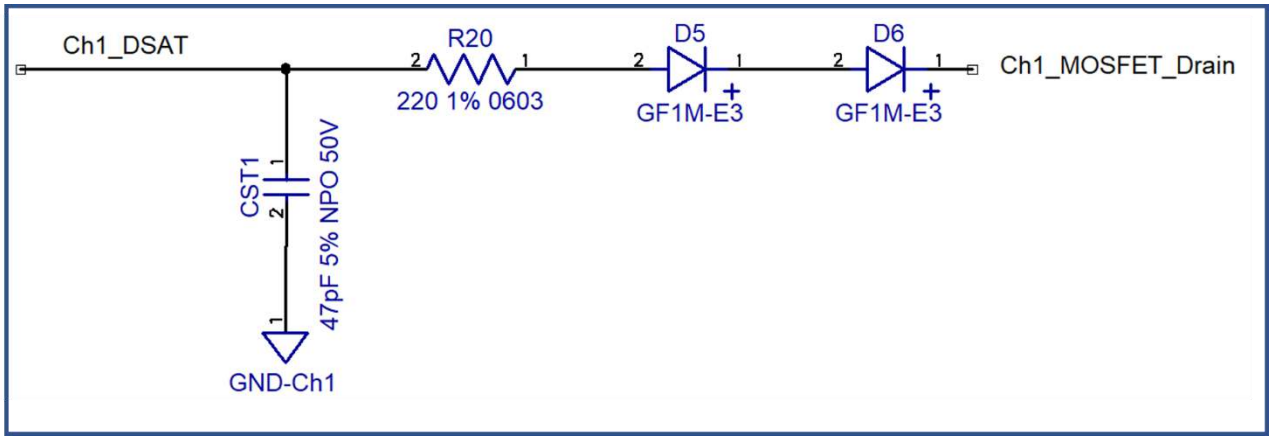


Figure 7 Recommended DSAT Sense Circuit for 2ASC-12A2HP SiC Driver Core

DC Link monitor

The 2ASC-12A2HP also features isolated DC Link Voltage monitoring and protection.

The 2ASC-12A2HP DC Link Monitor circuit performs two functions:

- Compares this monitored value against the DC Link Fault Threshold
- Converts the DC Link Voltage into a PWM

The resistor divider circuit shown in Figure 8 is recommended.

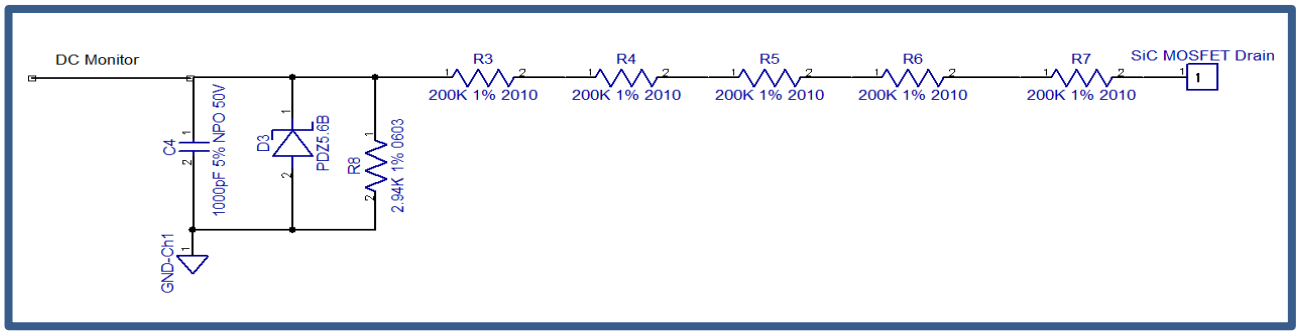


Figure 8 Recommended DC Link Monitor Circuit for 2ASC-12A2HP Core

Timing Diagrams

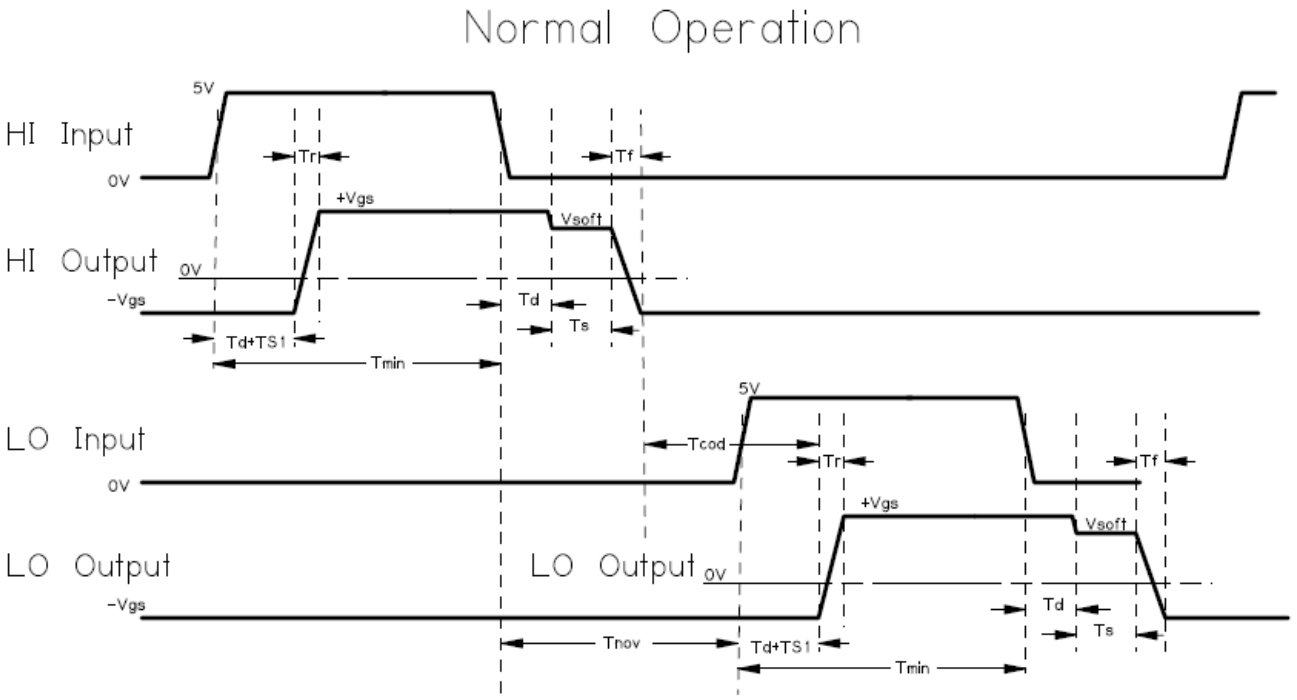


Figure 9 Signal input and output timing diagram.

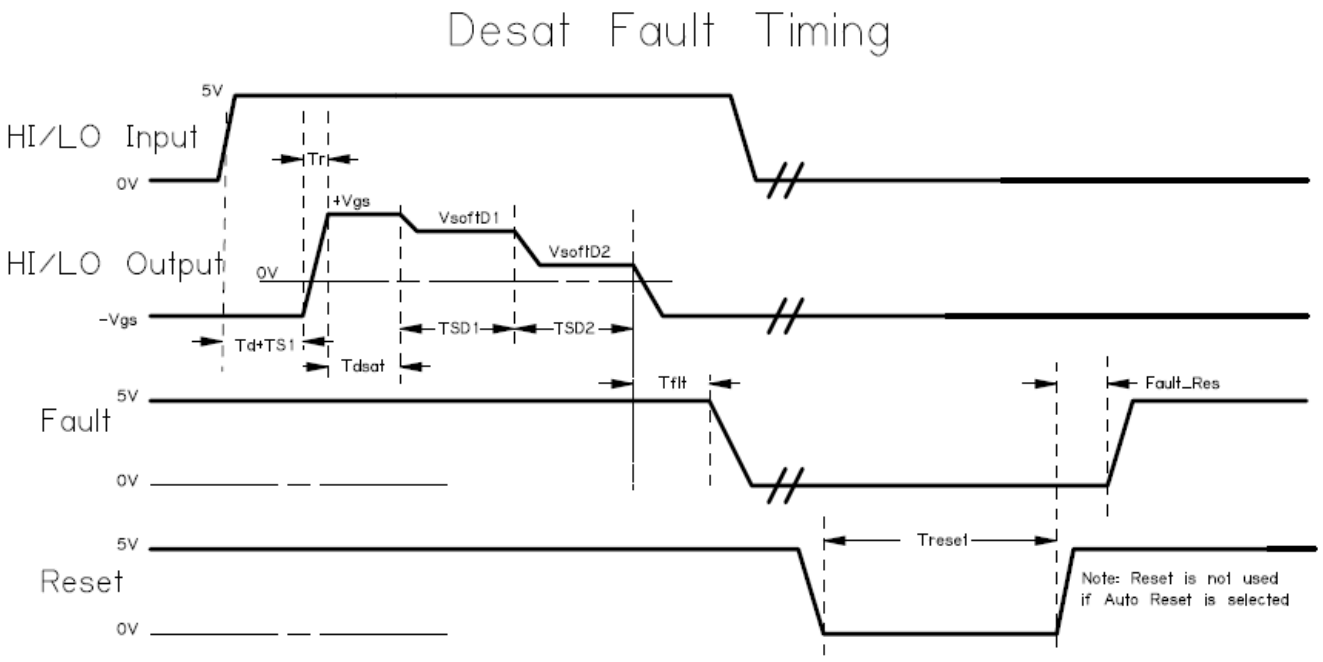


Figure 10 Signal desaturation and fault diagram.

Timing Diagram Values

Conditions: V_{SUP} = +15.0 V, Temp = 0 ºC to 85 ºC

Description	Symbol	Min	Typ	Max	Unit	Notes
Minimum Pulse Width	T_{MIN}	T_{S1}			ns	The minimum pulse width is a factor of the 2-Level Turn-Off Time
Delay Time	T_D			250	ns	
De-Glitch Time			200		ns	Input signal de-glitch time
Rise Time	T_R		80		ns	Measured from 10% to 90% points on edge Measurement Point 1 – Fig. 10
Fall Time	T_F		90		ns	Measured from 10% to 90% points on edge Measurement Point 2 – Fig. 10
2-Level Turn-Off Time	T_{S1}		360		ns	Software configurable
2-Level Turn-Off Voltage	Vsoft		1.5		V	Software configurable
Desaturation Time	T_{DSAT}	1400	1500	1600	ns	Software configurable
1st DSAT V	Vsoft D1		9		V	Multi-Level Turn-Off – First DSAT Step
First DSAT Time*	TSD1		400		ns	First DSAT 2-level turn-off time
2nd DSAT V	Vsoft D2		5		V	Multi-Level Turn-Off – Second DSAT Step
Second DSAT Time*	TSD2		200		ns	Second DSAT 2-level turn-off time
Fault Time Delay	T_{FLT}		5000		ns	
Fault Reset	Fault_Res		1000		ns	
Fault Response Time	T_{RESP}		200		ns	
Dead Time - Input	T_{NOV}		1000		ns	Recommended Minimum Time between Inputs
Dead Time – Driver	Tcod	1000			ns	Minimum Time between drive signals allowed by driver, software configurable
Reset Timing	Treset	1000			ns	Minimum Reset Time
Automatic Reset (Optional)			5		ms	Standard setting of 5 ms

*Note 2

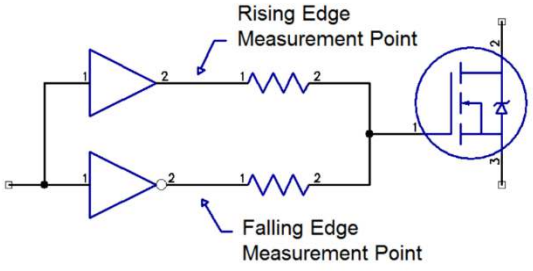


Figure 11 Measurement points for rise and fall time

Temperature and High Voltage PWM Monitoring

The AgileSwitch 2ASC-12A1HP Driver provides two 31.5 kHz, 5.0V PWM output signals that monitor the thermistor temperature (isolated or non-isolated) and the DC Link Voltage (High Side drain to Low Side source) of the SiC MOSFET power module. The recommended output impedance for the PWM signals is 510Ω. When combined with an external low pass filter, these signals represent a real time, voltage for both High Voltage and Thermistor Temperature. A Sallen-Key active low pass filter can be used with these outputs as shown below with a 2 kHz cut-off frequency. The cut-off frequency can be optimized for your application. For simplicity, a simple RC low pass filter with 100 Hz cut-off frequency can also be used.

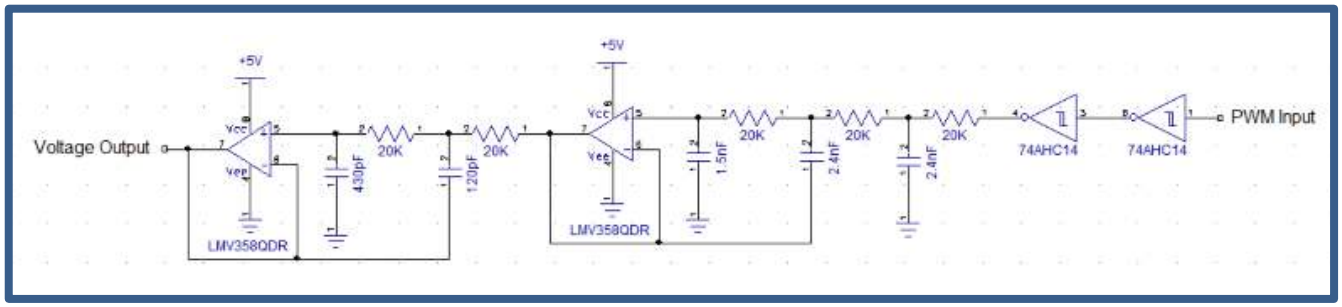


Figure 2 Example of a 2kHz Low Pass Filter

Temperature Monitor

The 2ASC Series Cores feature isolated and non-isolated temperature monitor inputs. The isolation designation refers to the processing of the temperature information at the gate driver level. The isolated temperature monitor senses temperature on the high-voltage side of the board; this information is sent across the digital isolator and output as a PWM signal on TE-F, Temperature Monitoring Output. The non-isolated temperature monitor provides the same PWM information on TE-F, but it senses temperature on the low-voltage side of the board; therefore, the thermistor must be externally isolated if using the non-isolated temperature monitor.

The isolated temperature monitor is recommended. It is at the user's discretion to determine the best approach for their application.

The Intelligent Configuration Tool (ICT) gives the user the ability to select the monitoring type and thermistor characteristics. The thermistor characteristics required to configure the temperature monitor are the Beta (β) value and a reference point. The reference point is typically expressed as a resistance at 25 °C. These values can be found on the thermistor or SiC module data sheet.

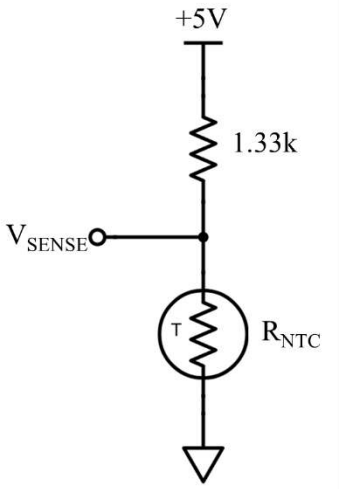
For users looking for an external thermistor recommendation, Microchip recommends USUR1000-502G.

Temperature Monitor Inputs

There are three temperature monitor inputs on a 2ASC-12A1HP – CH1_Temp, CH2_Temp, and TE-P.

CH1_Temp, CH2_Temp – Isolated Temperature Monitor Inputs

There is an internal 1.33 kΩ pull-up resistor connected to CH1_Temp and CH2_Temp. Connecting one of the thermistor pins to the temperature sense pin and other thermistor pin to the LO Side ground forms a voltage divider, as shown below. Temperature monitoring should always be managed only on the Channel driving the LO side, or bottom, switch.

Schematic	Equation
	$V_{SENSE} = 5\left(\frac{R_{NTC}}{R_{NTC} + 1330}\right)$

With the known pull-up value and temperature-resistance curve for the thermistor, the output voltage of this divider can be converted to temperature. The 2ASC Series Cores perform these calculations, converting the sensed voltage to the corresponding temperature for the configured thermistor characteristics. This information is transmitted across the digital isolation boundary and output on the temperature monitoring pin (TE-F) as a PWM signal. The output PWM duty cycle scales linearly across the configured temperature range, with 0% corresponding to the minimum temperature and 100% with the maximum temperature. To convert the filtered output voltage to temperature, the following equation can be used:

$$T = T_{MIN} + (T_{MAX} - T_{MIN})\left(\frac{V_{OUT}}{V_{FSR}}\right) = T_{MIN} + (T_{MAX} - T_{MIN})D$$

where T_{MIN} and T_{MAX} are the configured sense limits, V_{OUT} is the measured output voltage, V_{FSR} is the full-scale voltage range, and D is the duty cycle ratio. Note that the ratio V_{OUT}/V_{FSR} is the same as the duty cycle ratio.

For example, suppose a 2ASC Series Core has been configured for a temperature sensing range of 25 °C to 125 °C, and the output waveform shows a duty cycle of 40%. The measured temperature is then 25+100*0.4, or 65 °C.

TE-P – Non-Isolated Temperature Monitor Input

The same equations and calculations apply to the non-isolated temperature monitor. The key difference is that there is not an internal 1.33 kΩ pull-up resistor connected to TE-P on the 2ASC Series Core. The user is expected to include this on their adapter board. It is already provided if using a Microchip Module Adapter Board (MAB) designed for a device without an integrated thermistor. An example is the 62CA1 which is designed for the D3/62mm package.

DC Link Voltage Monitor

The DC Link (HI Side drain to LO Side source) Monitor Output Voltage is 1% accurate from 50V to 1650V. The PWM output is the ratio of the DC Link Voltage / 1700V. For example, an 825V DC Link Voltage, the PWM output will be 50%. The linear equation for the Voltage Monitor PWM Output with a 2 kHz 4 pole filter is:

$$V_{DC}[V] = 340\ X\ Vmonitor$$

Fault and Monitoring Conditions

Fault Condition/Action	Generic Sample Default Trigger Values	Action if Active (Default Setting)	Faults Low Active			Faults High Active		
			HI Fault	LO Fault	All Faults	HI Fault	LO Fault	All Fault
NO FAULTS	N/A	N/A	HIGH	HIGH	HIGH	LOW	LOW	LOW
DSAT/UVLO – HI	See Electrical Characteristics	Turn Off HI & LO Side	LOW	HIGH	LOW	HIGH	LOW	HIGH
DSAT/UVLO – LO	See Electrical Characteristics	Turn Off HI &LO Side	HIGH	LOW	LOW	LOW	HIGH	HIGH
OVLO	See Electrical Characteristics	Turn Off HI & LO Side	HIGH	HIGH	LOW	LOW	LOW	HIGH
Temperature Fault	Thermistor temperature above setting	No Action	HIGH	HIGH	LOW	LOW	LOW	HIGH
DC Link Voltage Fault	DC Link Voltage above setting	Turn Off HI & LO Side	HIGH	HIGH	LOW	LOW	LOW	HIGH
Power On Configuration Fault*	Failure to Configure Gate drivers	Turn Off HI & LO Side	LOW	LOW	LOW	HIGH	HIGH	HIGH

*After power up, if all Fault lines are Active, then either there is a real fault (UVLO/DSAT) on both the HI and LO sides or there has been a software configuration failure.

Important Precautions

Caution: Handling devices with high voltages involves risk to life. It is imperative to comply with all respective precautions and safety regulations.

When installing the core and adapter board, please make sure that power is turned off. Hot swapping may cause damage to the IC components on the board.

Microchip assumes that the core and adapter board have been mounted on the SiC MOSFET prior to start-up testing. It is recommended that the user checks that the SiC MOSFET power modules are operating inside the Specified Operating Area (SOA) as specified by the module manufacturer including short circuit testing under very low load conditions.

Configurable Parameters

Easily configure and fine-tune the performance of AgileSwitch® Digital Gate Drivers to meet the requirements of your application. The Intelligent Configuration Tool (ICT) is all you need to adjust the software-configurable parameters to optimize your system's performance.

Visit Microchip.com - Intelligent Configuration Tool for details.

Reference Designs

Microchip has developed Reference Module Adapter Boards for the 2ASC-12A1HP. The design files for these adapter boards can be found here.

Mechanical Dimensions

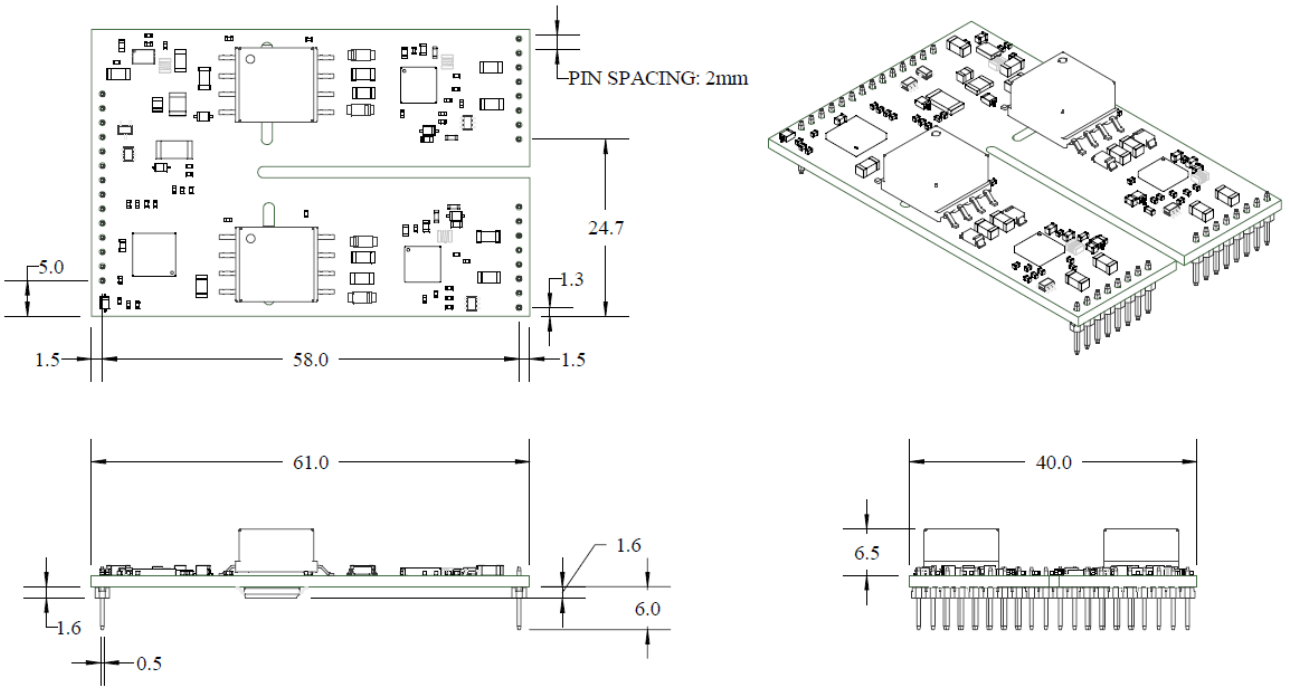


Figure 13: Dimensions of the 2ASC-12A2HP Core(+/- 0.1mm)

Dimensions are in mm.

Download the full drawing and model for additional details. * (Coming Soon)

Revisions

Version	Date	Description
1	4/8/2021	Preliminary Release
2	5/3/2021	Modifications to Electrical table
3	8/4/2021	General updates for commercial release
4	9/16/2021	General updates for commercial release

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Patent Notices

Offering	Issued U.S. Patent Numbers
AgileStack™ Power stack control systems	8,984,197
Gate drive control system for SiC and IGBT power devices	9,490,798
Additional Patents Pending	

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