TLV70433DBVEVM-712, TLV70433PKEVM-712 Evaluation Modules

This user’s guide describes the characteristics, operation, and use of the TLV70433DBVEVM-712 and the TLV70433PKEVM-712 evaluation modules (EVM) as a reference design for engineering demonstration and evaluation of the Texas Instruments' TLV70433 low-dropout linear regulator (LDO). This user’s guide includes setup instructions, a schematic diagram, layout and thermal guidelines, a bill of materials (BOM), printed circuit board (PCB) layout drawings, and test results for the evaluation module. Throughout this document, the abbreviation *EVM* and the term *evaluation module* are synonymous with the TLV70433DBVEVM-712 and the TLV70433PKEVM-712 EVMs, unless otherwise noted.

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1 Introduction

The TLV70433DBVEVM-712 and TLV70433PKEVM-712 EVMs help design engineers to evaluate the operation and performance of the TLV704xx family of linear regulators for possible use in their own circuit applications. The PCB itself contains two LDO footprints to allow either the DBV (SOT23-5) or PK (SOT89) packages to be installed. This particular EVM configuration contains a single, fixed (3.3-V output) linear regulator designed for ultralow quiescent current across its full load range. The regulator, including external components, is capable of delivering up to 150 mA to the load depending on the input-output power dissapation across the device. The TLV704xx does not require an input capacitor the output capacitor must only be 1 μF (effective minimum) for stability; however, for conservative design practice that accounts for a wide variety of noisy environments, dynamic line conditions, and the possible use of long reactive power leads attached to the EVM input, a 1-μF capacitor is installed.

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2 Setup

This section describes the connectors and ground connections found on the EVM as well as how to properly connect, set up, and use the TLV70433DBVEVM-712 or TLV70433PKEVM-712.

2.1 Input / Output Connectors, Jumper, and Resistor Descriptions

J4: VIN

The positive input lead and ground return lead from the input power supply should be twisted and kept as short as possible to minimize electromagnetic interference (EMI) transmission. Additional bulk capacitance should be added between J4 and J2 (GND) if the supply leads are greater than 6 in (15.24 cm) in length. For example, an additional leaded 47-μF electrolytic capacitor connected from J4 to J2 (GND) improves the transient response of the TLV70728 by eliminating unwanted ringing that sometimes occurs as a result of long wire connections.

J2: GND

This is the ground-return connection for the input power supply.

J5: VOUT

This is the regulated output voltage connector.

J1: GND

This is the output ground-return connector.

J3

This test jack/jumper is used to do one of the folllowing:

- Measure the LDO ground or quiescent current; or
- When connected by a shorting strip (not provided with the EVM), to provide an alternative means to ground either of the LDO packages when R_1 or R_2 is not installed.

R1 and R2

0-Ω resistors that connect the ground pin of either respective LDO package (SOT89 or SOT23) to the ground plane. If this resistor is removed, then this ground connection must be made across the J3 test jack/jumper using a shorting strip (not provided with the EVM).

2.2 Soldering Guidelines

Any solder re-work to modify the EVM for the purpose of repair or other application reasons must be performed using a hot-air system to avoid damaging the integrated circuit (IC).

2.3 Equipment Setup

Follow these procedures to set up the test equipment properly.

- Turn off the input power supply after verifying that its output voltage is set to less than 24 V. Connect the positive voltage lead from (+) the input power supply to V_{IN}, at the J4 connector of the EVM. Connect the ground lead from the (–) input power supply to GND at the J2 connector of the EVM.
- Connect a 0-mA to 150-mA load between the output (V_{OUT}) at connector J5 and ground at connector J1.

3 Operation

Follow these procedures to correctly operate the TLV70433DBVEVM-712 or TLV70433PKEVM-712.

- Turn on the input power supply. For initial operation, it is recommended that the input power supply, V_{IN} – J4, be set between 5 V and 10 V.
- Vary the respective loads and V_{IN} voltages as necessary for test purposes.

4 LDO Ground Current Measurement

The LDO ground, or quiescent current (isolated from the load current), can be measured after taking these steps:

Step 1. Turn off the input power supply.

Step 2. Remove the 0-Ω resistor R1 on the TPS70433PKEVM-712 EVM (or R2 on the TPS70433DBVEVM-712 EVM).

Step 3. Connect a current meter across pin 1 of J3 and pin 2 of J3.

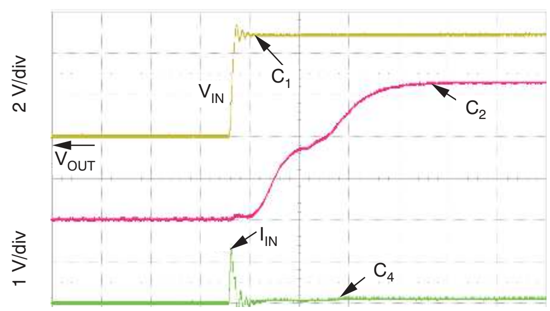
Step 4. Turn on the power supply, as disussed in Section 3.

5 Test Results

This section provides typical performance waveforms for the TLV70433DBEVM-712 and the TLV70433PKEVM-712.

5.1 Turn-On Sequence

Figure 1 shows the turn-on characteristic of the LDO. V_{IN} (C_1, yellow) quickly transitions to 5.0 V to turn on the LDO. The output voltage, V_{OUT} (C_2, red), then ramps up to its nominal 3.3-V output in accord with the control loop design after the input current surge I_{IN} (C_4, green) has sufficiently charged the input and output capacitors.



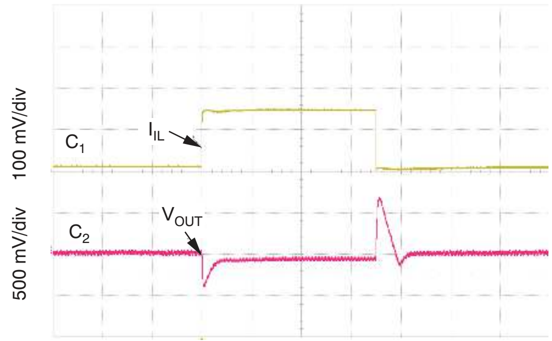
Note:

- C_1, V_{IN}: turn-on to 5 V;
- C_2, V_{OUT}: 3.3-V turn-on ramp;
- C_3, Input rush current at turn-on

Figure 1. Turn-On Sequence

5.2 Output Load Transient

Figure 2 illustrates the output voltage transient response to a load step transient of 10 mA to 150 mA. Oscilloscope channel C_1 shows the current step and channel C_2 shows the V_{OUT} voltage response



Note:

- C_1: Load step of 10 mA to 150 mA;
- C_2, V_{OUT}: Output voltage transient response.

Figure 2. Step Load and Transient Response

6 Thermal Guidelines and Layout Recommendations

Thermal management is a key design component of any power converter, and is especially important when the power dissipation in the LDO is high. Use Equation 1 to approximate the maximum power dissipation for a given ambient temperature.

$$T_J = T_A + P_D \bullet \theta_{JA}$$

Where:

T_J = junction temperature

T_A = ambient temperature

P_D = power dissipation in the IC (in watts)

θ_{JA} = thermal resistance from junction to ambient (1)

All temperatures are in degrees Celsius (°C).

The maximum silicon junction temperature, T_J, must not be allowed to exceed +125°C. The layout design must use copper trace and plane areas effectively as thermal sinks, in order not to allow T_J to exceed the absolute maximum ratings under all temperature conditions and voltage conditions across the application.

Designers should carefully consider the thermal design of the PCB for optimal performance over temperature. For this EVM, Figure 3 illustrates one way in which the V_{IN} plane, connected to pin 2 of both the SOT89 and SOT23 package, can be used to thermally cool the LDO by sinking dissipated power. The PCB is a two-layer board with 2-oz. copper on top and bottom layers.

7 Board Layout

This section provides the TLV70433DBVEVM-712 and the TLV70433PKEVM-712 board layout and schematic.

7.1 Layout

NOTE: Board layouts are not to scale. These figures are intended to show how the board is laid out; they are not intended to be used for manufacturing TLV70433DBVEVM-712 and the TLV70433PKEVM-712 PCBs.

Figure 3 through Figure 5 show the PCB layouts.

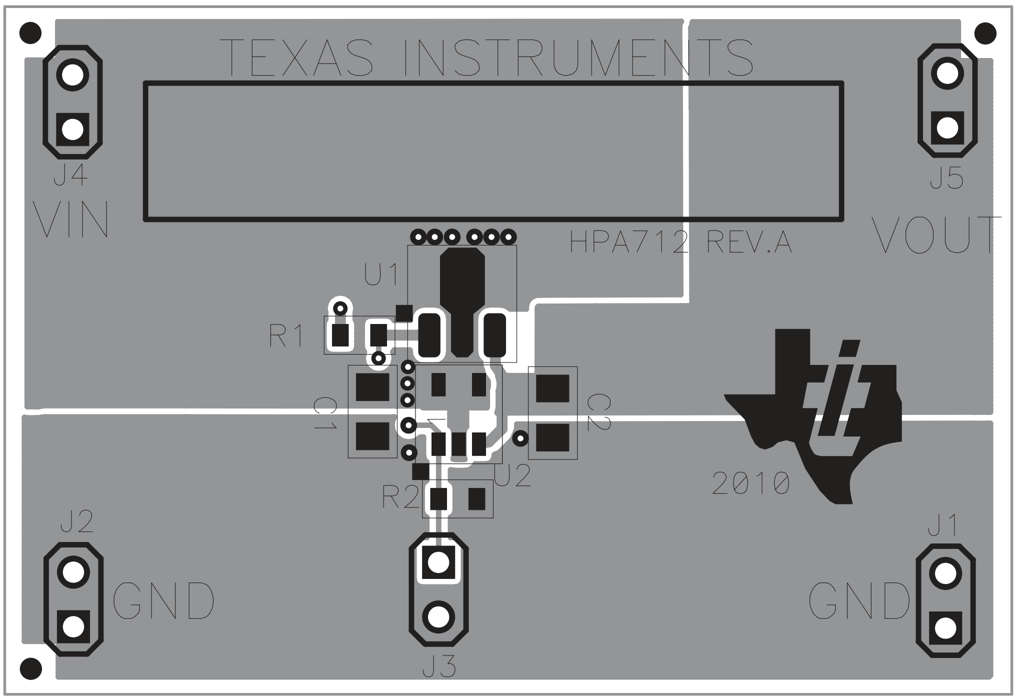


Figure 3. Assembly Layer

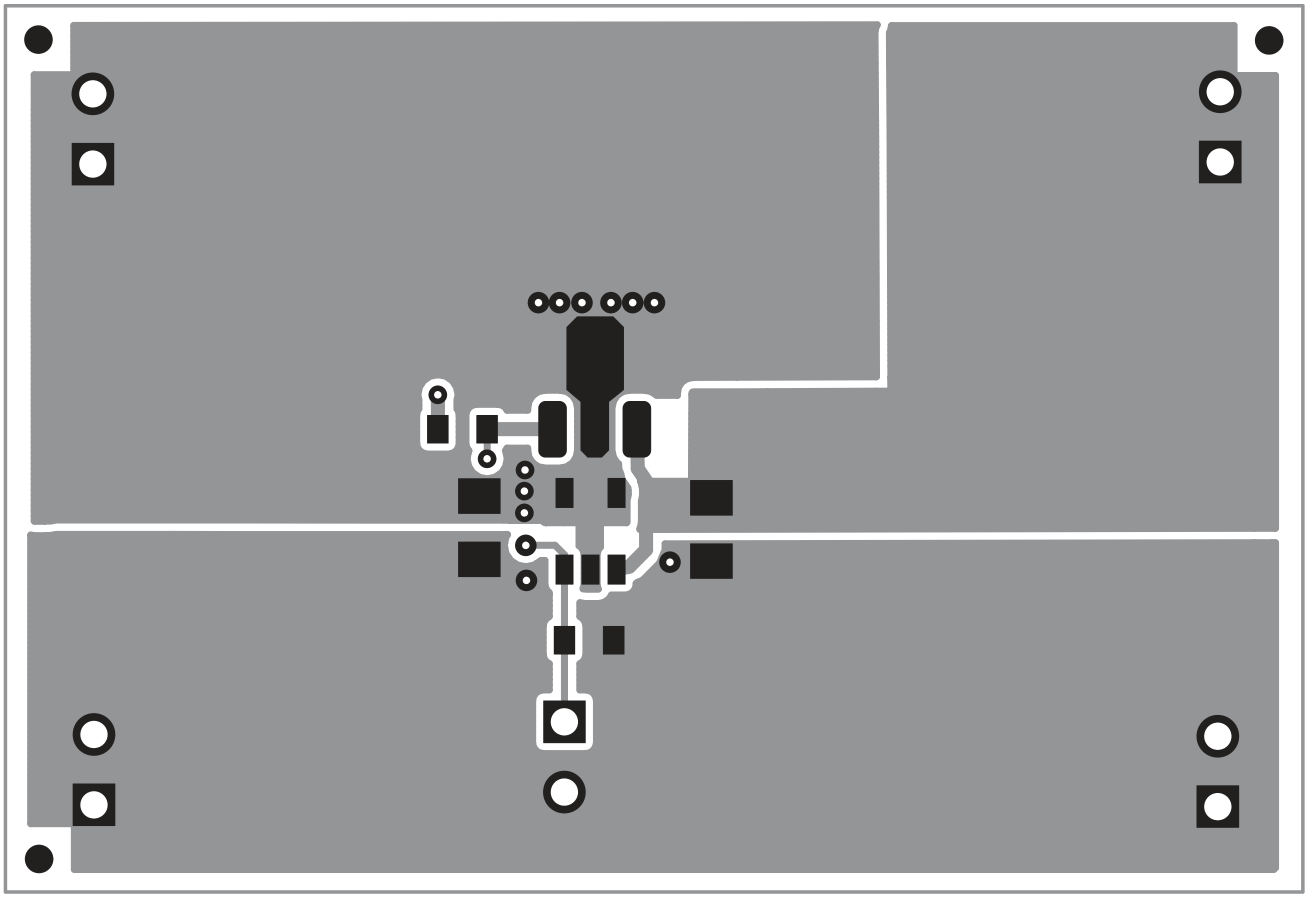


Figure 4. Top Layer Routing

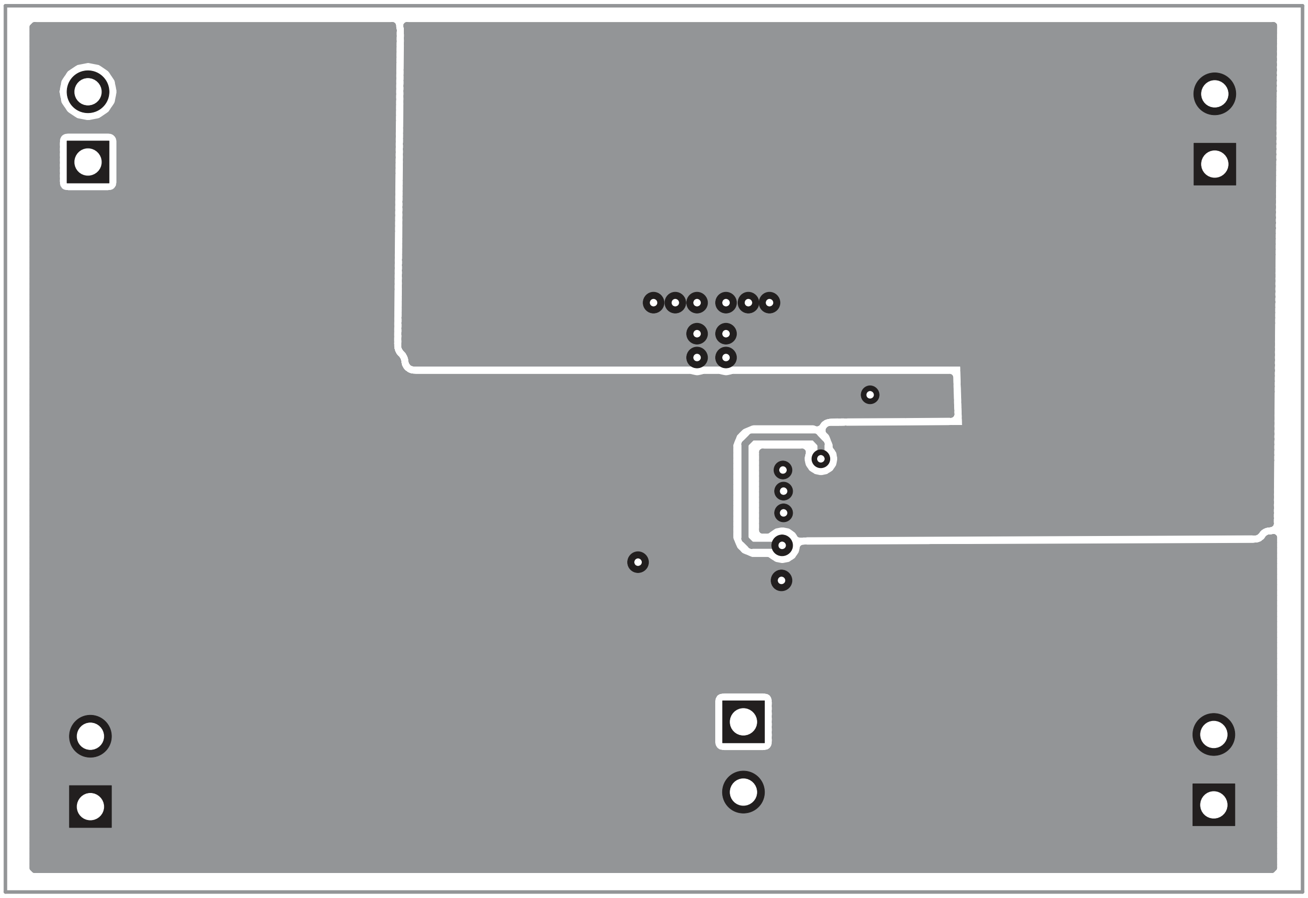


Figure 5. Bottom Layer Routing

7.2 Schematic

Figure 6 illustrates the schematic for this EVM.

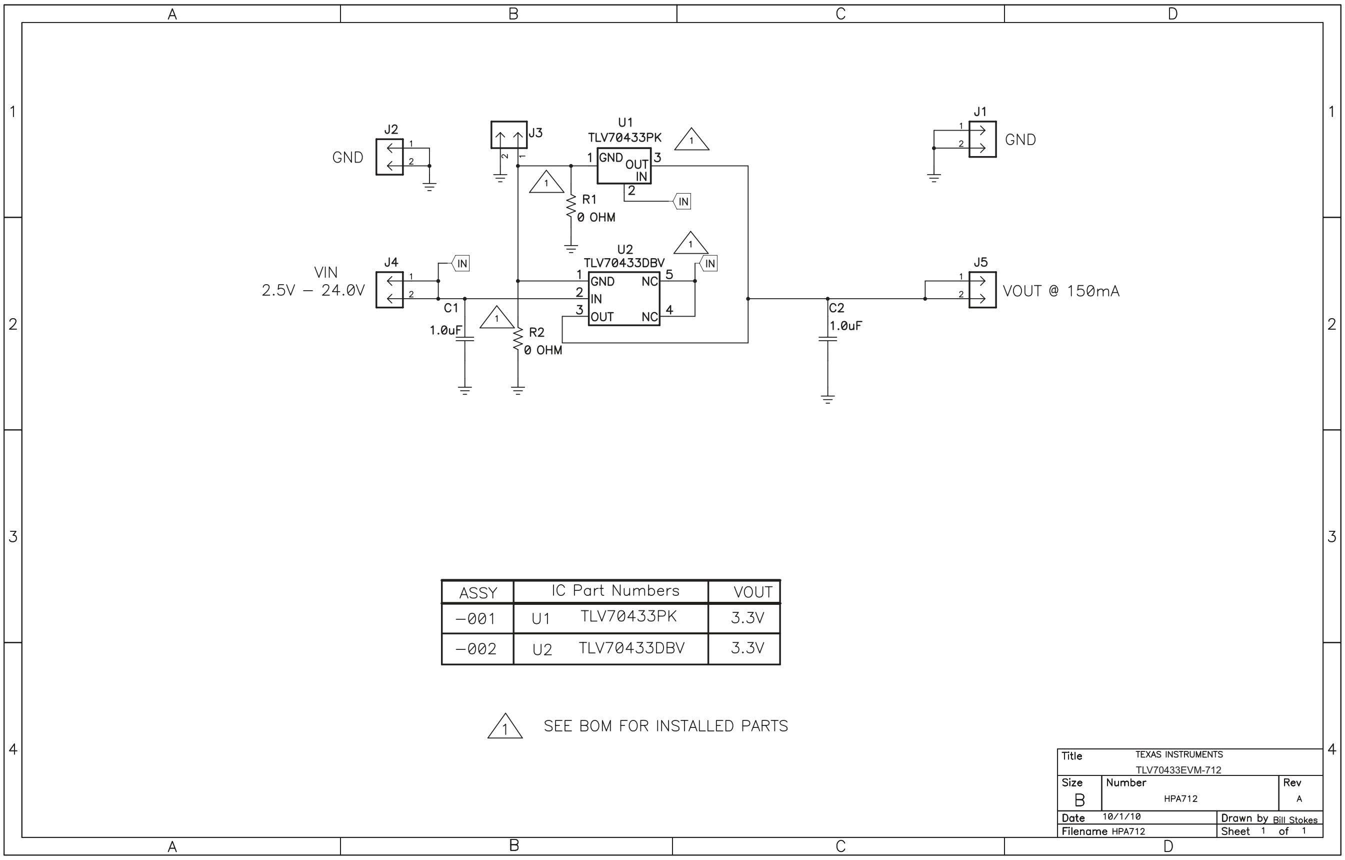


Figure 6. TLV70433DBVEVM-712, TLV70433PKEVM-712 Schematic

8 Bill of Materials

This section provides the TLV70433DBVEVM-712 and the TLV70433PKEVM-712 bill of materials.

Table 1. TLV70433DBVEVM-712, TLV70433PKEVM-712 Bill of Materials(1)(2)(3)(4)

Count		RefDes	Value	Description	Size	Part Number	MFR
-001	-002						
2	2	C1, C2	1.0 µF	Capacitor, ceramic	0805	STD	muRata
5	5	J1, J2, J3, J4, J5	PTC36SAAN	Header, 2-pin, 100-mil spacing	0.100 inch x 2	STD	Sullins
1	0	R1	0	Resistor, chip, 1/16W, 1%	0603	PTC36SAAN	Vishay
0	1	R2	0	Resistor, chip, 1/16W, 1%	0603	PTC36SAAN	Vishay
1	1	U1	TLV70433PK	IC, 24-V input, 150-mA, Ultraow IQ, LDO Regulator	SOT-89	TLV70433PK	TI
0	0	U2	TLV70433DBV	IC, 24-V input, 150-mA, Ultraow IQ, LDO Regulator	SOT-23	TLV70433DBV	TI
1	1	—	—	PCB, 1.260In x 1.845 In x 0.062 In		HPA712	Any
0	0	—	—	Shunt, 100-mil, black	0.100	929950-00	3M
1	1	—	—	Label (see (5))	1.25 x 0.25 inch	THT-13-457-10	Brady

(1) These assemblies are ESD sensitive. ESD precautions must be observed.
(2) These assemblies must be clean and free from flux and all contaminants. Use of *no-clean* flux is not acceptable.
(3) These assemblies must comply with IPC-A-610 Class 2 workmanship standards.
(4) Ref designators marked with an asterisk (*******) cannot be substituted. All other components can be substituted with equivalent components.
(5) Install label after final wash. Text should be 8-point font, and correspond to the text shown in Table 2.

Table 2. Assembly Marking

Assembly No	Text
HPA712A-001	TLV0433PKEVM-712
HPA712A-002	TLV0433DBVEVM-712

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EVM Warnings and Restrictions

It is important to operate this EVM within the input voltage range of –0.3 V to 24 V and the output voltage range of 1.2 V to 5 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than +100°C. The EVM is designed to operate properly with certain components above +100°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.