19-3360; Rev 0; 8/04

MAXIM

Multiphase, Fixed-Frequency Controller for AMD Hammer CPU Core Power Supplies

General Description

The MAX8707 is a multiphase (3-/4-phase), interleaved, fixed-frequency, step-down controller for AMD Hammer CPU core supplies. Interleaved multiphase operation reduces the input ripple current and output voltage ripple while easing component selection and layout placement. The MAX8707 includes active voltage positioning with adjustable gain and offset, reducing power dissipation and bulk output-capacitance requirements.

The MAX8707 is intended for two different notebook CPU core applications: stepping down the battery directly or stepping down the +5V system supply to create the core voltage. The single-stage conversion method allows these devices to directly step down high-voltage batteries for the highest possible efficiency. Alternatively, 2-stage conversion (stepping down the +5V system supply instead of the battery) at higher switching frequency provides the minimum possible physical size.

The MAX8707 features dedicated differential current-sense inputs for each phase and includes a fifth pair of current-sense inputs to provide an accurate voltage-positioning slope and average current-limit protection using a single current-sense resistor. The MAX8707 also has two dedicated inputs that provide differential remote voltage sensing.

The MAX8707 provides an analog input for setting the suspend voltage and a slew-rate controller for transitions between VID codes or the suspend voltage. The controllers reduce the transition slew rate during startup and shutdown, providing soft-start with minimal input surge current and damped soft-shutdown without negative output undershoot. The MAX8707 includes output fault protection—undervoltage, nonlatched overvoltage, and thermal overload—and an independent voltage-regulator power-OK (VROK) output.

The MAX8707 has a selectable switching frequency, allowing 200kHz, 300kHz, or 600kHz per-phase operation. The MAX8707 is available in the low-profile, 40-pin, 6mm x 6mm thin QFN package. Refer to the MAX8702/MAX8703 for compatible drivers.

Features

- ♦ **3-/4-Phase Interleaved Fixed-Frequency Controller**
- ♦ **±0.75% V_{OUT} Accuracy Over Line, Load, and Temperature**
- ♦ **5-Bit On-Board Digital-to-Analog Converter (DAC)—0.80V to 1.55V**
- ♦ **Adjustable Suspend Voltage Input**
- ♦ **Active Voltage Positioning with Adjustable Gain and Offset**
- ♦ **Accurate Lossless Current Balance**
- ♦ **Accurate Droop and Current Limit**
- ♦ **Remote Output and Ground Sense**
- ♦ **Output Slew-Rate Control**
- ♦ **Power-Good Window Comparator**
- ♦ **Selectable 200kHz/300kHz/600kHz Switching Frequency**
- ♦ **Output Overvoltage and Undervoltage Protection**
- ♦ **Thermal Fault Protection**
- ♦ **2V ±0.7% Reference Output**
- ♦ **Soft-Startup and Shutdown**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX8707ETL	-40°C to +85°C	40 Thin QFN 6mm x 6mm

Applications

AMD Hammer Desknote Computers

Multiphase CPU Core Supplies

Voltage-Positioned Step-Down Converters

Notebook/Desktop Computers

Servers

Pin Configuration appears at end of data sheet.

Multiphase, Fixed-Frequency Controller for AMD Hammer CPU Core Power Supplies

ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND .....-0.3V to +6V
D0–D4 to GND.....-0.3V to +6V
SKIP, SUS, VROK, ILIM(AVE) to GND.....-0.3V to +6V
SUSV, OFS, OSC to GND.....-0.3V to +6V
CSP_, CSN_, CRSP, CRSN to GND .....-0.3V to +6V
VPS, FBS, CCV, REF to GND .....-0.3V to (V_{CC} + 0.3V)
ILIM(PK), TRC, TIME to GND .....-0.3V to (V_{CC} + 0.3V)
PWM_, $\overline{DRSKP}$ to PGND .....-0.3V to (V_{CC} + 0.3V)
PGND, GNDS to GND .....-0.3V to +0.3V

$\overline{SHDN}$ to GND (Note 1).....-0.3V to +14V
REF Short-Circuit Duration .....Continuous
Continuous Power Dissipation (T_A = +70°C)
40-Pin 6mm x 6mm Thin QFN
(derate 26.3mW/°C above +70°C).....2.105W
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 1: $\overline{SHDN}$ can be forced to 12V for debugging prototype boards using the no-fault test mode, which disables fault protection.

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1. V_{CC} = $V_{\overline{SHDN}}$ = 5V, OSC = REF, V_{VPS} = V_{FBS} = V_{CRSN} = V_{CRSP} = $V_{CSP\_}$ = 1.20V, V_{SUSV} = 0.8V, OFS = SUS = GNDS = PGND = SKIP = GND, D0–D4 set for 1.20V (D0–D4 = 01110). **T_A = 0°C to +85°C**, unless otherwise specified. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
PWM CONTROLLER							
Input Voltage Range	V_{CC}			4.5		5.5	V
DC Output Voltage Accuracy	V_{OUT}	Includes load-regulation error (VPS = FBS)	DAC codes from 1.10V to 1.55V	-0.75		+0.75	%
			DAC codes from 0.80V to 1.075V	-2.0		+2.0	
			SUS = V_{CC}	-20		+20	mV
SUSV Input Range	V_{SUSV}			0.4		2.0	V
SUSV Input-Bias Current	I_{SUSV}	V_{SUSV} = 0.4V to 2V		-0.1		+0.1	µA
OFS Input Range	V_{OFS}	Negative offsets		0		0.8	V
		Positive offsets		1.2		2.0	
OFS GAIN	A_{OFS}	ΔV_{OUT} / ΔV_{OFS}, ΔV_{OFS} = V_{OFS}, V_{OFS} = 0 to 0.8V		-0.131	-0.125	-0.118	V/V
		ΔV_{OUT} / ΔV_{OFS}, ΔV_{OFS} = V_{OFS}-V_{REF}, V_{OFS} = 1.2V to 2V		-0.131	-0.125	-0.118	
OFS Input-Bias Current	I_{OFS}	V_{OFS} = 0 to 2V		-0.1		+0.1	µA
GNDS Input Range	V_{GNDS}			-200		+200	mV
GNDS Gain	A_{GNDS}	ΔV_{OUT} / ΔV_{GNDS}, -200mV ≤ V_{GNDS} ≤ +200mV		0.95	1.00	1.05	V/V
GNDS Input-Bias Current	I_{GNDS}			-2		+2	µA
FBS Input-Bias Current	I_{FBS}	CRSP = CRSN, CSP_ = CSN_		-10		+10	µA
Switching Frequency Accuracy (Per Phase)	f_{SW}	OSC = GND		180	200	220	kHz
		OSC = REF		270	300	330	
		OSC = V_{CC}		540	600	660	

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1. V_{CC} = $V_{\overline{SHDN}}$ = 5V, OSC = REF, V_{VPS} = V_{FBS} = V_{CRSN} = V_{CRSP} = $V_{CSP\_}$ = 1.20V, V_{SUSV} = 0.8V, OFS = SUS = GNDS = PGND = SKIP = GND, D0–D4 set for 1.20V (D0–D4 = 01110). **T_A = 0°C to +85°C**, unless otherwise specified. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
TIME Slew-Rate Accuracy		R_{TIME} = 143kΩ (6.25mV/µs)		-10		+10	%
		R_{TIME} = 47kΩ (19mV/µs) to 392kΩ (2.28mV/µs)		-15		+15	
		Startup and shutdown, R_{TIME} = 47kΩ (4.75mV/µs) to 392kΩ (0.57mV/µs)		-20		+20	
BIAS AND REFERENCE							
Quiescent Supply Current (V_{CC})	I_{CC}	Measured at V_{CC}, VPS and FBS forced above the regulation points			7	12	mA
Shutdown Supply Current (V_{CC})	$I_{CC(SHDN)}$	Measured at V_{CC}, $\overline{SHDN}$ = GND			0.05	10	µA
Reference Voltage	V_{REF}	V_{CC} = 4.5V to 5.5V, I_{REF} = 0		1.986	2.000	2.014	V
Reference Load Regulation	ΔV_{REF}	I_{REF} = 0 to 500µA		-2	-0.2		mV
		I_{REF} = -100µA to 0			0.21	6.2	
FAULT PROTECTION							
Output Overvoltage-Protection Threshold	V_{OVP}	Measured at VPS with respect to unloaded output voltage, rising edge, 8mV hysteresis	PWM (SKIP = GND) or SKIP mode when $V_{OUT} \le V_{TRIP}$	150	200	250	mV
			SKIP = V_{CC} and $V_{OUT} > V_{TRIP}$	1.70	1.75	1.80	V
		Minimum OVP level			1.1		
Output Overvoltage Propagation Delay	t_{OVP}	VPS forced 25mV above trip threshold			10		µs
Output Undervoltage-Protection Threshold	V_{UVP}	Measured at VPS with respect to 70% of the unloaded nominal output voltage		-30		+30	mV
Output Undervoltage Propagation Delay	t_{UVP}	VPS forced 25mV below trip threshold			10		µs
VROK Transition Blanking Time	t_{BLANK}	Measured from the time when VPS reaches the target voltage, slew rate set by R_{TIME} (Note 2)			20		µs
VROK Threshold		Undervoltage measured at VPS with respect to 87.5% unloaded output voltage, falling edge, 15mV hysteresis		-30		+30	mV
		Overvoltage measured at VPS with respect to 112.5% of the unloaded output voltage, rising edge, 15mV hysteresis		-30		+30	
VROK Delay	t_{VROK}	VPS forced 25mV outside the VROK trip thresholds			10		µs
VROK Output Low Voltage		I_{SINK} = 3mA				0.4	V
VROK Leakage Current		High state, VROK forced to 5.5V				1	µA

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ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1. V_{CC} = $V_{\overline{SHDN}}$ = 5V, OSC = REF, V_{VPS} = V_{FBS} = V_{CRSN} = V_{CRSP} = $V_{CSP\_}$ = 1.20V, V_{SUSV} = 0.8V, OFS = SUS = GNDS = PGND = SKIP = GND, D0–D4 set for 1.20V (D0–D4 = 01110). **T_A = 0°C to +85°C**, unless otherwise specified. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC} Undervoltage-Lockout Threshold	$V_{UVLO(VCC)}$	Rising edge, hysteresis = 20mV, PWM_ disabled below this level	4.10	4.25	4.45	V
Thermal-Shutdown Threshold	T_{SHDN}	Rising edge hysteresis = 15°C		+160		°C
DROOP AND TRANSIENT RESPONSE						
DC Droop Amplifier Offset			-1.5		+1.5	mV
DC Droop Amplifier Transconductance (CRS Sense Enabled)	$G_{m(VPS)}$	ΔI_{VPS} / (N x ΔV_{CRS}), V_{VPS} = V_{CRSN} = 1.2V, V_{CRSP} - V_{CRSN} = -60mV to +60mV, N = number of phases enabled	194	200	206	µS
DC Droop Amplifier Transconductance (CRS Sense Disabled)	$G_{m(VPS)}$	ΔI_{VPS} / ($\Sigma\Delta V_{CS}$), V_{CRSP} = V_{CC}, V_{VPS} = $V_{CSN\_}$ = 1.2V, $V_{CSP\_}$ – $V_{CSN\_}$ = -60mV to +60mV	194	200	206	µS
Transient-Droop Transresistance	R_{TRANS}	Current-sense gain (A_{CS} = 10 typ) divided by the voltage preamplifier transconductance ($G_{m(TRC)}$ = 2ms typ)	4.75	5.0	5.25	kΩ
Transient Detection Threshold		Measured at VPS with respect to steady-state VPS regulation voltage; falling edge, 5.5mV hysteresis (typ)	-30	-25	-20	mV
CURRENT LIMIT AND BALANCE						
Current-Sense Input Preamplifier Offsets		CSP_ - CSN_	-2.0		+2.0	mV
ILIM(AVE) Input Range (Adjustable Mode)	$V_{ILIM(AVE)}$		V_{REF} - 1.0		V_{REF} - 0.2	V
ILIM(AVE) Average Current-Limit Threshold Voltage (Positive, Default)	$V_{AVELIMIT}$	CRSP - CRSN; ILIM(AVE) = V_{CC}	22	25	28	mV
ILIM(AVE) Average Current-Limit Threshold Voltage (Positive, Adjustable)	$V_{AVELIMIT}$	CRSP - CRSN; $V_{ILIM(AVE)}$ = V_{REF} - 0.2V	7	10	13	mV
		CRSP - CRSN; $V_{ILIM(AVE)}$ = V_{REF} - 1.0V	46	50	54	
ILIM(AVE) Average Current-Limit Threshold Voltage (Negative)		CRSP - CRSN; ILIM(AVE) = V_{CC}	-30	-25	-20	mV
ILIM(AVE) Input Current	$I_{ILIM(AVE)}$		-0.1		+0.1	µA
ILIM(AVE) Current-Limit Default Switchover Threshold			3	V_{CC} - 1.0	V_{CC} - 0.4	V
ILIM(PK) Peak Current-Limit Threshold Voltage (Positive)	$V_{PKLIMIT}$	CSP_ - CSN_, $R_{ILIM(PK)}$ = R_{TRC} x 8V / $V_{LIM(PK)}$; $V_{PKLIMIT}$ = 30mV	24	30	36	mV
		CSP_ - CSN_, $R_{ILIM(PK)}$ = R_{TRC} x 8V / $V_{LIM(PK)}$; $V_{PKLIMIT}$ = 50mV	40	50	60	
ILIM(PK) Peak Current-Limit Threshold Voltage (Negative)		CSP_ - CSN_, $R_{ILIM(PK)}$ = R_{TRC} x 8V / $V_{PKLIMIT}$, $V_{PKLIMIT}$ = 50mV	-60	-50	-40	mV

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1. V_{CC} = $V_{\overline{SHDN}}$ = 5V, OSC = REF, V_{VPS} = V_{FBS} = V_{CRSN} = V_{CRSP} = $V_{CSP\_}$ = 1.20V, V_{SUSV} = 0.8V, OFS = SUS = GNDS = PGND = SKIP = GND, D0–D4 set for 1.20V (D0–D4 = 01110). **T_A = 0°C to +85°C**, unless otherwise specified. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ILIM(PK) Idle Current-Limit Threshold Voltage (Skip Mode)	V_{IDLE}	CSP_ - CSN_, V_{SKIP} ≥ 1.2V, $R_{ILIM(PK)}$ = R_{TRC} x 8V / $V_{PKLIMIT}$, $V_{PKLIMIT}$ = 50mV		2	5	8	mV
Current-Sense Input Current		CSP_, CRSP		-0.2		+0.2	µA
		CSN_, CRSN		-1.0		+1.0	
Current-Sense Common-Mode Input Range		CRSP, CRSN, CSP_, CSN_		0		2	V
Phase Disable Threshold		CSP4		3	V_{CC} - 1	V_{CC} - 0.4	V
CRS Sense Input Disable Threshold		CRSP		3	V_{CC} - 1	V_{CC} - 0.4	V
LOGIC AND I/O							
Logic Input High Voltage	V_{IH}	$\overline{SHDN}$, SUS		2.4			V
Logic Input Low Voltage	V_{IL}	$\overline{SHDN}$, SUS				0.8	V
$\overline{SHDN}$ No-Fault Threshold		To enable no-fault mode		11		13	V
D0–D4 Logic Input High Voltage				0.8			V
D0–D4 Logic Input Low Voltage						0.4	V
OSC 3-Level Input Logic Levels	V_{OSC}		High (V_{CC})	V_{CC} - 0.4			V
			Medium (REF)	1.8		2.2	
			Low (GND)			0.4	
SKIP Input Logic Levels	V_{SKIP}		High	1.2			V
			Low (GND)			0.8	
Logic Input Current		$\overline{SHDN}$, SKIP, SUS, OSC, D0–D4 = 0 to 5V		-1		+1	µA
Logic Output High Voltage	V_{OH}	PWM_, $\overline{DRSKP}$; I_{SOURCE} = 3mA		V_{CC} - 0.4			V
Logic Output Low Voltage	V_{OL}	PWM_, $\overline{DRSKP}$; I_{SINK} = 3mA				0.4	V

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ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1. V_{CC} = $V_{\overline{SHDN}}$ = 5V, OSC = REF, V_{VPS} = V_{FBS} = V_{CRSN} = V_{CRSP} = $V_{CSP\_}$ = 1.20V, V_{SUSV} = 0.8V, OFS = SUS = GNDS = PGND = SKIP = GND, D0–D4 set for 1.20V (D0–D4 = 01110). **T_A = -40°C to +85°C**, unless otherwise specified.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	MAX	UNITS
PWM CONTROLLER						
Input Voltage Range	V_{CC}			4.5	5.5	V
DC Output Voltage Accuracy	V_{OUT}	Includes load-regulation error (VPS = FBS)	DAC codes from 1.10V to 1.55V	-1.0	+1.0	%
			DAC codes from 0.80V to 1.075V	-3.0	+3.0	
			SUS = V_{CC}	-25	+25	mV
SUSV Input Range	V_{SUSV}			0.4	2.0	V
OFS Input Range	V_{OFS}	Negative offsets		0	0.8	V
		Positive offsets		1.2	2.0	
OFS GAIN	A_{OFS}	ΔV_{OUT} / ΔV_{OFS}; ΔV_{OFS} = V_{OFS}, V_{OFS} = 0 to 0.8V		-0.131	-0.118	V/V
		ΔV_{OUT} / ΔV_{OFS}; ΔV_{OFS} = V_{OFS} - V_{REF}, V_{OFS} = 1.2V to 2V		-0.131	-0.118	
GNDS Input Range	V_{GNDS}			-200	+200	mV
GNDS Gain	A_{GNDS}	ΔV_{OUT} / ΔV_{GNDS}, -200mV ≤ V_{GNDS} ≤ +200mV		0.95	1.05	V/V
Switching Frequency Accuracy (Per Phase)	f_{SW}	OSC = GND		180	220	kHz
		OSC = REF		270	330	
		OSC = V_{CC}		540	660	
TIME Slew-Rate Accuracy		R_{TIME} = 143kΩ (6.25mV/µs)		-10	+10	%
		R_{TIME} = 47kΩ (19mV/µs) to 392kΩ (2.28mV/µs)		-15	+15	
		Startup and shutdown, R_{TIME} = 47kΩ (4.75mV/µs) to 392kΩ (0.57mV/µs)		-20	+20	
BIAS AND REFERENCE						
Quiescent Supply Current (V_{CC})	I_{CC}	Measured at V_{CC}, VPS and FBS forced above the regulation points			12	mA
Shutdown Supply Current (V_{CC})	$I_{CC(SHDN)}$	Measured at V_{CC}, $\overline{SHDN}$ = GND			10	µA
Reference Voltage	V_{REF}	V_{CC} = 4.5V to 5.5V, I_{REF} = 0		1.98	2.02	V
Reference Load Regulation	ΔV_{REF}	I_{REF} = 0 to 500µA		-2		mV
		I_{REF} = -100µA to 0			6.2	mV
FAULT PROTECTION						
Output Overvoltage-Protection Threshold	V_{OVP}	Measured at VPS with respect to unloaded output voltage, rising edge, 8mV hysteresis	PWM (SKIP = GND) or SKIP mode when V_{OUT} ≤ V_{TRIP}	150	250	mV
			SKIP = V_{CC} and V_{OUT} > V_{TRIP}	1.70	1.80	V

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1. V_{CC} = $V_{\overline{SHDN}}$ = 5V, OSC = REF, V_{VPS} = V_{FBS} = V_{CRSN} = V_{CRSP} = $V_{CSP\_}$ = 1.20V, V_{SUSV} = 0.8V, OFS = SUS = GNDS = PGND = SKIP = GND, D0–D4 set for 1.20V (D0–D4 = 01110). **T_A = -40°C to +85°C**, unless otherwise specified.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Output Undervoltage-Protection Threshold	V_{UVP}	Measured at VPS with respect to 70% of the unloaded nominal output voltage	-40	+40	mV
VROK Threshold		Undervoltage, measured at VPS with respect to 87.5% of the unloaded output voltage, falling edge, 15mV hysteresis	-40	+40	mV
		Overvoltage, measured at VPS with respect to 112.5% of the unloaded output voltage, rising edge, 15mV hysteresis	-40	+40	
VROK Output Low Voltage		I_{SINK} = 3mA		0.4	V
V_{CC} Undervoltage-Lockout Threshold	$V_{UVLO(VCC)}$	Rising edge, hysteresis = 20mV, PWM_ disabled below this level	4.10	4.45	V
DROOP AND TRANSIENT RESPONSE					
DC Droop Amplifier Offset			-2	+2	mV
DC Droop Amplifier Transconductance (CRS Sense Enabled)	$G_{m(VPS)}$	ΔI_{VPS} / (N x ΔV_{CRS}); V_{VPS} = V_{CRSN} = 1.2V, V_{CRSP} - V_{CRSN} = -60mV to +60mV, N = number of phases enabled	190	210	µS
DC Droop Amplifier Transconductance (CRS Sense Disabled)	$G_{m(VPS)}$	ΔI_{VPS} / ($\Sigma\Delta V_{CS}$), V_{CRSP} = V_{CC}, V_{VPS} = $V_{CSN\_}$ = 1.2V, $V_{CSP\_}$ - $V_{CSN\_}$ = -60mV to +60mV	190	210	µS
Transient-Droop Transresistance	R_{TRANS}	Current-sense gain (A_{CS} = 10 typ) divided by the voltage preamplifier transconductance ($G_{m(TRC)}$ = 2mS typ)	4.50	5.25	kΩ
CURRENT LIMIT AND BALANCE					
Current-Sense Input Preamplifier Offsets		CSP_ - CSN_	-2.5	+2.5	mV
ILIM(AVE) Input Range (Adjustable Mode)	$V_{ILIM(AVE)}$		V_{REF} - 1.0	V_{REF} - 0.2	V
ILIM(AVE) Average Current-Limit Threshold Voltage (Positive, Default)	$V_{AVELIMIT}$	CRSP - CRSN; ILIM(AVE) = V_{CC}	20	30	mV
ILIM(AVE) Average Current-Limit Threshold Voltage (Positive, Adjustable)	$V_{AVELIMIT}$	CRSP - CRSN; $V_{ILIM(AVE)}$ = V_{REF} - 0.2V	5	15	mV
		CRSP - CRSN; $V_{ILIM(AVE)}$ = V_{REF} - 1.0V	44	56	
ILIM(AVE) Average Current-Limit Threshold Voltage (Negative)		CRSP - CRSN; ILIM(AVE) = V_{CC}	-31	-19	mV
ILIM(AVE) Current-Limit Default Switchover Threshold			3	V_{CC} - 0.4	V

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ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1. V_{CC} = $V_{\overline{SHDN}}$ = 5V, OSC = REF, V_{VPS} = V_{FBS} = V_{CRSN} = V_{CRSP} = $V_{CSP\_}$ = 1.20V, V_{SUSV} = 0.8V, OFS = SUS = GNDS = PGND = SKIP = GND, D0–D4 set for 1.20V (D0–D4 = 01110). **T_A = -40°C to +85°C**, unless otherwise specified.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	MAX	UNITS
ILIM(PK) Peak Current-Limit Threshold Voltage (Positive)	$V_{PKLIMIT}$	CSP_ - CSN_, $R_{ILIM(PK)}$ = R_{TRC} x 8V / $V_{LIM(PK)}$	$V_{PKLIMIT}$ = 30mV	24	36	mV
			V_{PKLIMT} = 50mV	40	60	
ILIM(PK) Peak Current-Limit Threshold Voltage (Negative)		CSP_ - CSN_, $R_{ILIM(PK)}$ = R_{TRC} x 8V / $V_{PKLIMIT}$, $V_{PKLIMIT}$ = 50mV		-60	-40	mV
ILIM(PK) Idle Current-Limit Threshold Voltage (Skip Mode)	V_{IDLE}	CSP_ - CSN_, V_{SKIP} ≥ 1.2V, $R_{ILIM(PK)}$ = R_{TRC} x 8V / $V_{PKLIMIT}$, $V_{PKLIMIT}$ = 50mV		2	8	mV
Current-Sense Input Current		CSP_, CRSP		-0.2	+0.2	µA
		CSN_, CRSN		-1.0	+1.0	
Current-Sense Common-Mode Input Range		CRSP, CRSN, CSP_, CSN_		0	2	V
Phase Disable Threshold		CSP4		3	V_{CC} - 0.4	V
CRS Sense Input Disable Threshold		CRSP		3	V_{CC} - 0.4	V
LOGIC AND I/O						
Logic Input High Voltage	V_{IH}	$\overline{SHDN}$, SUS		2.4		V
Logic Input Low Voltage	V_{IL}	$\overline{SHDN}$, SUS			0.8	V
D0–D4 Logic Input High Voltage				0.8		V
D0–D4 Logic Input Low Voltage					0.4	V
OSC 3-Level Input Logic Levels	V_{OSC}	High (V_{CC})		V_{CC} - 0.4		V
		Medium (REF)		1.8	2.2	
		Low (GND)			0.4	
SKIP Input Logic Levels	V_{SKIP}	High		1.2		V
		Low (GND)			0.8	
Logic Output High Voltage	V_{OH}	PWM_, $\overline{DRSKP}$; I_{SOURCE} = 3mA		V_{CC} - 0.4		V

Note 2: VROK is blanked during the transitions, when the internal target is being slewed. See the *Output-Voltage Transition Timing* section. VROK is reenabled in t_{BLANK} (20µs) after the transition is completed.

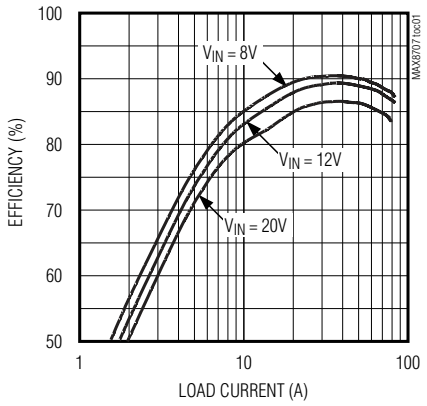
Note 3: Specifications to T_A = -40°C are guaranteed by design and are not production tested.

Multiphase, Fixed-Frequency Controller for AMD Hammer CPU Core Power Supplies

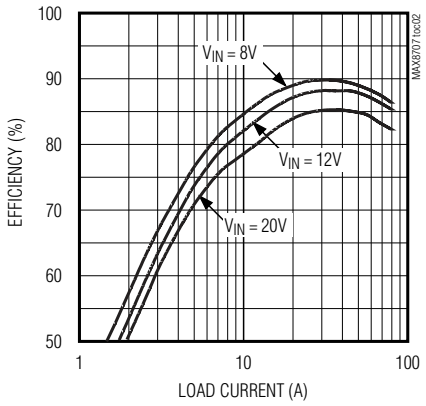
Typical Operating Characteristics

(Circuit of Figure 1. V_{IN} = 12V, V_{CC} = 5V, SUS = SKIP = GND, $\overline{SHDN}$ = V_{CC}, V_{SUSV} = 0.80V, T_A = +25°C, unless otherwise specified.)

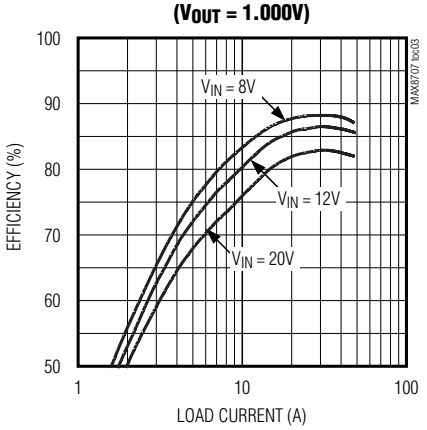
EFFICIENCY vs. LOAD CURRENT (V_{OUT} = 1.525V)



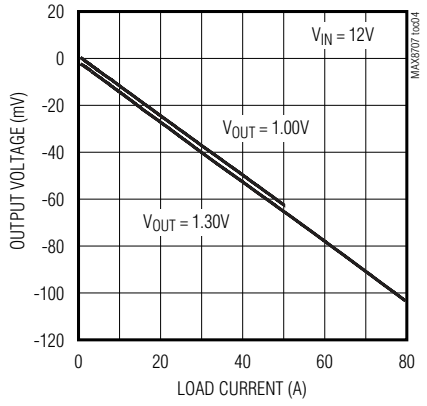
EFFICIENCY vs. LOAD CURRENT (V_{OUT} = 1.300V)



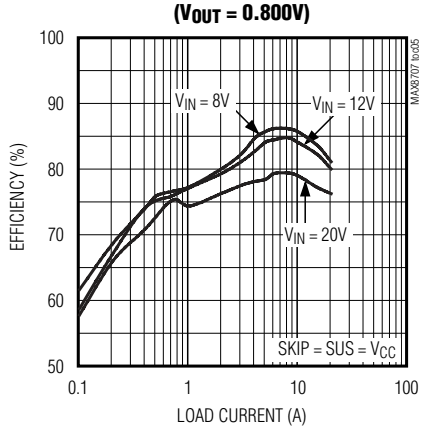
EFFICIENCY vs. LOAD CURRENT (V_{OUT} = 1.000V)



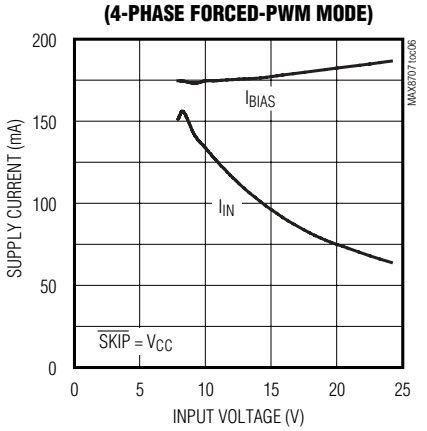
OUTPUT VOLTAGE DEVIATION vs. LOAD CURRENT



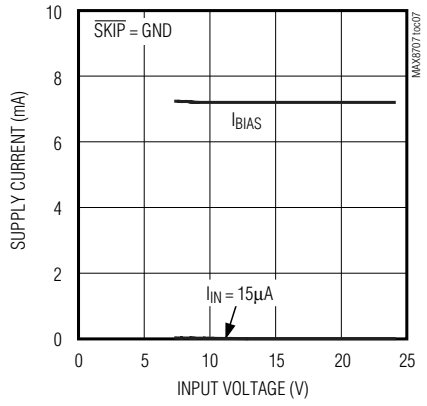
SINGLE-PHASE EFFICIENCY vs. LOAD CURRENT (V_{OUT} = 0.800V)



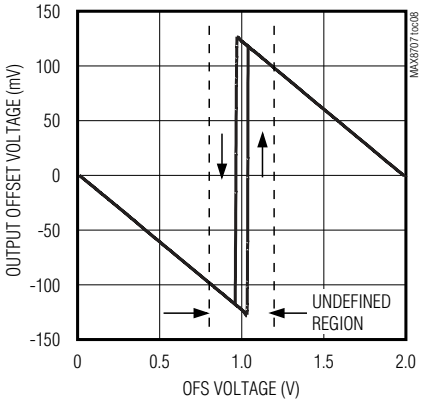
NO-LOAD SUPPLY CURRENT vs. INPUT VOLTAGE (4-PHASE FORCED-PWM MODE)



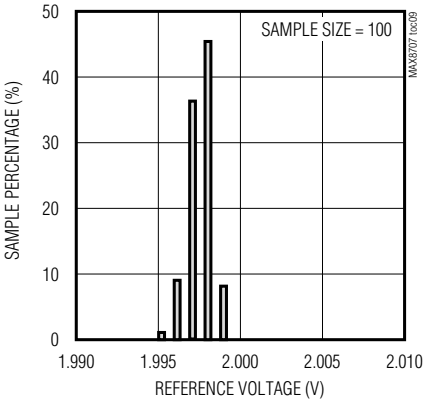
NO-LOAD SUPPLY CURRENT vs. INPUT VOLTAGE (1-PHASE PULSE SKIPPING)



OUTPUT OFFSET VOLTAGE vs. OFS VOLTAGE



REFERENCE VOLTAGE DISTRIBUTION

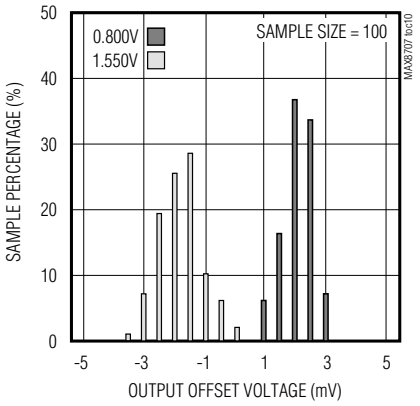


Multiphase, Fixed-Frequency Controller for AMD Hammer CPU Core Power Supplies

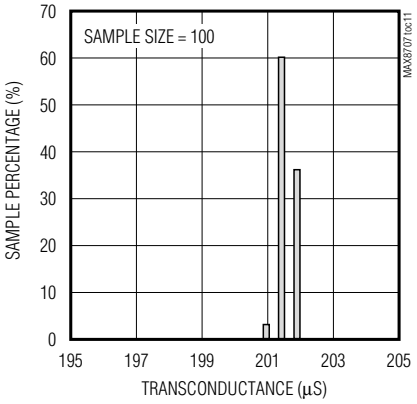
Typical Operating Characteristics

(Circuit of Figure 1. V_{IN} = 12V, V_{CC} = 5V, SUS = SKIP = GND, $\overline{SHDN}$ = V_{CC}, V_{SUSV} = 0.80V, T_A = +25°C, unless otherwise specified.)

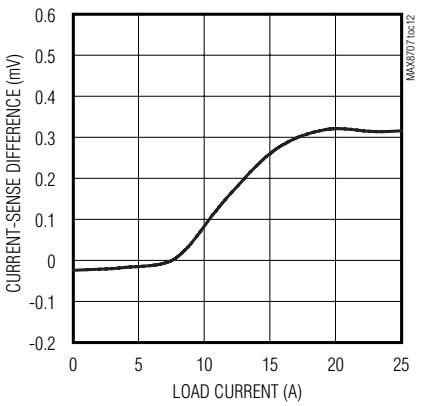
OUTPUT OFFSET VOLTAGE DISTRIBUTION



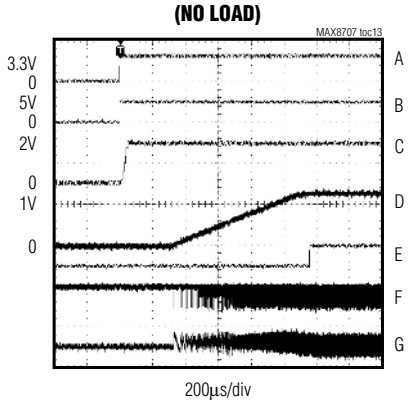
VPS TRANSCONDUCTANCE DISTRIBUTION



CURRENT-SENSE VOLTAGE DIFFERENCE vs. LOAD CURRENT

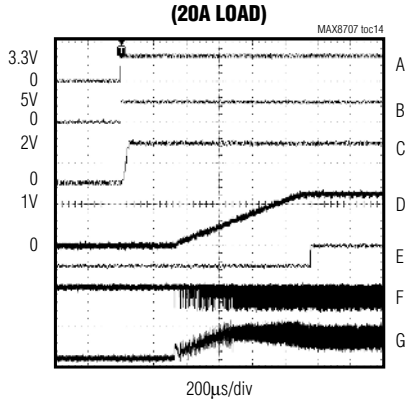


STARTUP WAVEFORM (NO LOAD)



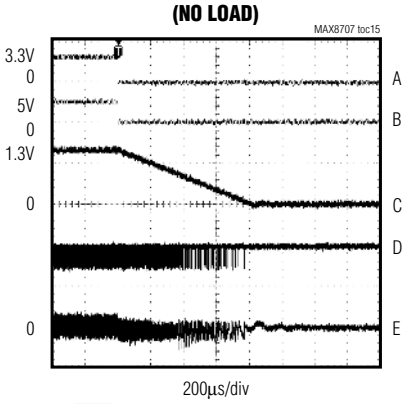
A. $\overline{SHDN}$, 5V/div
B. $\overline{DRSKP}$, 10V/div
C. REF, 2V/div
D. OUT, 1V/div
E. VROK, 10V/div
F. DL1, 10V/div
G. INDUCTOR CURRENT (I_{L1}), 10A/div

STARTUP WAVEFORM (20A LOAD)



A. $\overline{SHDN}$, 5V/div
B. $\overline{DRSKP}$, 10V/div
C. REF, 2V/div
D. OUT, 1V/div
E. VROK, 10V/div
F. DL1, 10V/div
G. INDUCTOR CURRENT (I_{L1}), 10A/div

SHUTDOWN WAVEFORM (NO LOAD)



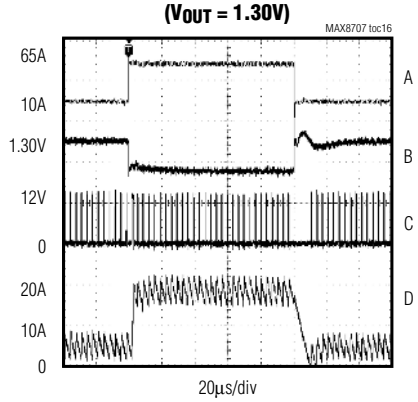
A. $\overline{SHDN}$, 5V/div
B VROK, 10V/div
C. OUT, 1V/div
D. DL1, 10V/div
E. INDUCTOR CURRENT (I_{L1}), 10A/div

Multiphase, Fixed-Frequency Controller for AMD Hammer CPU Core Power Supplies

Typical Operating Characteristics (continued)

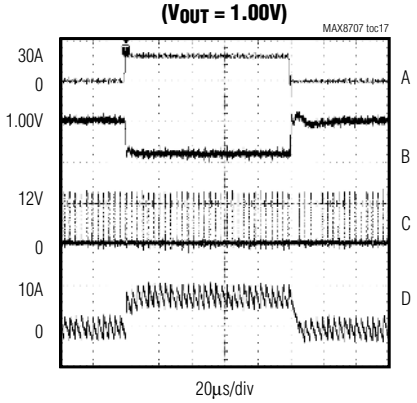
(Circuit of Figure 1. V_{IN} = 12V, V_{CC} = 5V, SUS = SKIP = GND, $\overline{SHDN}$ = V_{CC}, V_{SUSV} = 0.80V, T_A = +25°C, unless otherwise specified.)

LOAD TRANSIENT (V_{OUT} = 1.30V)



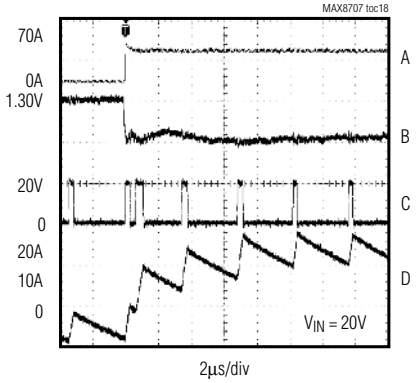
A. I_{OUT} = 10A TO 65A, 50A/div
B. V_{OUT}, 100mV/div
C. LX1, 10V/div
D. INDUCTOR CURRENT (I_{L1}), 10A/div

LOAD TRANSIENT (V_{OUT} = 1.00V)



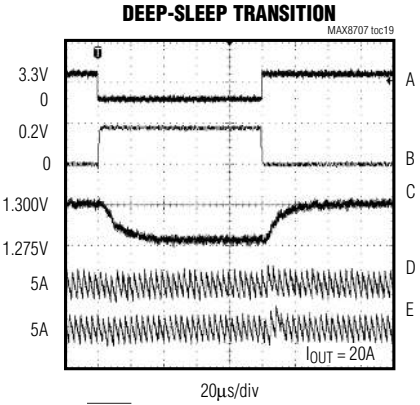
A. I_{OUT} = 0 TO 30A, 50A/div
B. V_{OUT}, 50mV/div
C. LX1, 10V/div
D. INDUCTOR CURRENT (I_{L1}), 10A/div

TRANSIENT PHASE REPEAT



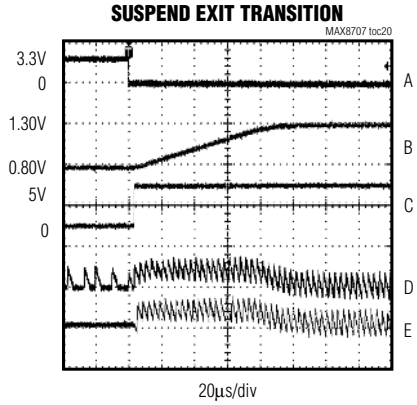
A. I_{OUT} = 0 TO 70A, 100A/div
B. V_{OUT}, 100mV/div
C. LX1, 10V/div
D. INDUCTOR CURRENT (I_{L1}), 10A/div

DEEP-SLEEP TRANSITION



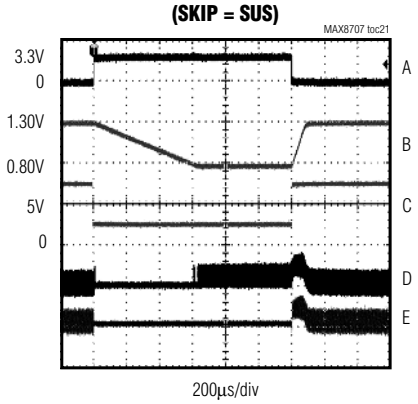
A. $\overline{DPSLP}$, 5V/div
B. OFS, 200mV/div
C. V_{OUT}, 25mV/div
D. INDUCTOR CURRENT (I_{L1}), 10A/div
E. INDUCTOR CURRENT (I_{L3}), 10A/div

SUSPEND EXIT TRANSITION



A. SUS, 5V/div
B. V_{OUT}, 500mV/div
C. $\overline{DRSKP}$, 5V/div
D. INDUCTOR CURRENT (I_{L1}), 10A/div
E. INDUCTOR CURRENT (I_{L3}), 10A/div

SUSPEND TRANSITION (SKIP = SUS)



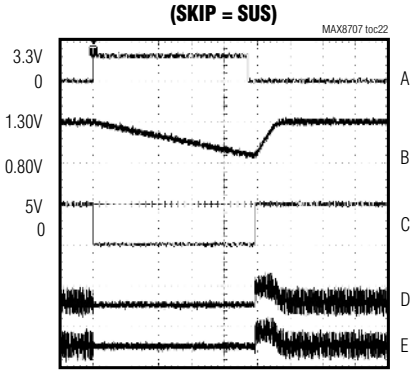
A. SUS, 5V/div
B. V_{OUT}, 500mV/div
C. $\overline{DRSKP}$, 5V/div
D. INDUCTOR CURRENT (I_{L1}), 10A/div
E. INDUCTOR CURRENT (I_{L3}), 10A/div

Multiphase, Fixed-Frequency Controller for AMD Hammer CPU Core Power Supplies

Typical Operating Characteristics (continued)

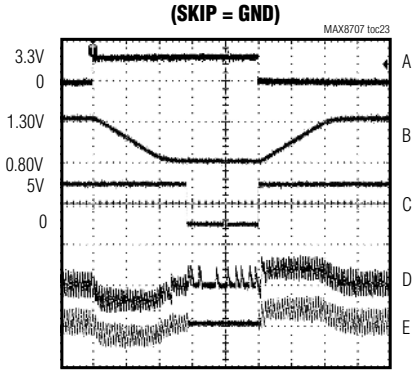
(Circuit of Figure 1. V_{IN} = 12V, V_{CC} = 5V, SUS = SKIP = GND, $\overline{SHDN}$ = V_{CC}, V_{SUSV} = 0.80V, T_A = +25°C, unless otherwise specified.)

SUSPEND TRANSITION (SKIP = SUS)



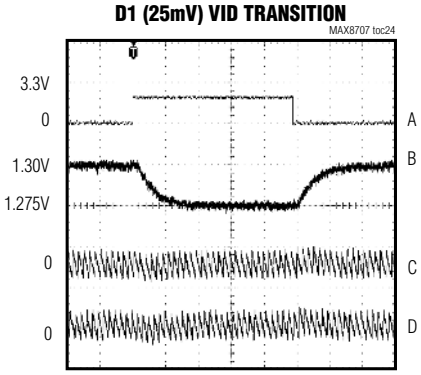
A. SUS, 5V/div
B. V_{OUT}, 500mV/div
C. $\overline{DRSKP}$, 5V/div
D. INDUCTOR CURRENT (I_{L1}), 10A/div
E. INDUCTOR CURRENT (I_{L3}), 10A/div

SUSPEND TRANSITION (SKIP = GND)



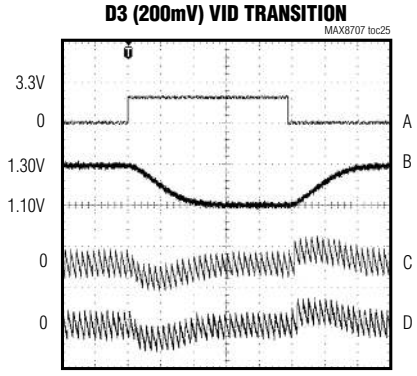
A. SUS, 5V/div
B. V_{OUT}, 500mV/div
C. $\overline{DRSKP}$, 5V/div
D. INDUCTOR CURRENT (I_{L1}), 10A/div
E. INDUCTOR CURRENT (I_{L3}), 10A/div

D1 (25mV) VID TRANSITION



A. D1, 5V/div
B. V_{OUT}, 25mV/div
C. INDUCTOR CURRENT (I_{L1}), 10A/div
D. INDUCTOR CURRENT (I_{L3}), 10A/div

D3 (200mV) VID TRANSITION



A. D3, 5V/div
B. V_{OUT}, 200mV/div
C. INDUCTOR CURRENT (I_{L1}), 10A/div
D. INDUCTOR CURRENT (I_{L3}), 10A/div

Pin Description

PIN	NAME	FUNCTION
1	D2	Low-Voltage VID DAC Code Input. The D0–D4 inputs do not have internal pullups. These 1.0V logic inputs are designed to interface directly with the CPU. In normal mode (Table 4, SUS = GND), the output voltage is set by the VID code indicated by the logic-level voltages on D0–D4. In suspend mode (SUS = high), the output voltage tracks the voltage at SUSV.
2	D3	Low-Voltage VID DAC Code Input
3	D4	Low-Voltage VID DAC Code Input (MSB)
4	N.C.	No Connect. **Leave open. Pin internally connected.**
5	SKIP	Pulse-Skipping Indicator Input. When pulse skipping, the controller blanks the VROK upper threshold. 3.3V or V_{CC} (high) = 1-phase pulse-skipping operation (phases 2, 3, and 4 disabled) GND = multiphase forced-PWM operation The controller automatically enters forced-PWM mode during startup, shutdown, and the no-CPU VID mode.
6	$\overline{SHDN}$	Shutdown Control Input. This input cannot withstand the battery voltage. Connect to V_{CC} for normal operation. Connect to ground to put the IC into its 50nA (typ) shutdown state. During the startup and shutdown transitions, the output voltage is ramped at 1/4th the output-voltage slew rate programmed by R_{TIME}. After completing soft-shutdown, the drivers are disabled—$\overline{DRSKP}$ and PWM_ are pulled low. Forcing $\overline{SHDN}$ to 11V~13V disables both overvoltage-protection and undervoltage-protection circuits, and clears the fault latch. Do not connect $\overline{SHDN}$ to >13V.
7	SUS	Suspend Control Input. When the controller detects a transition on SUS, the controller slews the output voltage to the new voltage level determined by SUSV (SUS = high) or D0–D4 (SUS = low). The controller blanks VROK during the transition and another 20µs after the new target voltage is reached. When SUS is high, the offset (OFS) is automatically disabled.
8	SUSV	Suspend-Mode Voltage Input. Connect to the output of a resistive voltage-divider from REF to GND to provide an analog voltage between 0.4V to 2V. The output voltage is set by the voltage at SUSV when SUS is high.
9	ILIM(AVE)	Average Current-Limit Threshold Adjustment. The controller uses the accurate CRSP-to-CRSN current-sense voltage to limit the average current per phase. When the average current-limit threshold is exceeded, the controller internally reduces the peak inductor current-limit threshold (ILIM(PK)) at 2% of $I_{PKLIMIT}$ per µs until the average current remains within the programmed limits. When the accurate current sensing is disabled (CRSP = V_{CC}), the average current-limit circuit is disabled and $I_{LIM(AVE)}$ should be connected to V_{CC}. The average current-limit threshold defaults to 25mV if ILIM(AVE) is connected to V_{CC}. In adjustable mode, the average current-limit threshold voltage is precisely 1/20th the voltage difference between ILIM(AVE) and the reference: (V_{REF} - $V_{ILIM(AVE)}$) / 20 for a range of 1.0V (V_{REF} - 1V) to 1.8V (V_{REF} - 0.2V). The logic threshold for switchover to the 25mV default value is approximately V_{CC} - 1V.
10	OFS	Adjustable Offset Voltage Input. For 0 < V_{OFS} < 0.8V, 1/8th the voltage at OFS is subtracted from the output. For 1.2V < V_{OFS} < 2.0V, 1/8th the difference between REF and OFS is added to the output. Voltages in the range of 0.8V < V_{OFS} < 1.2V are undefined. The controller disables the offset amplifier during suspend mode (SUS = high).

Multiphase, Fixed-Frequency Controller for AMD Hammer CPU Core Power Supplies

Pin Description (continued)

PIN	NAME	FUNCTION
11	OSC	Oscillator Select Input. OSC is a 3-level logic input for selecting the per-phase switching frequency. Connect to GND for 200kHz, connect to REF for 300kHz, or connect to V_{CC} for 600kHz per phase.
12	GNDS	Ground Remote-Sense Input. Connect GNDS directly to the CPU ground-sense pin. GNDS internally connects to an amplifier that adjusts the output voltage, compensating for voltage drops from the regulator ground to the load ground.
13	TIME	Slew-Rate Adjustment Pin. Connect a resistor from TIME to GND to set the internal slew rate. A 47kΩ to 392kΩ corresponds to slew rates of 19mV/µs to 2.28mV/µs, respectively, for all suspend voltage transitions. $$t_{TRAN(SUS)} = \frac{\lvert V_{NEW} - V_{OLD} \rvert}{dV_{TARGET}/dt}$$ where $dV_{TARGET} / dt = 6.25mV/\mu s \times 143k\Omega / R_{TIME}$ is the slew rate. For soft-start and shutdown, the controller automatically reduces the slew rate by 1/4th. For all dynamic VID transitions, the rate at which the VID inputs (D0–D4) are clocked sets the slew rate, as long as it is less than the dv/dt set by R_{TIME}.
14	ILIM(PK)	Peak Inductor Current-Limit Threshold Adjustment (Cycle-by-Cycle Current Limit). If the voltage across the current-sense inputs (CSP to CSN) exceeds the peak current-limit threshold, the controller immediately terminates the respective phase's on-time. Connect a resistor $R_{ILIM(PK)}$ from ILIM(PK) to GND to set the cycle-by-cycle peak current-limit threshold: $$R_{ILIM(PK)} = \frac{8V \times R_{TRC}}{I_{PKLIMIT} R_{CS}}$$ where R_{CS} is the resistance value of the current-sense element (inductors' DCR or current-sense resistor), R_{TRC} is the resistance between TRC and REF, and $I_{PKLIMIT}$ is the desired peak current limit (per phase).
15	CCV	Voltage Integrator Capacitor Connection. Connect a 470pF x (4 / η_{PH}) or greater capacitor from CCV to analog ground (GND) to set the integration time constant.
16	TRC	Transient-Voltage Preamplifier Output. Connect a resistor (R_{TRC}) between TRC and REF to set the transient droop based on the voltage-positioning requirements. TRC does not affect the DC steady-state droop. Choose R_{TRC} based on the equation: $$R_{TRC} = A_{CS}\left(\frac{R_{TRANS}R_{CS}}{\eta_{PH}R_{DROOP(AC)}}\right)$$ as defined in the *Design Procedure* (page 33). If voltage positioning is not required, R_{TRC} is determined by the stability requirements. TRC is high impedance in shutdown.

Pin Description (continued)

PIN	NAME	FUNCTION
17	REF	2.0V Reference Output. Bypass to GND with a 0.22µF to 1µF (max) ceramic capacitor. The reference can source 500µA for external loads. Loading REF degrades output-voltage accuracy according to the REF load-regulation error.
18	VROK	Open-Drain Power-Good Output. After power-up, VROK remains high impedance as long as the output voltage remains in regulation. The controller blanks VROK (high impedance) whenever the slew-rate control is active (output-voltage transitions). VROK is forced low during startup and shutdown. In pulse-skipping mode (SKIP = high), the upper VROK threshold is disabled.
19	GND	Analog Ground. Connect the MAX8707's exposed pad to analog ground.
20	PGND	Power Ground. Ground connection for the driver control outputs (PWM_) and driver skip output ($\overline{DRSKP}$).
21	V_{CC}	Analog Supply-Voltage Input. Connect V_{CC} to the system supply voltage (4.5V to 5.5V) with a series 10Ω resistor. Bypass to analog GND with a 1µF or greater ceramic capacitor, as close to the IC as possible.
22	PWM1	PWM Driver Control Output for Phase 1. Logic low in shutdown.
23	PWM2	PWM Driver Control Output for Phase 2. Logic low in shutdown.
24	PWM3	PWM Driver Control Output for Phase 3. Logic low in shutdown.
25	PWM4	PWM Driver Control Output for Phase 4. Logic low when disabled (CSP4 = V_{CC}) and in shutdown.
26	$\overline{DRSKP}$	Driver Skip Control Output. Push/pull logic output that controls the operating mode of the skip-mode driver ICs. $\overline{DRSKP}$ swings from V_{CC} to PGND. When $\overline{DRSKP}$ is high, the driver ICs operate in forced-PWM mode. When $\overline{DRSKP}$ is low, the driver ICs enable their zero-crossing comparators and operate in pulse-skipping mode.
27	FBS	Remote Feedback Sense Input. Connect FBS to the CPU output sense point. To minimize output-voltage errors due to any resistance in series with the FBS input, the controller generates an FBS input bias current equal in magnitude and opposite in polarity to the VPS output current. FBS is high impedance in shutdown.
28	VPS	Voltage-Positioning Transconductance-Amplifier Output. Connect a resistor R_{VPS} between VPS and FBS to set the DC steady-state droop (load line) based on the required voltage-positioning slope (see the *Voltage-Positioning Amplifier* section). $R_{VPS} = R_{DROOP} / (R_{SENSE} \times G_{M(VPS)})$ where R_{DROOP} is the desired DC voltage-positioning slope, R_{SENSE} is the current-sense resistor, and $G_{M(VPS)}$ = 200µS. R_{SENSE} is the accurate sense resistor used to generate current-sense voltage (CRSP, CRSN). When CRSP is connected to V_{CC}, the input to the transconductance amplifier is the sum of the current-sense voltage (CSP_, CSN_) inputs. When the inductors' DC resistances (R_{DCR}) are used as the current-sense elements (for lossless sensing), R_{VPS} should include an NTC thermistor to minimize the temperature dependence of the voltage-positioning slope. To disable voltage positioning, short VPS to FBS. VPS is high impedance in shutdown.
29	CRSN	Negative Current-Sense Resistor Input. CRSN is the negative differential input used for accurate sensing of the phase 1 inductor current. Connect a current-sense resistor between CRSP and CRSN for accurate voltage positioning and current limit. Float CRSN when not used (CRSP pulled up to V_{CC}).

Multiphase, Fixed-Frequency Controller for AMD Hammer CPU Core Power Supplies

Pin Description (continued)

PIN	NAME	FUNCTION
30	CRSP	Positive Current-Sense Resistor Input. CRSP is the positive differential input used for accurate sensing of the phase 1 inductor current. Connect a current-sense resistor between CRSP and CRSN. If current-sense resistors are used on all phases (CSP_, CSN_), this additional current-sense (CRSP, CRSN) feature can be disabled by connecting CRSP to V_{CC} and floating CRSN.
31	CSP1	Positive Current-Sense Input for Phase 1. This input should be connected to the positive terminal of the current-sense resistor or of the DCR sensing filtering capacitor, depending on the current-sense method implemented.
32	CSN1	Negative Current-Sense Input for Phase 1
33	CSN2	Negative Current-Sense Input for Phase 2
34	CSP2	Positive Current-Sense Input for Phase 2. This input should be connected to the positive terminal of the current-sense resistor or of the DCR sensing filtering capacitor, depending on the current-sense method implemented.
35	CSP3	Positive Current-Sense Input for Phase 3. This input should be connected to the positive terminal of the current-sense resistor or of the DCR sensing filtering capacitor, depending on the current-sense method implemented.
36	CSN3	Negative Current-Sense Input for Phase 3
37	CSN4	Negative Current-Sense Input for Phase 4
38	CSP4	Positive Current-Sense Input for Phase 4. This input should be connected to the positive terminal of the current-sense resistor or of the DCR sensing filtering capacitor, depending on the current-sense method implemented. Connect CSP4 to V_{CC} for fixed 3-phase operation.
39	D0	Low-Voltage VID-DAC Code Inputs. The D0–D4 inputs do not have internal pullups. These 1.0V logic inputs are designed to interface directly with the CPU. In normal mode (Table 4, SUS = low), the output voltage is set by the D0–D4 VID-DAC inputs. In suspend mode (SUS = high), the output voltage tracks the voltage at SUSV.
40	D1	Low-Voltage VID-DAC Code Inputs

Detailed Description

+5V Bias Supply (Vcc)

The MAX8707 requires an external +5V bias supply in addition to the battery. Typically, this +5V bias supply is the notebook's 95%-efficient, +5V system supply. Keeping the bias supply external to the controller improves efficiency and eliminates the cost associated with the +5V linear regulator that would otherwise be needed to supply the PWM circuit and gate drivers. If stand-alone capability is needed, the +5V bias supply can be generated with an external linear regulator.

The +5V bias supply must provide V_{CC} (PWM controller) and V_{DRV} (FET gate-drive power), so the maximum current drawn is:

$$I_{BIAS} = I_{CC} + I_{DRIVE}$$

where I_{CC} is provided in the *Electrical Characteristics* table and I_{DRIVE} is the driver's supply current dominated by $f_{SW} \times Q_G$ (per phase) as defined in the driver's data sheet. If the +5V bias supply is powered up prior to the battery supply, the enable signal ($\overline{SHDN}$ going from low to high) must be delayed until the battery voltage is present to ensure startup.

Switching Frequency (OSC)

OSC is a 3-level logic input used to set the per-phase switching frequency. Connect OSC directly to GND, REF, or V_{CC} for 200kHz, 300kHz, and 600kHz operation, respectively. High-frequency (600kHz, OSC = V_{CC}) operation optimizes the application for the smallest component size, trading off efficiency due to higher switching losses. This may be acceptable in ultra-portable devices where the load currents are lower. Low-frequency (200kHz, OSC = GND) operation offers the best overall efficiency at the expense of component size and board space.

Interleaved Multiphase Operation

The MAX8707 interleaves all the active phases—resulting in out-of-phase operation that minimizes the input and output filtering requirements, reduces electromagnetic interference (EMI), and improves efficiency. The multiphase controller shares the current between multiple phases that operate 90° out-of-phase (4-phase operation) or 120° out-of-phase (3-phase operation). The high-side MOSFETs do not turn on simultaneously during normal operation. The instantaneous input current is effectively reduced by the number of active phases, resulting in reduced input voltage ripple, ESR power loss, and RMS ripple current (see the *Input-Capacitor Selection* section). Therefore, the controller achieves high performance while minimizing the component count—which reduces cost, saves board space, and lowers component power requirements—making the MAX8707 ideal for high-power, cost-sensitive applications.

Transient Phase Repeat

When a transient occurs, the response time of the controller depends on its ability to quickly respond to the output-voltage deviation and slew the inductor current to the new current level. Multiphase, fixed-frequency controllers typically respond only to the clock edge, resulting in a delayed response from the actual transient event. To eliminate this delay time, the MAX8707 includes transient phase repeat, which allows the controller to immediately respond when heavy load transients are detected. If the controller detects that the output voltage has dropped by 25mV, the transient detection comparator immediately retriggers the phase that completed its on-time last. The controller triggers the subsequent phases as normal—on the appropriate oscillator edges. This effectively triggers a phase a full cycle early, increasing the total inductor-current slew rate and providing an immediate transient response.

Feedback-Adjustment Amplifiers

Voltage-Positioning Amplifier (Steady-State Droop)

The multiphase controllers include a transconductance amplifier for adding gain to the voltage-positioning sense path. The current-sense inputs differentially sense the voltage across either a single current-sense resistor (CRS sensing enabled) or the inductor's DCR (CRS sensing disabled). The VPS amplifier's input is generated by sensing either a single phase (CRS sensing) and multiplying by the number of active phases, or by summing the current-sense (CS_) inputs of all active phases (CRSP = V_{CC}). The transconductance amplifier's output connects to the regulator's voltage-positioned feedback input (VPS), so the resistance between VPS and the output voltage-sense point (FBS) determines the voltage-positioning gain:

$$V_{OUT} = V_{TARGET} - R_{VPS} I_{VPS}$$

where the target voltage (V_{TARGET}) is defined in the *Nominal Output-Voltage Selection* section, and the transconductance amplifier's output current (I_{VPS}) is determined by the current-sense voltage and the number of active phases (η_{PH}):

$$I_{VPS} = \eta_{PH} (V_{CRSP} - V_{CRSN}) G_{M(VPS)}$$

when CRS sensing is enabled, or:

$$I_{VPS} = \Sigma (V_{CSP\_} - V_{CSN\_}) G_{M(VPS)}$$

when CRS sensing is disabled (CRSP = V_{CC}).

where $G_{M(VPS)}$ is typically 200µS as defined in the *Electrical Characteristics* table. To avoid output-voltage errors caused by the VPS current flowing through parasitic trace resistance or feedback fliter resistance, a second transconductance amplifier generates an equal and opposite current on the FBS input.

Disable voltage positioning by shorting VPS directly to FBS.

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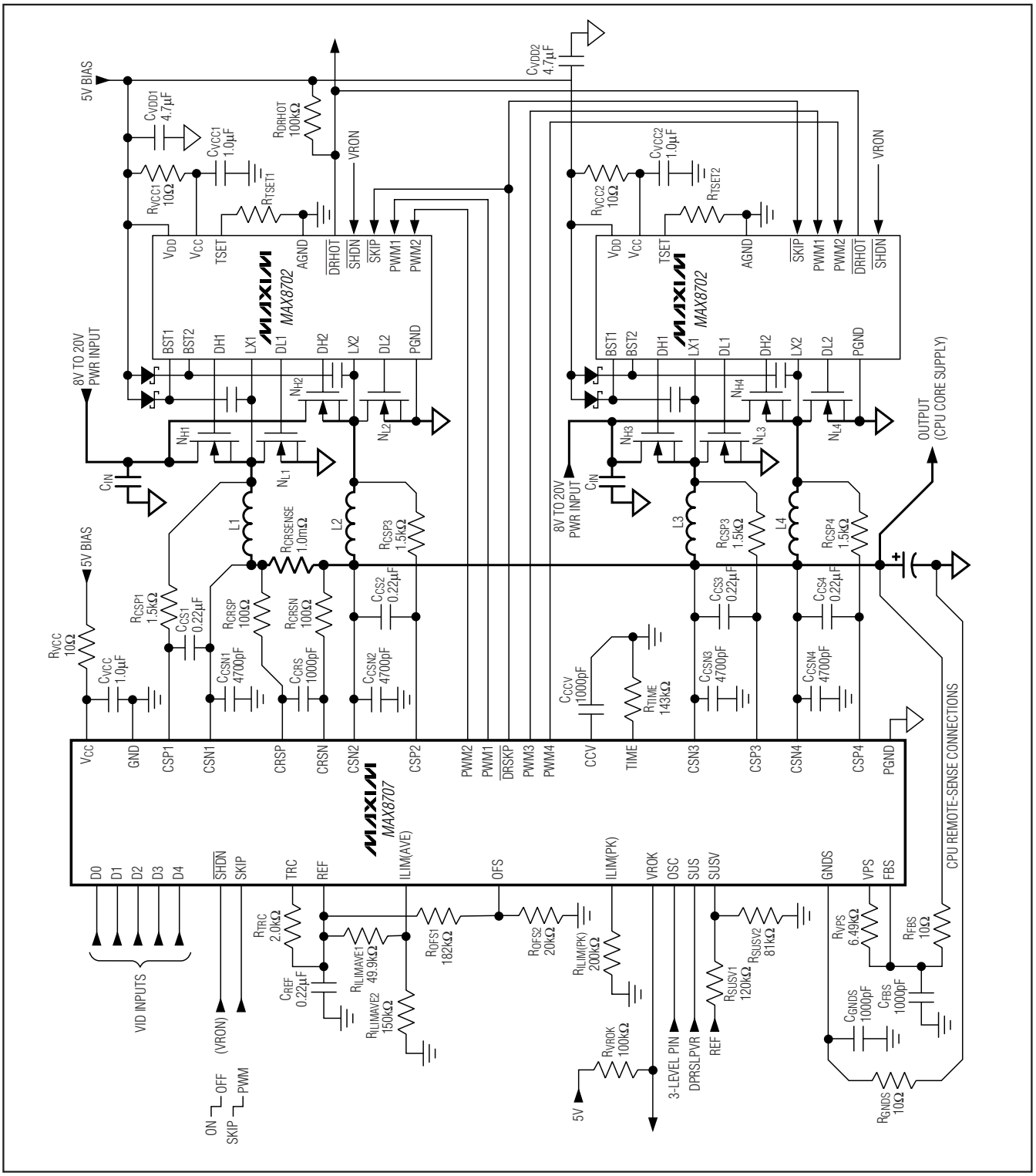

Figure 1. Standard MAX8707 AMD Hammer Application Circuit

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Transient-Droop Amplifier

The MAX8707 controller includes a transient-droop transconductance amplifier to handle the instantaneous load transients typical of CPU applications. The transient-droop amplifier sets the correct voltage-positioning slope during a load transient, complimenting the slower steady-state voltage-positioning amplifier. The current-sense inputs differentially sense the voltage across the CSP_ and CSN_ current-sense element (inductor's DCR or current-sense resistor). The transconductance amplifier's output connects to the regulator's transient-response input (TRC), so the resistance between TRC and the reference voltage (REF) determines the transient voltage-positioning gain as defined in the *Multiphase, Fixed-Frequency Design Procedure* section.

If voltage positioning is not required, R_{DROOP} is defined by the maximum output-voltage sag with the worst-case transient load (ΔV_{OUT} / ΔI_{OUT}) and is subject to stability requirements. TRC is high impedance in shutdown.

Differential Remote Sense

The multiphase controllers include differential, remote-sense inputs to eliminate the effects of voltage drops down the PC board traces and through the processor's power pins.

The MAX8707 GNDS amplifier adds an offset directly to the target voltage, adjusting the output voltage to counteract the voltage drop in the ground path. Connect the feedback sense (FBS), voltage-positioning resistor (R_{VPS}), and ground-sense (GNDS) inputs directly to the processor's core supply remote- sense outputs.

Integrator Amplifier

An integrator amplifier forces the DC average of the VPS voltage to equal the target voltage. This transconductance amplifier integrates the feedback voltage and provides a fine adjustment to the regulation voltage (Figure 2), allowing accurate DC output-voltage regulation regardless of the output ripple voltage. The integrator amplifier has the ability to shift the output voltage by ±100mV (typ). The differential input voltage range is at least ±60mV total, including DC offset and AC ripple. The integration time constant can be set easily with an external compensation capacitor at the CCV pin. Use a 470pF x (4 / η_{PH}) or greater ceramic capacitor.

The MAX8707 disables the integrator by connecting the amplifier inputs together at the beginning of all transitions done in pulse-skipping mode (SKIP = high). The integrator remains disabled until 20µs after the transition is completed (the internal target settles) and the output is in regulation (edge detected on the error comparator).

Table 1. Component Selection for Standard Multiphase Applications

DESIGNATION	MAX8707 AMD HAMMER COMPONENTS
	Circuit of Figure 1
Input Voltage Range	7V to 24V
VID Output Voltage (D4–D0)	1.50V (D4–D0 = 00010)
SUSV Suspend Voltage (SUS = High)	0.80V
Maximum Load Current	80A
Number of Phases (η_{TOTAL})	4 phases (1) MAX8705 + (2) MAX8702
Inductor (Per Phase)	0.56µH, 1.6mΩ Panasonic ETQP4LR56WFC
Switching Frequency (Per Phase)	300kHz (OSC = REF)
High-Side MOSFET (N_H, Per Phase)	Siliconix (1) Si7892DP
Low-Side MOSFET (N_L, Per Phase)	Siliconix (2) Si7356DP
Total Input Capacitance (C_{IN})	(8) 10µF, 25V TDK C3225X7R1E106M Taiyo Yuden TMK325BJ106MN
Total Output Capacitance (C_{OUT})	(6) 330µF, 2.5V, 9mΩ Sanyo 2R5TPE330M9
Current-Sense Resistor (R_{SENSE})	1.0mΩ Panasonic ERJM1WTJ1M0U

When voltage positioning is disabled (VPS = FBS), the transient droop must be less than the ±80mV minimum adjustment range of the integrator amplifier to guarantee proper DC output-voltage accuracy.

Offset Amplifier

The multiphase controllers include a fifth amplifier used to add small offsets to the voltage-positioned load line. The offset amplifier sums directly with the target voltage, making the offset gain independent of the DAC code. This amplifier has the ability to offset the output by ±100mV. The offset is adjusted using resistive voltage-dividers at the OFS input. For inputs from 0 to 0.8V, the offset amplifier adds a negative offset to the output that is equal to 1/8th the voltage appearing at the OFS input (V_{OFFSET} = -0.125 x V_{OFS}). For inputs from 1.2V

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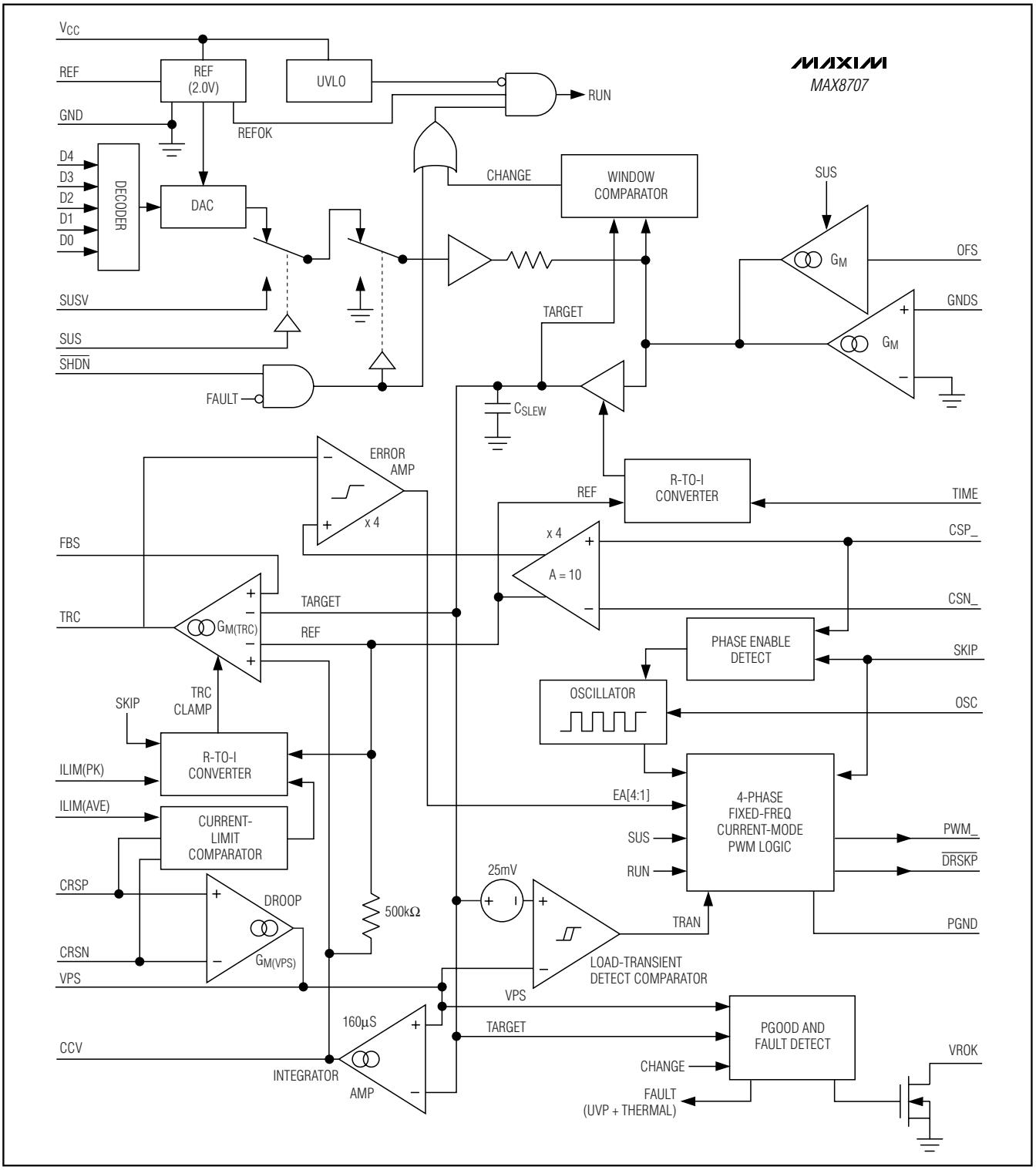

Figure 2. MAX8707 Functional Diagram

Table 2. Component Suppliers

MANUFACTURER	WEBSITE
BI Technologies	www.bitechnologies.com
Central Semiconductor	www.centralsemi.com
Coilcraft	www.coilcraft.com
Coiltronics	www.coiltronics.com
Fairchild Semiconductor	www.fairchildsemi.com
International Rectifier	www.irf.com
Kemet	www.kemet.com
Panasonic	www.panasonic.com
Sanyo	www.secc.co.jp
Siliconix (Vishay)	www.vishay.com
Sumida	www.sumida.com
Taiyo Yuden	www.t-yuden.com
TDK	www.component.tdk.com
TOKO	www.tokoam.com

Table 3. Operating-Mode Truth Table

$\overline{SHDN}$	SUS	SKIP	OFS	OUTPUT VOLTAGE	OPERATING MODE
GND	X	X	X	GND	Low-Power Shutdown Mode. PWM_ outputs are forced low, and the controller is disabled. The supply current drops to 10µA (max).
V_{CC}	GND	GND	GND or REF	D0–D4 (no offset)	Normal Operation. The no-load output voltage is determined by the selected VID DAC code (D0–D4, Table 4).
V_{CC}	GND	V_{CC}	GND or REF	D0–D4 (no offset)	Pulse-Skipping Operation. When SKIP is pulled high, the MAX8707 immediately enters pulse-skipping operation allowing automatic PWM/PFM switchover under light loads. The VROK upper threshold is blanked.
V_{CC}	GND	X	0 to 0.8V or 1.2V to 2.0V	D0–D4 (plus offset)	Deep-Sleep Mode. The no-load output voltage is determined by the selected VID-DAC code (D0–D4, Table 4) plus the offset voltage set by OFS.
V_{CC}	V_{CC}	X	X	SUSV (no offset)	Suspend Mode/One Phase Skip. The no-load output voltage is determined by the suspend voltage present on SUSV, overriding all other active modes of operation.
V_{CC}	X	X	X	GND	Fault Mode. The fault latch has been set by either UVP or thermal shutdown. The controller remains in FAULT mode until V_{CC} power is cycled or $\overline{SHDN}$ toggled.

X = Don't Care

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to 2V, the offset amplifier adds a positive offset to the output that is equal to 1/8th the difference between the reference voltage and the voltage appearing at the OFS input (V_{OFFSET} = 0.125 x (V_{REF} - V_{OFS})). With this scheme, the controller supports both positive and negative offsets with a single input. The piecewise linear-transfer function is shown in Figure 3. The regions of the transfer function below zero, above 2.0V, and between 0.8V and 1.2V are undefined. OFS inputs are disallowed in these regions, and the respective effects on the output are not specified.

The controller disables the offset amplifier during suspend mode (SUS = high).

Nominal Output-Voltage Selection

The nominal no-load output voltage (V_{TARGET}) is defined by the selected voltage reference (VID DAC or SUSV) plus the offset voltage and remote ground-sense adjustment (V_{GNDS}) as defined in the following equation:

$$V_{TARGET} = V_{DAC} + V_{OFFSET} + V_{GNDS}$$

when SUS = GND

where V_{DAC} is the selected VID voltage during normal operation (SUS = low, Table 4), and V_{OFFSET} is the offset voltage defined by the OFS pin (Figure 3). In suspend mode (SUS = high), the offset voltage amplifier is disabled and the target voltage tracks the SUSV input voltage:

$$V_{TARGET} = V_{SUSV} + V_{GNDS}$$

when SUS = V_{CC}

The MAX8707 uses a multiplexer that selects from one of three different inputs (Figure 2)—the output of the VID DAC, the SUSV suspend voltage, or ground (controller disabled). On startup, the MAX8707 slews the target voltage from ground to either the decoded D0–D4 (SUS = low) voltage or the SUSV voltage (SUS = high).

DAC Inputs (D0–D4)

During normal forced-PWM operation (SUS = low), the DAC programs the output voltage using the D0–D4 inputs. D0–D4 are low-voltage (1.0V) logic inputs, designed to interface directly with the CPU. Do not leave D0–D4 unconnected. D0–D4 can be changed while the MAX8707 is active, initiating a transition to a new output-voltage level. Change D0–D4 together, avoiding greater than 50ns skew between bits. Otherwise, incorrect DAC readings may cause a partial transition to the wrong voltage level followed by the intended transition to the correct voltage level, lengthening the overall transition time. The available DAC codes and resulting output voltages are compatible with the AMD Hammer (Table 4) specifications.

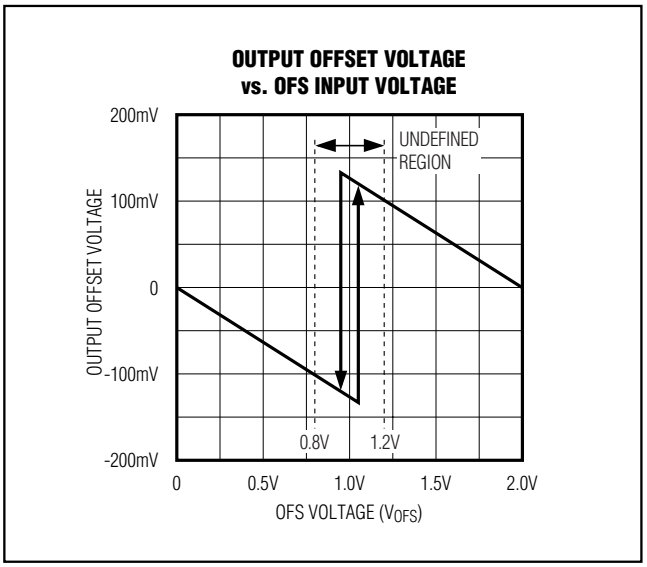

Figure 3. Output Offset Voltage vs. OFS Input Voltage

Suspend Mode

When the processor enters low-power suspend mode, the processor sets the regulator to a lower output voltage to reduce power consumption. The MAX8707 includes a buffered suspend-voltage input (SUSV) and a digital SUS control input. The suspend voltage is adjusted with an external resistive voltage-divider from REF to SUSV to analog ground. The suspend-voltage adjustment range is from 0.4V to 2.0V (V_{REF}).

When the CPU suspends operation (SUS = high), the controller disables the offset amplifier, overrides the 5-bit VID-DAC code set by D0–D4, and slews the output voltage to the target voltage set by the SUSV voltage. During the transition, the MAX8707 blanks both VROK thresholds until 20µs after the slew-rate controller reaches the suspend-mode voltage. Once the 20µs timer expires, the MAX8707 (SKIP pulled low) automatically switches to the 1-phase, pulse-skipping control scheme, forces $\overline{DRSKP}$ low, and blanks the upper VROK threshold.

Output-Voltage Transition Timing

The MAX8707 performs mode transitions in a controlled manner, automatically minimizing input surge currents. This feature allows the circuit designer to achieve nearly

Table 4. AMD Hammer Output-Voltage VID DAC Codes (SUS = GND)

D4	D3	D2	D1	D0	OUTPUT VOLTAGE (V)		D4	D3	D2	D1	D0	OUTPUT VOLTAGE (V)
0	0	0	0	0	1.550		1	0	0	0	0	1.150
0	0	0	0	1	1.525		1	0	0	0	1	1.125
0	0	0	1	0	1.500		1	0	0	1	0	1.100
0	0	0	1	1	1.475		1	0	0	1	1	1.075
0	0	1	0	0	1.450		1	0	1	0	0	1.050
0	0	1	0	1	1.425		1	0	1	0	1	1.025
0	0	1	1	0	1.400		1	0	1	1	0	1.000
0	0	1	1	1	1.375		1	0	1	1	1	0.975
0	1	0	0	0	1.350		1	1	0	0	0	0.950
0	1	0	0	1	1.325		1	1	0	0	1	0.925
0	1	0	1	0	1.300		1	1	0	1	0	0.900
0	1	0	1	1	1.275		1	1	0	1	1	0.875
0	1	1	0	0	1.250		1	1	1	0	0	0.850
0	1	1	0	1	1.225		1	1	1	0	1	0.825
0	1	1	1	0	1.200		1	1	1	1	0	0.800
0	1	1	1	1	1.175		1	1	1	1	1	No CPU*

**No-CPU Mode: The controller enters the no-CPU mode by ramping down the output voltage to 0V with the shutdown slew rate. When exiting the no-CPU mode, the controller ramps the output up to the new VID output voltage using the startup slew rate. In no-CPU mode, the controller remains in standby so VID transitions may be detected.*

ideal transitions, guaranteeing just-in-time arrival at the new output-voltage level with the lowest possible peak currents for a given output capacitance.

At the beginning of an output-voltage transition, the MAX8707 blanks both VROK thresholds, preventing the VROK open-drain output from changing states during the transition. The controller enables the lower VROK threshold approximately 20µs after the slew-rate controller reaches the target output voltage, but the upper VROK threshold is enabled only if the controller remains in forced-PWM operation. If the controller enters pulse-skipping operation, the upper VROK threshold remains blanked. The slew-rate (set by resistor R_{TIME}) must be set fast enough to ensure that the transition can be completed within the maximum allotted time.

When transitions occur in pulse-skipping mode, the MAX8707 sets OVP to 1.75V and disables the integrator at the beginning of all transitions. OVP remains at 1.75V and the integrator remains disabled until 20µs after the transition is completed (internal target settles) and the output is in regulation (an error-comparator edge is detected).

The MAX8707 automatically controls the current to the minimum level required to complete the transition in the calculated time. The slew-rate controller uses an internal capacitor and current source programmed by R_{TIME} to transition the output voltage. The total transition time depends on R_{TIME}, the voltage difference, and the accuracy of the slew-rate controller (C_{SLEW} accuracy). The slew rate is not dependent on the total output capacitance, as long as the surge current is less than the current limit set by ILIM(AVE) and ILIM(PK). For voltage transitions into and out of suspend mode, the transition time (t_{TRAN}) is given by:

$$t_{TRAN(SUS)} = \frac{|V_{NEW} - V_{OLD}|}{dV_{TARGET}/dt}$$

where $dV_{TARGET} / dt = 6.25mV/\mu s \times 143k\Omega / R_{TIME}$ is the slew rate, V_{OLD} is the original output voltage, and V_{NEW} is the new target voltage. See TIME Slew-Rate Accuracy in the *Electrical Characteristics* for t_{SLEW} limits. For soft-start and shutdown, the controller automatically reduces the slew rate by 1/4th:

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$$t_{TRAN(START)} = t_{TRAN(SHDN)} = \frac{4V_{TARGET}}{dV_{TARGET}/dt}$$

For all dynamic VID transitions, the rate at which the VID inputs (D0–D4) are clocked sets the slew rate, with a maximum slew-rate limit set by the R_{TIME} value. The practical range of R_{TIME} is 47kΩ to 392kΩ corresponding to slew rates of 19mV/µs to 2.28mV/µs, respectively. The output voltage tracks the slewed target voltage, making the transitions relatively smooth.

The average inductor current per phase required to make an output-voltage transition is:

$$I_L \cong \frac{C_{OUT}}{\eta_{PH}} \times (dV_{TARGET}/dt)$$

where dV_{TARGET} / dt is the required slew rate, C_{OUT} is the total output capacitance, and η_{PH} is the number of active phases.

Suspend Transition (Forced-PWM Operation Selected)

When the MAX8707 enters suspend mode while configured for forced-PWM operation (SKIP pulled low), the controller ramps the output voltage down to the programmed SUSV voltage at the slew rate determined by R_{TIME}. The controller blanks VROK (forced high impedance) until 20µs after the transition is completed—internal target voltage equals the SUSV voltage. After this blanking time expires, the controller automatically shuts down phases 2, 3, and 4 ($\overline{DRSKP}$ pulled low), and enters single-phase, pulse-skipping operation. VROK monitors only the lower threshold in skip mode.

When exiting suspend mode (SUS pulled low), the MAX8707 immediately activates all enabled phases ($\overline{DRSKP}$ driven high) so the output voltage may be ramped up at the slew rate set by R_{TIME}. The controller blanks VROK (forced high impedance) until 20µs after the transition is completed—internal target voltage equals the selected VID-DAC voltage.

Suspend Transition (Pulse-Skipping Operation Selected)

If the MAX8707 is configured for pulse-skipping operation (SKIP = high) when SUS goes high, the MAX8707 immediately disables phases 2, 3, and 4 ($\overline{DRSKP}$ pulled low) and enters pulse-skipping operation (Figure 5). The output drops at a rate determined by the load and the output capacitance. The internal target still ramps as before, and VROK remains high impedance until the new target is reached plus an extra 20µs. After this time expires, VROK monitors only the lower threshold.

When exiting deeper sleep (SUS pulled low), the MAX8707 starts to slew the internal target up towards the new target. The controller remains in skip mode while the output voltage is higher than the internal target. As the internal target approaches the output voltage, the MAX8707 activates all enabled phases ($\overline{DRSKP}$ driven high) so the output voltage may be ramped up at the slew rate set by R_{TIME}. The controller blanks VROK (forced high impedance) until 20µs after the transition is completed.

Forced-PWM Operation (Normal Mode)

During soft-start, soft-shutdown, and normal operation—when the CPU is actively running (SKIP = low, Table 5)—the MAX8707 operates with a low-noise, forced-PWM control scheme. Forced-PWM operation forces $\overline{DRSKP}$ high, instructing the drivers to disable their zero-crossing comparators and force the low-side gate-drive waveforms to constantly be the complement of the high-side gate-drive waveforms. This keeps the switching frequency constant and allows the inductor current to reverse under light loads, providing fast, accurate negative output-voltage transitions by quickly discharging the output capacitors.

Forced-PWM operation comes at a cost: the no-load +5V bias supply current remains between 10mA to 200mA per phase, depending on the external MOSFETs and switching frequency. To maintain high efficiency under light-load conditions, the controller switches to a low-power pulse-skipping control scheme after entering suspend mode.

Light-Load Pulse-Skipping Operation

The MAX8707 includes a light-load operating-mode control input (SKIP) used to disable extra phases and enable/disable the driver's zero-crossing comparator. When the driver's zero-crossing comparators are enabled ($\overline{DRSKP}$ pulled low), the controller forces PWM_ low for the disabled phases so the driver pulls DL_ low when its current-sense inputs detect zero inductor current. This keeps the inductor from discharging the output capacitors and forces the controller to skip pulses under light-load conditions to avoid overcharging the output. When the zero-crossing comparators are disabled, each controller maintains PWM operation under light-load conditions (forced PWM).

After the MAX8707 enters suspend mode while configured for forced-PWM operation (SKIP pulled low), the controller automatically switches to the pulse-skipping control scheme 20µs after the target voltage reaches the programmed SUSV voltage.

When pulse-skipping operation is enabled, the controller terminates the on-time when the output voltage exceeds the feedback threshold and when the current-

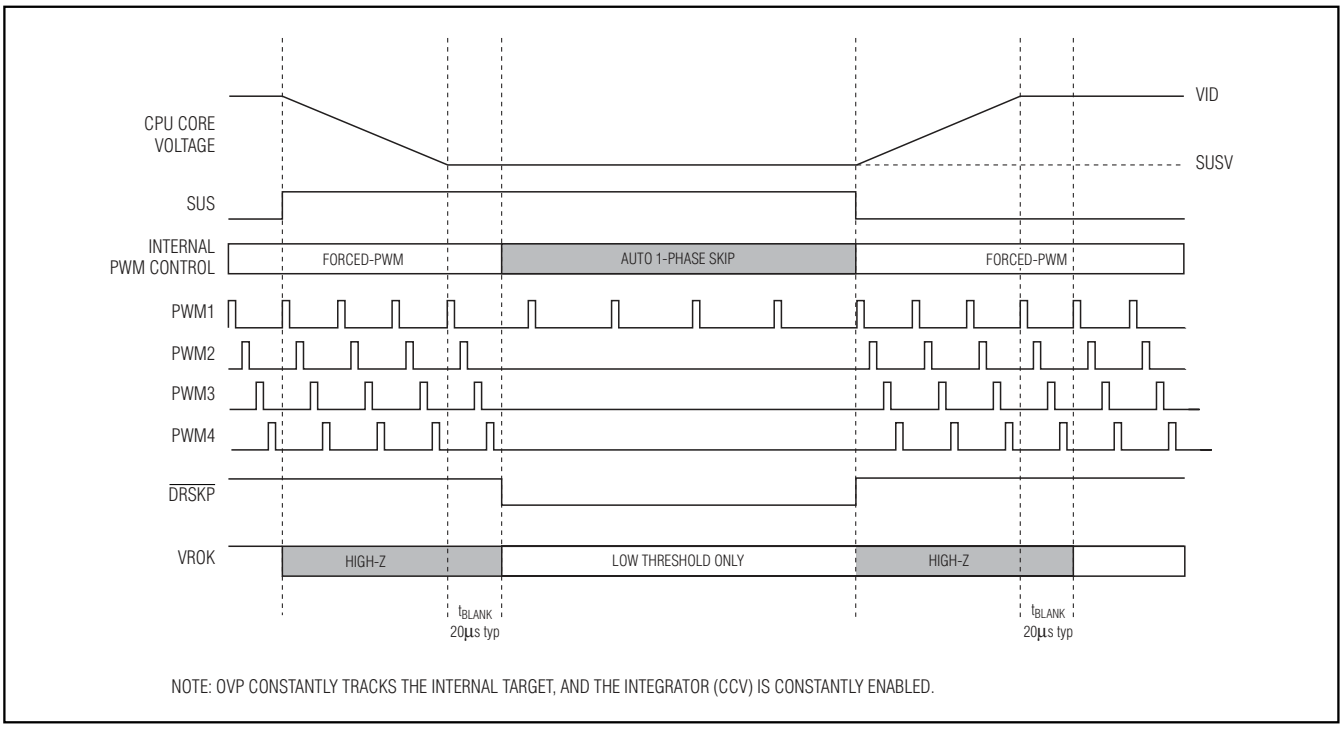

Figure 4. Suspend Transition in Forced-PWM Mode (SKIP = low)

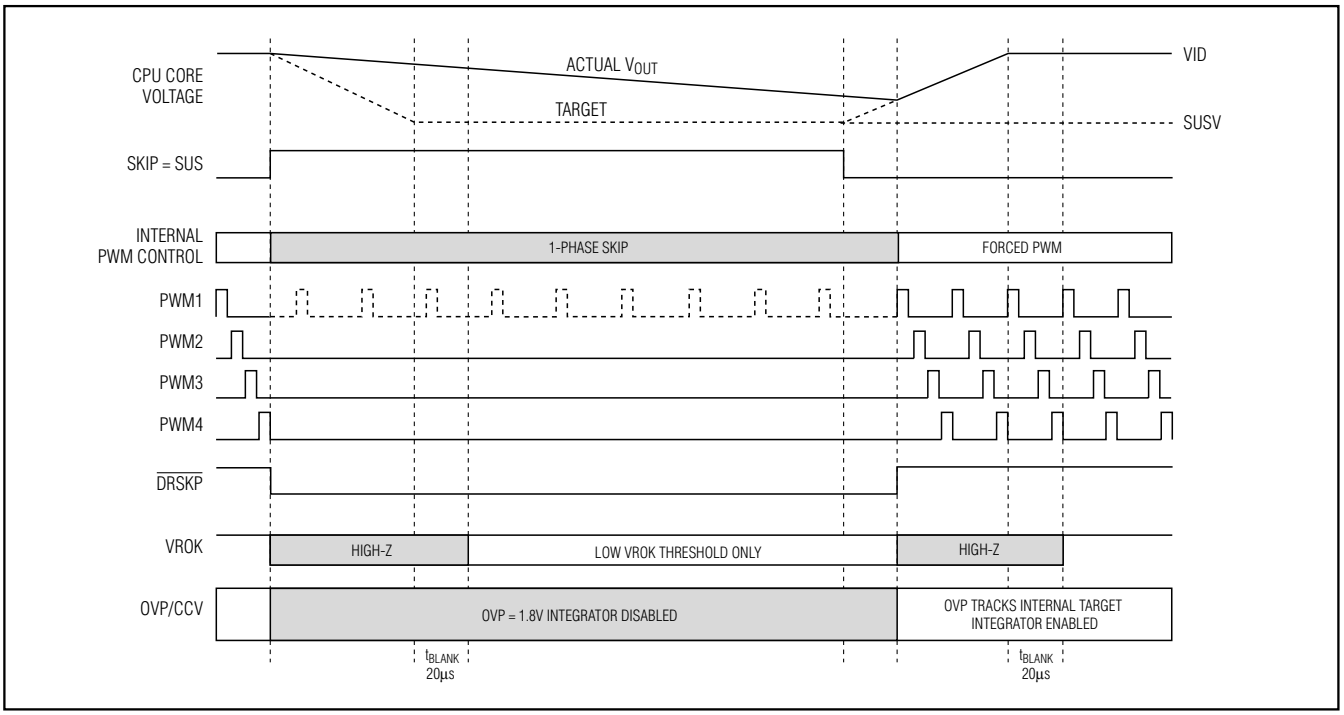

Figure 5. Suspend Transition in Pulse-Skipping Operation (SKIP = SUS)

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Table 5. SKIP Settings

SKIP (INPUT)	SUS (INPUT)	MODE	$\overline{\text{DRSKP}}$ (OUTPUT)	OPERATION
Low (GND)	Low (GND)	Multiphase Forced-PWM	High (V_{DD})	The controller operates with a constant switching frequency, providing low-noise forced-PWM operation. The controller disables the zero-crossing comparators, forcing the low-side gate-drive waveform to constantly be the complement of the high-side gate-drive waveform.
	High (3.3V or V_{CC})	1-Phase Pulse Skipping	Low (PGND)	The controller automatically switches to pulse-skipping operation 20µs after the target voltage reaches the SUSV voltage. Pulse-skipping operation forces the controller into PFM operation under light loads. Phase 1 remains active while the other three phases are disabled—PWM2, PWM3, and PWM4 pulled low.
High (>1.2V)	Don't Care	1-Phase Pulse Skipping	Low (PGND)	Pulse-skipping operation forces the controller into PFM operation under light loads. Phase 1 remains active while the other three phases are disabled—PWM2, PWM3, and PWM4 pulled low.

sense voltage exceeds the Idle Mode™ current-sense threshold (V_{IDLE} = 0.1 x $V_{PKLIMIT}$). Under heavy-load conditions, the continuous inductor current remains above the Idle-Mode current-sense threshold, so the on-time depends only on the feedback-voltage threshold. Under light-load conditions, the controller remains above the feedback-voltage threshold, so the on-time duration depends solely on the Idle-Mode current-sense threshold, which is approximately 10% of the full-load current-limit threshold set by ILIM(PK).

When the controller enters suspend mode while SKIP is pulled high, the multiphase controller immediately disables three phases, and only the main phase (PWM1) remains active. When pulse skipping, the controller blanks the upper VROK threshold and the OVP threshold tracks the selected VID DAC code. The MAX8707 automatically uses forced-PWM operation during soft-start and soft-shutdown, regardless of the SKIP configuration.

Idle-Mode Current Sense Threshold

The Idle-Mode current-sense threshold forces a lightly loaded regulator to source a minimum amount of energy with each on-time since the controller cannot terminate the on-time until the current-sense voltage exceeds the Idle-Mode current-sense threshold (V_{IDLE} = 0.1 x $V_{PKLIMIT}$). Since the zero-crossing comparator prevents the switching regulator from sinking current, the controller must skip pulses to avoid overcharging the output. When the clock edge occurs, if the output voltage still exceeds the feedback threshold, the controller does not initiate another on-time. This forces the controller to actually regulate the valley of the output voltage ripple under light-load conditions.

Automatic Pulse-Skipping Crossover

In skip mode, the MAX8707 disables three phases and forces $\overline{\text{DRSKP}}$ low to instruct the skip-mode drivers to activate their zero-crossing comparators. Therefore, an inherent automatic switchover to PFM takes place at light loads (Figure 6), resulting in a highly efficient operating mode. This switchover is affected by a comparator that truncates the low-side switch on-time at the inductor current's zero crossing. The driver's zero-crossing comparator senses the inductor current across the low-side MOSFET (refer to the skip-mode driver data sheet). Once V_{LX} - V_{PGND} drops below the zero-crossing threshold, the driver forces DL low. This mechanism causes the threshold between pulse-skipping PFM and nonskipping PWM operation to coincide with the boundary between continuous and discontinuous inductor-current operation (also known as the critical conduction point). The load-current level at which the PFM/PWM crossover occurs, $I_{LOAD(SKIP)}$, is given by:

$$I_{LOAD(SKIP)} = \frac{V_{OUT}(V_{IN} - V_{OUT})}{2V_{IN}f_{SW}L}$$

The switching waveforms may appear noisy and asynchronous when light loading causes pulse-skipping operation, but this is a normal operating condition that

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results in high light-load efficiency. Trade-offs in PFM noise vs. light-load efficiency are made by varying the inductor value. Generally, low inductor values produce a broader efficiency vs. load curve, while higher values result in higher full-load efficiency (assuming that the coil resistance remains fixed) and less output voltage ripple. Penalties for using higher inductor values include larger physical size and degraded load-transient response (especially at low input-voltage levels).

Current Sense

The output current of each phase is sensed differentially. Each phase of the MAX8707 has an independent return path for fully differential current-sense. A low offset voltage and high-gain (10V/V) differential current amplifier at each phase allow low-resistance current-sense resistors to be used to minimize power dissipation. Sensing the current at the output of each phase offers advantages, including less noise sensitivity, more accurate current sharing between phases, and the flexibility of using either a current-sense resistor or the DC resistance of the output inductor.

Using the DC resistance (R_{DCR}) of the output inductor allows higher efficiency. In this configuration, the initial tolerance and temperature coefficient of the inductor's DCR must be accounted for in the output-voltage droop-error budget. This current-sense method uses an RC filtering network to extract the current information from the output inductor (Figure 7). The time constant of the RC network should match the inductor's time constant (L/R_{DCR}):

$$\frac{L}{R_{DCR}} = R_{EQ}\, C_{SENSE}$$

where C_{SENSE} is the sense capacitor and R_{EQ} is the equivalent sense resistance. To minimize the current-sense error due to the current-sense inputs' bias current ($I_{CSP\_}$ and $I_{CSN\_}$), choose R_{EQ} less than 2kΩ and use the above equation to determine the sense capacitance (C_{SENSE}). Choose capacitors with 5% tolerance and resistors with 1% tolerance specifications. Temperature compensation is recommended for this current-sense method.

When using a current-sense resistor for accurate output-voltage positioning (CRSP to CRSN for the MAX8707), differential RC-filter circuits should be used to cancel the equivalent series inductance of the current-sense resistor (Figure 7). Similar to inductor DCR-sensing methods, the RC filter's time constant should match the L/R time constant formed by the current-sense resistor's parasitic inductance:

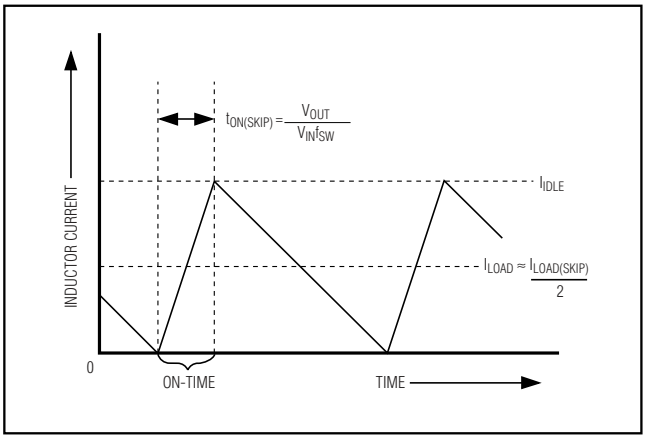

Figure 6. Pulse-Skipping/Discontinuous Crossover Point

$$\frac{L_{ESL}}{R_{SENSE}} = R_{EQ}\, C_{SENSE}$$

where L_{ESL} is the equivalent series inductance of the current-sense resistor, R_{SENSE} is the current-sense resistance value, C_{SENSE} is the compensation capacitor, and R_{EQ} is the equivalent compensation resistance.

Current Balance

The fixed-frequency, multiphase, current-mode architecture automatically forces the individual phases to remain current balanced. After the oscillator triggers an on-time, the controller does not terminate the on-time until the amplified differential current-sense voltage reaches the integrated threshold voltage (V_{REF} - V_{TRC}). This control scheme regulates the peak inductor current of each phase, forcing them to remain properly balanced. Therefore, the average inductor-current variation depends mainly on the variation in the current-sense element and inductance value.

Peak/Average Current Limit

The MAX8707 current-limit circuit employs a fast peak inductor current-sensing algorithm. Once the current-sense signal (CSP to CSN) of the active phase exceeds the peak current-limit threshold, the PWM controller terminates the on-time. The MAX8707 also includes a slower average current sense that uses a current-sense resistor between CRSP and CRSN to accurately limit the inductor current. When this average current-sense threshold is exceeded, the current-limit circuit lowers the peak current-limit threshold, effectively lowering the average inductor current. See the *Current Limit* section in the *Design Procedure* section.

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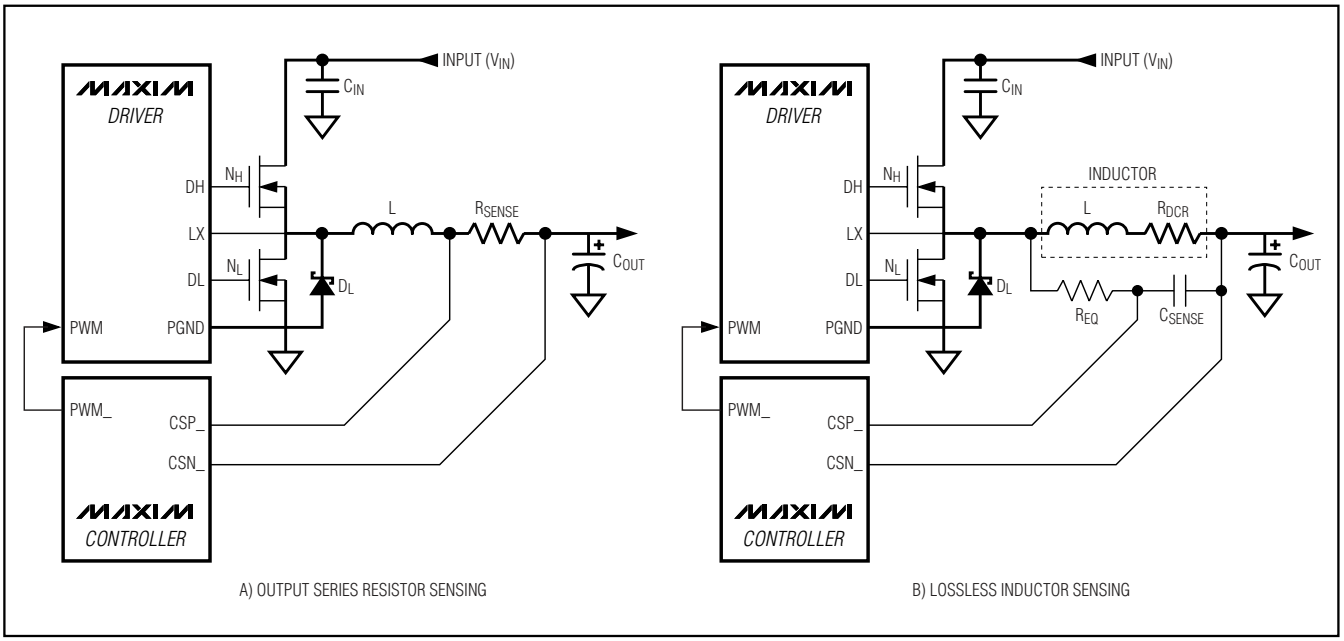

Figure 7. Current-Sense Methods

Power-Up Sequence (POR, UVLO)

Power-on reset (POR) occurs when V_{CC} rises above approximately 2V, resetting the fault latch and preparing the controller for operation. The V_{CC} undervoltage-lockout (UVLO) circuitry inhibits switching—forces $\overline{DRSKP}$ high and pulls the PWM_ outputs low—until V_{CC} rises above 4.25V. The controller powers up the reference once the system enables the controller—V_{CC} above 4.25V and $\overline{SHDN}$ pulled high. With the reference in regulation, the controller begins to slew the output voltage to the target voltage—either the output of the VID DAC (SUS = low) or the SUSV suspend voltage (SUS = high)—at 1/4th the slew rate set by R_{TIME}:

$$t_{TRAN(START)} = \frac{4V_{TARGET}}{dV_{TARGET}/dt}$$

where $dV_{TARGET} / dt = 6.25mV/\mu s \times 143k\Omega / R_{TIME}$ is the slew rate. The soft-start circuitry does not use a variable current limit, so full output current is available immediately. VROK becomes high impedance approximately 20µs after the MAX8707 reaches the target voltage.

For automatic startup, the battery voltage should be present before V_{CC}. If the controller attempts to bring the output into regulation without the battery voltage present, the fault latch trips. The controller remains shut down until the fault latch is cleared by toggling $\overline{SHDN}$ or cycling the V_{CC} power supply below 1V.

If the V_{CC} voltage drops below 4.25V, the controller assumes that there is not enough supply voltage to make valid decisions. To protect the output from overvoltage faults, the controller shuts down immediately—forces $\overline{DRSKP}$ high and pulls the PWM_ outputs low.

Shutdown

When $\overline{SHDN}$ goes low, the MAX8707 enters low-power shutdown mode. VROK is pulled low immediately, and the output voltage ramps down at 1/4th the slew rate set by R_{TIME}:

$$t_{TRAN(SHDN)} = \frac{4V_{OUT}}{dV_{TARGET}/dt}$$

where $dV_{TARGET} / dt = 6.25mV/\mu s \times 143k\Omega / R_{TIME}$ is the slew rate. Slowly discharging the output capacitors by slewing the output over a long period of time keeps the average negative inductor current low (damped response), thereby eliminating the negative output voltage excursion that occurs when the controller discharges the output quickly by permanently turning on the low-side MOSFET (underdamped response). This eliminates the need for the Schottky diode normally connected between the output and ground to clamp

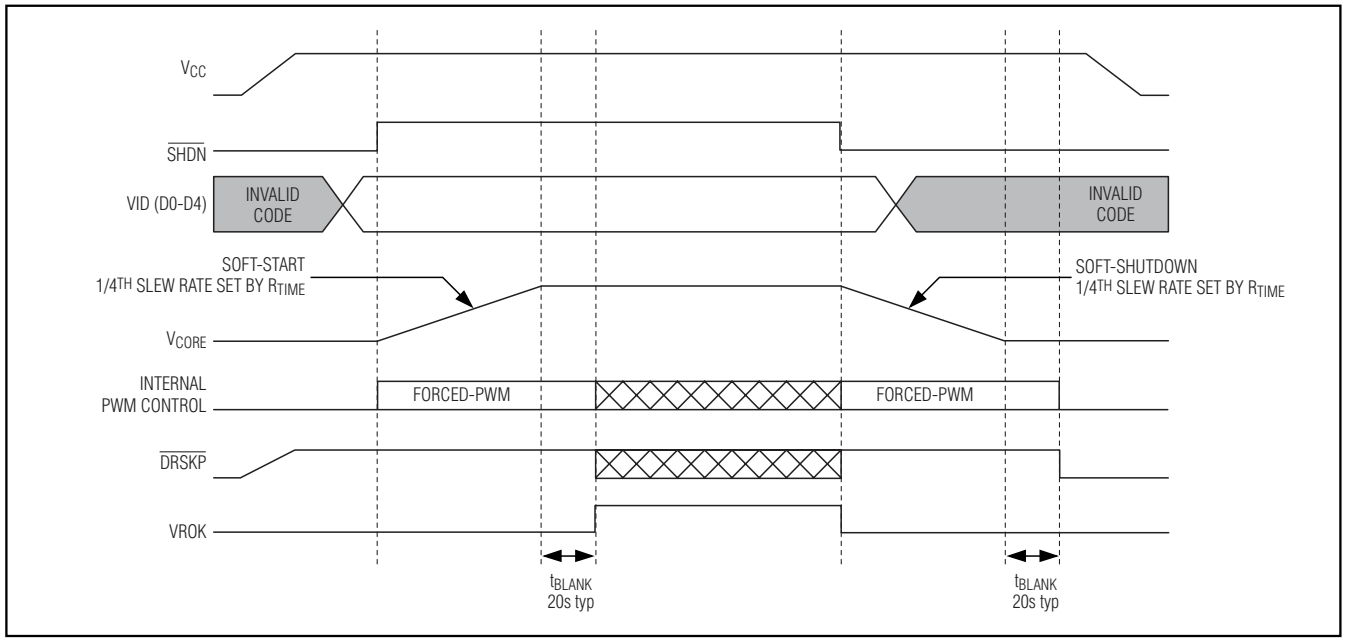

Figure 8. Power-Up and Shutdown Sequence Timing Diagram

the negative output-voltage excursion. When the controller reaches the 0V target, the drivers are disabled ($\overline{DRSKP}$ driven low and PWM_ outputs pulled low), the reference turns off, and the supply current drops to about 10µA (max). When a fault condition—output UVLO or thermal shutdown—activates the shutdown sequence, the protection circuitry sets the fault latch to prevent the controller from restarting. To clear the fault latch and reactivate the controller, toggle $\overline{SHDN}$ or cycle V_{CC} power below 1V.

Fault Protection

Output Overvoltage Protection (Unlatched)

The overvoltage-protection (OVP) circuit is designed to protect the CPU against a shorted high-side MOSFET by drawing high current and blowing the battery fuse. The MAX8707 continuously monitors the output for an overvoltage fault. The controller detects an OVP fault if the output voltage exceeds the set target voltage by more than 200mV. After entering pulse-skipping operation (SKIP rising edge), the OVP threshold is set to 1.75V until the output voltage drops below the target voltage for the first time. Once the MAX8707 detects the output is being regulated ($V_{OUT} \approx V_{TARGET}$), the OVP threshold begins tracking the target voltage again. When the OVP circuit detects an overvoltage fault, it immediately enters forced-PWM operation—pulling $\overline{DRSKP}$ high so the drivers force the low-side gate drivers high (DL = V_{DD}) and pull the high-side gate drivers low (DH = LX). The controller does not initiate an on-time pulse until the output voltage drops below the OVP threshold. This action turns on the synchronous-rectifier MOSFET with 100% duty and, in turn, rapidly discharges the output filter capacitor and forces the output low. If the condition that caused the overvoltage (such as a shorted high-side MOSFET) persists, the battery fuse blows.

Overvoltage protection can be disabled through the no-fault test mode (see the *No-Fault Test Mode* section).

Output Undervoltage Protection (Latched)

The output undervoltage-protection (UVP) function is similar to foldback current limiting, but employs a timer rather than a variable current limit. If the MAX8707 output voltage is under 70% of the nominal value, the controller activates the shutdown sequence and sets the fault latch. Once the controller ramps down to the 0V setting, it forces the PWM_ driver outputs low. Toggle $\overline{SHDN}$ or cycle the V_{CC} power supply below 1V to clear the fault latch and reactivate the controller.

UVP can be disabled through the no-fault test mode (see the *No-Fault Test Mode* section).

Thermal Fault Protection (Latched)

The MAX8707 features a thermal fault-protection circuit. When the junction temperature rises above +160°C, a

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thermal sensor sets the fault latch and activates the soft-shutdown sequence. Once the controller ramps down to the 0V setting, it forces the PWM_ driver outputs low. Toggle $\overline{SHDN}$ or cycle the V_{CC} power supply below 1V to clear the fault latch and reactivate the controller after the junction temperature cools by 15°C.

Thermal shutdown can be disabled through the no-fault test mode (see the *No-Fault Test Mode* section).

No-Fault Test Mode

The latched fault protection features can complicate the process of debugging prototype breadboards since there are (at most) a few milliseconds in which to determine what went wrong. Therefore, a no-fault test mode is provided to disable the fault protection—overvoltage protection, undervoltage protection, and thermal shutdown. Additionally, the test mode clears the fault latch if it has been set. The no-fault test mode is entered by forcing 11V to 13V on $\overline{SHDN}$.

Multiphase, Fixed-Frequency Design Procedure

Firmly establish the input voltage range and maximum load current before choosing a switching frequency and inductor operating point (ripple-current ratio). The primary design trade-off lies in choosing a good switching frequency and inductor operating point, and the following four factors dictate the rest of the design:

Input Voltage Range: The maximum value ($V_{IN(MAX)}$) must accommodate the worst-case high AC-adapter voltage. The minimum value ($V_{IN(MIN)}$) must account for the lowest input voltage after drops due to connectors, fuses, and battery selector switches. If there is a choice at all, lower input voltages result in better efficiency.

Maximum Load Current: There are two values to consider. The peak load current ($I_{LOAD(MAX)}$) determines the instantaneous component stresses and filtering requirements, and thus drives output capacitor selection, inductor saturation rating, and the design of the current-limit circuit. The continuous load current (I_{LOAD}) determines the thermal stresses and thus drives the selection of input capacitors, MOSFETs, and other critical heat-contributing components. Modern notebook CPUs generally exhibit $I_{LOAD} = I_{LOAD(MAX)} \times 80\%$.

For multiphase systems, each phase supports a fraction of the load, depending on the current balancing. When properly balanced, the load current is evenly distributed among each phase:

$$I_{LOAD(PHASE)} = \frac{I_{LOAD}}{\eta_{PH}}$$

where η_{PH} is the total number of active phases.

Switching Frequency: This choice determines the basic trade-off between size and efficiency. The optimal frequency is largely a function of maximum input voltage, due to MOSFET switching losses that are proportional to frequency and V_{IN}^2. The optimum frequency is also a moving target, due to rapid improvements in MOSFET technology that are making higher frequencies more practical.

Inductor Operating Point: This choice provides trade-offs between size vs. efficiency and transient response vs. output noise. Low inductor values provide better transient response and smaller physical size, but also result in lower efficiency and higher output noise due to increased ripple current. The minimum practical inductor value is one that causes the circuit to operate at the edge of critical conduction (where the inductor current just touches zero with every cycle at maximum load). Inductor values lower than this grant no further size-reduction benefit. The optimum operating point is usually found between 20% and 50% ripple current.

Inductor Selection

The switching frequency and operating point (% ripple current or LIR) determine the inductor value as follows:

$$L = \eta_{PH}\left(\frac{V_{IN} - V_{OUT}}{f_{SW}\, I_{LOAD(MAX)}\, LIR}\right)\left(\frac{V_{OUT}}{V_{IN}}\right)$$

where η_{PH} is the total number of phases, and f_{SW} is the switching frequency per phase.

Find a low-loss inductor with the lowest possible DC resistance that fits in the allotted dimensions. If using a swinging inductor (where the no-load inductance decreases linearly with increasing current), evaluate the LIR with properly scaled inductance values. For the selected inductance value, the actual peak-to-peak inductor ripple current ($\Delta I_{INDUCTOR}$) is defined by:

$$\Delta I_{INDUCTOR} = \frac{V_{OUT}(V_{IN} - V_{OUT})}{V_{IN}\, f_{SW}\, L}$$

Ferrite cores are often the best choice, although powdered iron is inexpensive and can work well at 200kHz. The core must be large enough not to saturate at the peak inductor current (I_{PEAK}):

$$I_{PEAK} = \left(\frac{I_{LOAD(MAX)}}{\eta_{PH}}\right) + \left(\frac{\Delta I_{INDUCTOR}}{2}\right)$$

Current Limit

Peak Inductor Current Limit (ILIM(PK))

The MAX8707 overcurrent protection employs a peak current-sensing algorithm that uses either current-sense resistors or the inductor's DCR as the current-sense element (see the *Current Sense* section). Since the controller limits the peak inductor current, the maximum average load current is less than the peak current-limit threshold by an amount equal to half the inductor ripple current. Therefore, the maximum load capability is a function of the current-sense resistance, inductor value, switching frequency, and input voltage. When combined with the undervoltage-protection circuit, this current-limit method is highly effective.

The peak current-limit threshold is set with a single external resistor between ILIM(PK) and analog ground, where the resistor is determined by the following equation:

$$R_{ILIM(PK)} = \frac{8V \times R_{TRC}}{I_{PKLIMIT}\, R_{SENSE}}$$

where R_{SENSE} is the resistance value of the current-sense element (inductors' DCR or current-sense resistor), R_{TRC} is the resistance between TRC and REF, and $I_{PKLIMIT}$ is the desired peak current limit (per phase). The peak current-limit-threshold voltage adjustment range is from 20mV to 80mV.

The peak current-limit circuit also prevents excessive reverse inductor currents when V_{OUT} is sinking current. The negative current-limit threshold is equivalent to the positive current limit, and tracks the positive current limit when $R_{ILIM(PK)}$ or R_{TRC} are adjusted. When a phase drops below the negative current limit, the controller activates an on-time pulse at the next clock edge, regardless of the error-amplifier state, until the inductor current rises above the negative current-limit threshold.

Average Inductor Current-Limit (ILIM(AVE))

The MAX8707 also uses the accurate CRSP to CRSN current-sense voltage to limit the average current per phase. When the average current-limit threshold is exceeded, the controller internally reduces the peak inductor current-limit threshold (ILIM(PK)) until the average current remains within the programmed limits. When the accurate current sensing is disabled (CRSP = V_{CC}), the average current-limit circuit is disabled.

The average current-limit threshold defaults to 25mV if ILIM(AVE) is connected to V_{CC}. In adjustable mode, the average current-limit threshold voltage is precisely 1/20th the voltage difference between ILIM(AVE) and the reference:

$$V_{LAVE} = \frac{V_{REF} - V_{ILIM(AVE)}}{20}$$

The logic threshold for switchover to the 25mV default value is approximately V_{CC} - 1V. The average current-limit circuit also prevents against excessive reverse inductor current when V_{OUT} is sinking current. The negative current-limit threshold is equivalent to the positive current limit, and tracks the positive current limit when V_{LAVE} is adjusted.

Output-Capacitor Selection

The output filter capacitor must have low enough effective series resistance (ESR) to meet output ripple and load-transient requirements. In CPU V_{CORE} converters and other applications where the output is subject to large load transients, the output capacitor's size typically depends on how much ESR is needed to prevent the output from dipping too low under a load transient. Ignoring the sag due to finite capacitance:

$$(R_{ESR} + R_{PCB}) \le \frac{V_{STEP}}{\Delta I_{LOAD(MAX)}}$$

In non-CPU applications, the output capacitor's size often depends on how much ESR is needed to maintain an acceptable level of output ripple voltage. The output ripple voltage of a step-down controller equals the total inductor ripple current multiplied by the output capacitor's ESR. When operating multiphase systems out-of-phase, the peak inductor currents of each phase are staggered, resulting in lower output ripple voltage (V_{RIPPLE}) by reducing the total inductor ripple current. For nonoverlapping, multiphase operation ($V_{IN} \ge \eta_{PH} \times V_{OUT}$), the maximum ESR to meet the output-ripple-voltage requirement is:

$$R_{ESR} \le \left[\frac{V_{IN}\, f_{SW}\, L}{(V_{IN} - \eta_{PH}\, V_{OUT})V_{OUT}}\right] V_{RIPPLE}$$

where η_{PH} is the total number of active phases, and f_{SW} is the switching frequency per phase. The actual capacitance value required relates to the physical size needed to achieve low ESR, as well as to the chemistry of the capacitor technology. Thus, the capacitor selection is usually limited by ESR and voltage rating rather than by capacitance value (this is true of polymer types).

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The capacitance value required is determined primarily by the output transient-response requirements. Low inductor values allow the inductor current to slew faster, replenishing the charge removed from or added to the output filter capacitors by a sudden load step. Therefore, the amount of output soar when the load is removed is a function of the output voltage and inductor value. The minimum output capacitance required to prevent overshoot (V_{SOAR}) due to stored inductor energy can be calculated as:

$$C_{OUT} \geq \frac{(\Delta I_{LOAD(MAX)})^2 L}{2\eta_{PH} V_{OUT} V_{SOAR}}$$

where η_{PH} is the total number of active phases. When using low-capacity ceramic filter capacitors, capacitor size is usually determined by the capacity needed to prevent V_{SOAR} from causing problems during load transients. Generally, once enough capacitance is added to meet the overshoot requirement, undershoot at the rising load edge is no longer a problem.

Input Capacitor Selection

The input capacitor must meet the ripple-current requirement (I_{RMS}) imposed by the switching currents. The multiphase controllers operate out-of-phase, which reduces the RMS input current by dividing the input current between several staggered stages. For duty cycles less than 100%/η_{PH} per phase, the I_{RMS} requirements can be determined by the following equation:

$$I_{RMS} = \left(\frac{I_{LOAD}}{\eta_{PH} V_{IN}}\right)\sqrt{\eta_{PH} V_{OUT}(V_{IN} - \eta_{PH} V_{OUT})}$$

where η_{PH} is the total number of out-of-phase switching regulators. The worst-case RMS current requirement occurs when operating with $V_{IN} = 2\eta_{PH} V_{OUT}$. At this point, the above equation simplifies to $I_{RMS} = 0.5 \times I_{LOAD} / \eta_{PH}$.

For most applications, nontantalum chemistries (ceramic, aluminum, or OS-CON) are preferred due to their resistance to inrush surge currents, typical of systems with a mechanical switch or connector in series with the input. If the MAX8707 is operated as the second stage of a two-stage power-conversion system, tantalum input capacitors are acceptable. In either configuration, choose an input capacitor that exhibits less than 10°C temperature rise at the RMS input current for optimal circuit longevity.

Setting Voltage Positioning

Voltage positioning dynamically lowers the output voltage in response to the load current, reducing the output capacitance and processor's power-dissipation requirements. The controller uses two transconductance amplifiers to set the transient and DC output voltage droop (Figure 2). The transient-compensation (TRC) amplifier determines how quickly the MAX8707 responds to the load transient. The slower voltage-positioning (VPS) amplifier adjusts the steady-state regulation voltage as a function of the load. This adjustability allows flexibility in the selected current-sense resistor value or inductor DCR, and allows smaller current-sense resistance to be used, reducing the overall power dissipated.

Steady-State Voltage Positioning

Connect a resistor (R_{VPS}) between VPS and FBS to set the DC steady-state droop (load line) based on the required DC voltage-positioning slope (R_{DROOP}):

$$R_{VPS} = \frac{R_{DROOP}}{R_{SENSE} G_{M(VPS)}}$$

where the current-sense resistance (R_{SENSE}) depends on the current-sense method, and the voltage-positioning amplifier's transconductance ($G_{M(VPS)}$) is typically 200µS as defined in the *Electrical Characteristics* table. When the MAX8707 CRS sensing is enabled, R_{SENSE} is defined as the accurate CRS current-sense resistance:

$$R_{SENSE} = R_{CRS}$$

when CRS sensing is enabled.

When the MAX8707 CRS sensing is disabled, the controller sums together the input signals of the current-sense inputs (CSP_, CSN_). These inputs typically use the inductors' DC resistance (R_{DCR}) to sense the current, so R_{SENSE} is defined as the average of the effective CS current-sense resistances (see the *Current Sense* section):

$$R_{SENSE} = R_{DCR}$$

when CRS sensing is disabled.

When the inductors' DCR (R_{DCR}) is used as the current-sense elements (for lossless sensing), R_{VPS} should include an NTC thermistor to minimize the temperature dependence of the voltage-positioning slope.

To avoid output-voltage errors caused by the voltage-positioning current, a second transconductance amplifier generates an equivalent current on the FBS input. Accurate MAX8707 CRS sensing is disabled by connecting CRSP to V_{CC}.

Disable voltage positioning by shorting VPS directly to FBS.

Transient Droop

Connect a resistor (R_{TRC}) between TRC and REF to set the transient droop ($R_{DROOP(AC)}$) based on the voltage-positioning requirements. TRC allows the controller to quickly respond to load transients, but it does not affect the DC steady-state droop. Choose R_{TRC} based on the equation:

$$R_{TRC} = \frac{R_{TRANS}R_{CS}}{\eta_{PH}R_{DROOP(AC)}}$$

where R_{CS} is the current-sense element connected from CSP_ to CSN_ (which is typically the inductor's effective DCR: $R_{CS} = L / R_{EQ}C_{SENSE}$), R_{TRANS} is the current-sense amplifier gain divided by the transient amplifier's transconductance as defined in the *Electrical Characteristics* table, and $R_{DROOP(AC)}$ is typically 80% of the DC voltage-positioning slope to minimize the transient sag voltage.

The TRC resistance also sets the small-signal loop gain, so a maximum R_{TRC} value is required for stability, even if voltage positioning is not used (VPS = FBS).

$$V_{RIPPLE}\ R_{TRC} < (R_{TRANS}\ R_{SENSE}\ \Delta I_L) / 3$$

TRC is high impedance in shutdown.

Applications Information

Duty-Cycle Limits

Minimum Input Voltage

The minimum input operating voltage (dropout voltage) is restricted by stability requirements, not the minimum off-time ($t_{OFF(MIN)}$). The MAX8707 does not include slope compensation, so the controller becomes unstable with duty cycles greater than 50% per phase:

$$V_{IN(MIN)} \geq 2V_{OUT(MAX)}$$

However, the controller may briefly operate with duty cycles over 50% during heavy load transients.

Maximum Input Voltage

The MAX8707 controller and driver has a minimum on-time, which determines the maximum input operating voltage that maintains the selected switching frequency. With higher input voltages, each pulse delivers more energy than the output is sourcing to the load. At the beginning of each cycle, if the output voltage is still above the feedback threshold voltage, the controller does not trigger an on-time pulse resulting in pulse-skipping operation regardless of the operating mode selected by SKIP. This allows the controller to maintain regulation above the maximum input voltage, but forces the controller to effectively operate with a lower switching frequency. This results in an input threshold voltage at which the controller begins to skip pulses ($V_{IN(SKIP)}$):

$$V_{IN(SKIP)} = V_{OUT}\left(\frac{1}{f_{SW}t_{ON(MIN)}}\right)$$

where f_{SW} is the switching frequency per phase selected by OSC, and $t_{ON(MIN)}$ is 110ns plus the driver's turn-off delay (PWM low to LX low) minus the driver's turn-on delay (PWM high to LX high). For the best high-voltage performance, use the slowest switching-frequency setting (200kHz per phase, OSC = GND).

PC Board Layout Guidelines

Careful PC board layout is critical to achieve low switching losses and clean, stable operation. The switching power stage requires particular attention (Figure 9). If possible, mount all of the power components on the top side of the board with their ground terminals flush against one another. Follow these guidelines for good PC board layout:

1) Keep the high-current paths short, especially at the ground terminals. This is essential for stable, jitter-free operation.
2) Connect all analog grounds to a separate solid copper plane, which connects to the GND pin of the controller. This includes the V_{CC} bypass capacitor, REF and GNDS bypass capacitors, compensation (CCV, TRC) components, and the resistive dividers connected to $I_{LIM(AVE)}$, SUSV, and OFS.
3) Keep the power traces and load connections short. This is essential for high efficiency. The use of thick copper PC boards (2oz vs. 1oz) can enhance full-load efficiency by 1% or more. Correctly routing PC board traces is a difficult task that must be approached in terms of fractions of centimeters, where a single mΩ of excess trace resistance causes a measurable efficiency penalty.
4) Connections for current limiting (CSP_, CSN_) and voltage positioning (CRSP, CRSN) must be made using Kelvin-sense connections to guarantee the current-sense accuracy.
5) Route high-speed switching nodes and driver traces away from sensitive analog areas (REF, CCV, TRC, VPS, etc.). Make all pin-strap control input connections ($\overline{SHDN}$, SKIP, SUS, OSC) to analog ground or V_{CC} rather than power ground or V_{DD}.
6) Keep the drivers close to the MOSFET, with the gate-drive traces (DL, DH, LX, and BST) short and wide to minimize trace resistance and inductance.

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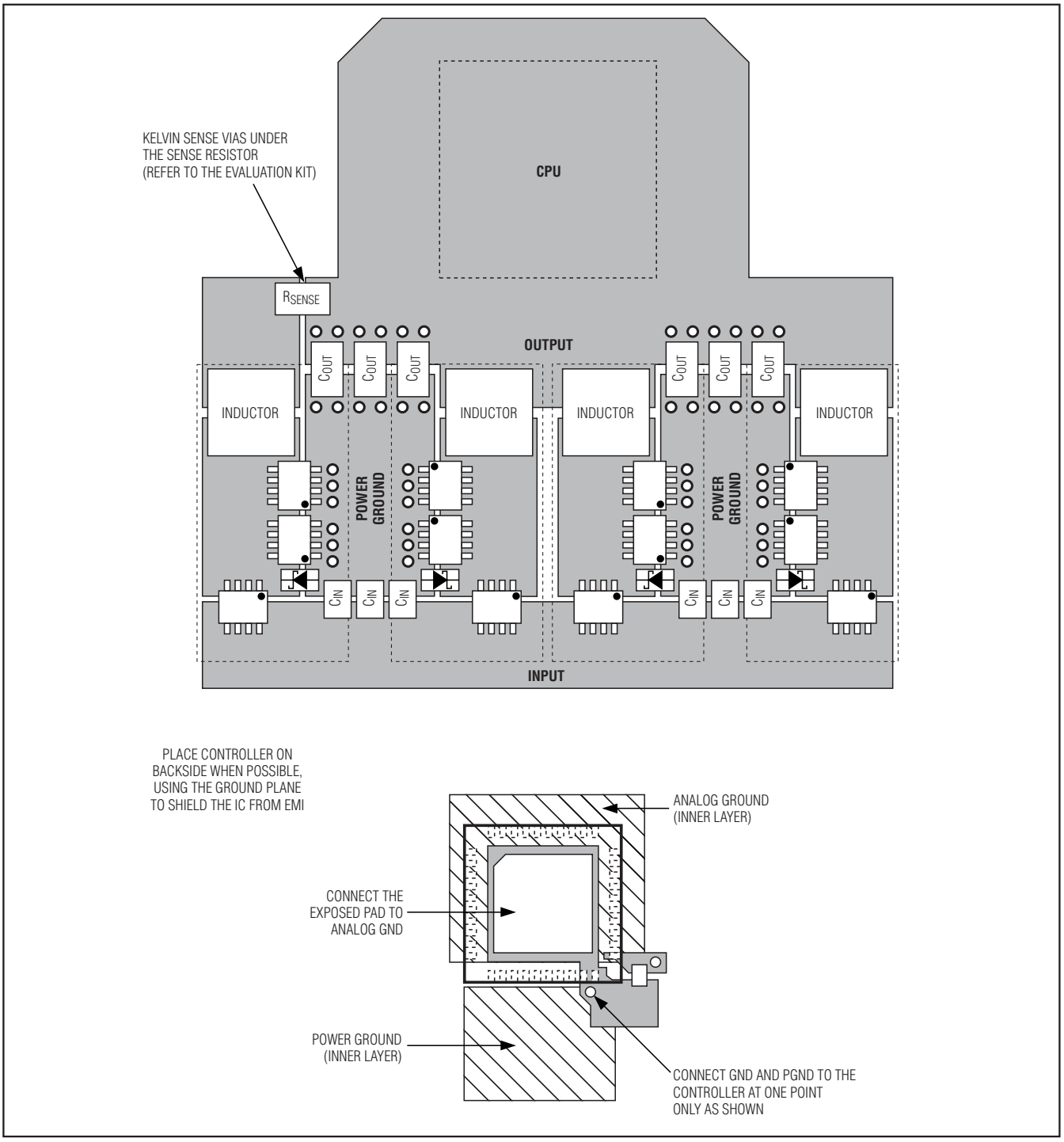

Figure 9. PC Board Layout Example

This is essential for high-power MOSFETs that require low-impedance gate drivers to avoid shoot-through currents.

7) When trade-offs in trace lengths must be made, it's preferable to allow the inductor charging path to be made longer than the discharge path. For example, it's better to allow some extra distance between the input capacitors and the high-side MOSFET than to allow distance between the inductor and the low-side MOSFET or between the inductor and the output filter capacitor.

Layout Procedure

1) Place the power components first, with ground terminals adjacent (low-side MOSFET source, C_{IN}, C_{OUT}, and D1 anode). If possible, make all these connections on the top layer with wide, copper-filled areas.
2) Mount the driver IC adjacent to the low-side MOSFETs. The DL gate traces must be short and wide (50mils to 100mils wide if the MOSFET is 1in from the driver IC).
3) Group the gate-drive components (BST diodes and capacitors, V_{DD} bypass capacitor) together near the driver IC.
4) Make the DC-DC controller ground connections as shown in the *Standard Application Circuits*. This diagram can be viewed as having three separate ground planes: input/output ground, where all the high-power components go; the power ground plane, where the PGND pin, V_{DD} bypass capacitor, and driver IC ground connection go; and the controller's analog ground plane, where sensitive analog components, the master's GND pin, and the V_{CC} bypass capacitor go. The controller's analog ground plane (GND) must meet the power ground plane (PGND) only at a single point directly beneath the IC. The power ground plane should connect to the high-power output ground with a short, thick metal trace from PGND to the source of the low-side MOSFETs (the middle of the star ground).
5) Connect the output power planes (V_{CORE} and system ground planes) directly to the output-filter-capacitor positive and negative terminals with multiple vias. Place the entire DC-DC converter circuit as close to the CPU as is practical.

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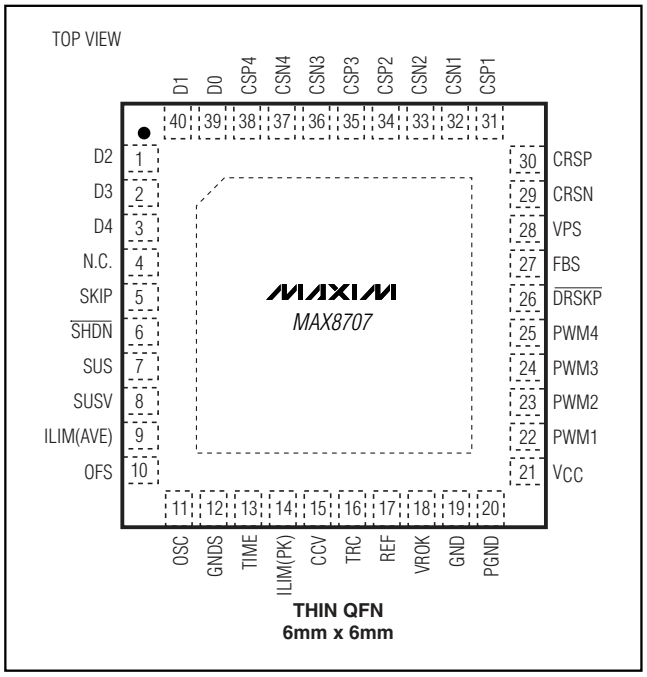
Pin Configuration



THIN QFN
6mm x 6mm

Chip Information

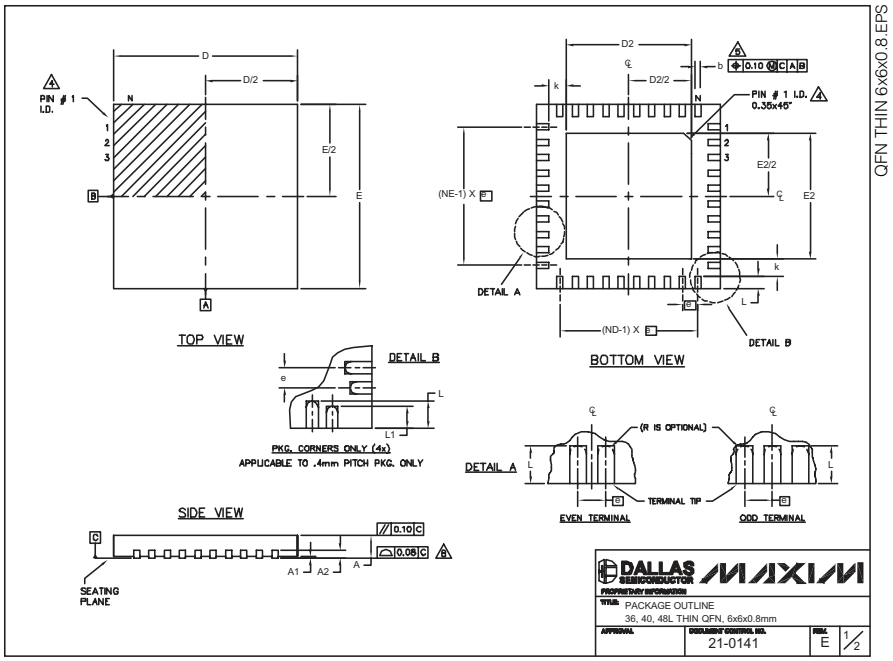
TRANSISTOR COUNT: 9011

PROCESS: BiCMOS

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

QFN THIN 6x6x0.8.EPS



COMMON DIMENSIONS									
PKG.	36L 6x6			40L 6x6			48L 6x6		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	–	0.05
A2		0.20 REF.			0.20 REF.			0.20 REF.	
b	0.20	0.25	0.30	0.20	0.25	0.30	0.15	0.20	0.25
D	5.90	6.00	6.10	5.90	6.00	6.10	5.90	6.00	6.10
E	5.90	6.00	6.10	5.90	6.00	6.10	5.90	6.00	6.10
e		0.50 BSC.			0.50 BSC.			0.40 BSC.	
k	0.25	–	–	0.25	–	–	0.25	0.35	0.45
L	0.45	0.55	0.65	0.30	0.40	0.50	0.40	0.50	0.60
L1	–	–	–	–	–	–	0.30	0.40	0.50
N		36			40			48	
ND		9			10			12	
NE		9			10			12	
JEDEC		WJJD-1			WJJD-2			–	

EXPOSED PAD VARIATIONS							DOWN BONDS ALLOWED
PKG. CODES	D2			E2			
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
T3666-1	3.60	3.70	3.80	3.60	3.70	3.80	NO
T3666-2	3.60	3.70	3.80	3.60	3.70	3.80	YES
T3666-3	3.60	3.70	3.80	3.60	3.70	3.80	NO
T4066-1	4.00	4.10	4.20	4.00	4.10	4.20	NO
T4066-2	4.00	4.10	4.20	4.00	4.10	4.20	YES
T4066-3	4.00	4.10	4.20	4.00	4.10	4.20	YES
T4066-4	4.00	4.10	4.20	4.00	4.10	4.20	NO
T4066-5	4.00	4.10	4.20	4.00	4.10	4.20	NO
T4866-1	4.20	4.30	4.40	4.20	4.30	4.40	YES

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. ⚠1 THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. ⚠2 DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. ⚠3 COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT FOR 0.4mm LEAD PITCH PACKAGE T4866-1.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE 36, 40, 48L THIN QFN, 6x6x0.8mm
APPROVAL
DOCUMENT CONTROL NO. 21-0141
REV. E
2/2