



CMOS 12-Bit Monolithic Multiplying DAC

AD7541A

T-51-09-12

1.1 Scope.

This specification covers the detail requirements for a 12-bit monolithic CMOS multiplying digital-to-analog converter. The AD7541A is a direct replacement for the industry standard AD7541, offering improved performance in the areas of latch-up, lower gain error and gain temperature coefficient.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number ¹
-1	AD7541AS(X)/883B
-2	AD7541AT(X)/883B

NOTE

¹See paragraph 1.2.3 for package identifier.

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
Q	Q-18	18-Pin Cerdip
E	E-20A	20-Contact LCC

1.3 Absolute Maximum Ratings. ($T_A = 25^\circ\text{C}$ unless otherwise noted. Pin numbers refer to DIP package.)

V_{DD} (Pin 16) to GND	+17V
V_{REF} (Pin 17) to GND	$\pm 25\text{V}$
V_{RFB} (Pin 18) to GND	$\pm 25\text{V}$
Digital Input Voltage (Pin 4–Pin 15) to GND	$-0.3\text{V}, V_{DD}$
V_{PIN1}, V_{PIN2} to GND	-0.3V to V_{DD}
Power Dissipation	
Up to $+75^\circ\text{C}$	450mW
Derates above $+75^\circ\text{C}$	6mW/ $^\circ\text{C}$
Operating Temperature Range	-55°C to $+125^\circ\text{C}$
Storage Temperature Range	-65°C to $+150^\circ\text{C}$

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 35^\circ\text{C}/\text{W}$ for Q-18 and E-20A
 $\theta_{JA} = 120^\circ\text{C}/\text{W}$ for Q-18 and E-20A

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Test	Symbol	Device	Design Limit @ +125°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Resolution	RES	-1, 2	12					Bits
Relative Accuracy	RA	-1	1	1	1			± LSB max
		-2	1/2	1	1/2	1/2		
Differential Nonlinearity	DNL	-1	1	1	1		All Grades Guaranteed Monotonic to 12 Bits, T _{min} to T _{max}	± LSB
		-2	1/2	1	1/2	1/2		
Gain Error ²	AE	-1	8	6	8			± LSB max
		-2	5	6	5	3		
Gain Tempco	TC _{AE}	-1, 2	5					± ppm/°C max
Power Supply Rejection	PSRR	-1, 2	0.02	0.01	0.02		ΔV _{DD} = ± 5%	± % per % max
Output Leakage Current Pin 1 Pin 2	I _{OUT1}	-1, 2	200	5	200		Digital Inputs = 0V Digital Inputs = V _{DD}	± nA max
	I _{OUT2}	-1, 2	200	5	200			± nA max
Output Current Settling Time		-1, 2	0.6				To ± 1/2LSB, R _{OUT1} = 100Ω, C _{OUT1} = 13pF Digital Inputs = V _{IH} to V _{IL} or V _{IL} to V _{IH}	μs typ
Feedthrough Error ³	FT	-1, 2	1				V _{REF} = ± 10V 10kHz Sinewave T _A = +25°C	mV p-p typ
Reference Input Resistance	R _{IN}	-1, 2	7	7	7			kΩ min
		-1, 2	18	18	18			kΩ max
Digital Input High Voltage	V _{IH}	-1, 2	2.4	2.4	2.4			V min
Digital Input Low Voltage	V _{IL}	-1, 2	0.8	0.8	0.8			V max
Digital Input Leakage Current	I _{IN}	-1, 2	1	1	1		V _{IN} = 0V or V _{DD}	± μA max
Digital Input Capacitance	C _{IN}	-1, 2	8					pF max
Output Capacitance Pin 1 Pin 2	C _{OUT1}	-1, 2	200				Digital Inputs = V _{IH} Digital Inputs = V _{IH}	pF max
	C _{OUT2}	-1, 2	70					pF max
Output Capacitance Pin 1 Pin 2	C _{OUT1}	-1, 2	70				Digital Inputs = V _{IL} Digital Inputs = V _{IL}	pF max
	C _{OUT2}	-1, 2	200					pF max
Supply Current from V _{DD}	I _{DD}	-1, 2	2	2	2		Digital Inputs = V _{IH} or V _{IL} Digital Inputs = 0V or V _{DD}	mA max
			500	100	500			μA max

NOTES

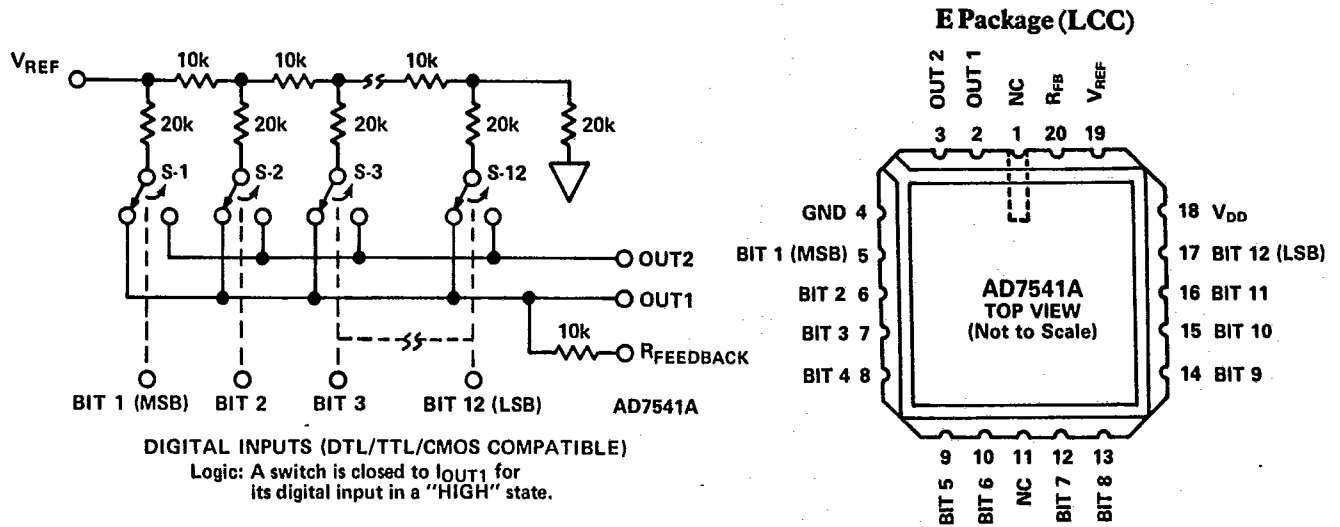
¹V_{DD} = +15V; V_{OUT1} = V_{OUT2} = 0V; V_{REF} = +10V unless otherwise stated.²Measured using internal feedback resistor and includes effect of leakage current and gain TC.³Feedthrough error can be reduced by connecting the lid of the ceramic package to ground.

Table 1.

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3.2.1 Functional Block Diagram and Terminal Assignments.



3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (80).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).

