

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceed the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-35835
 - Class Q Military
 - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
 - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

TYPES SN54H102, SN74H102 AND-GATED J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

REVISED DECEMBER 1983

- Package Options Include Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

description

These monolithic J-K flip-flops are negative-edge-triggered. They feature gated J-K inputs and an asynchronous clear input. The AND gate inputs are inhibited while the clock input is low; when the clock goes high, the inputs are enabled and data will be accepted. Logical state of J and K inputs may be allowed to change when the clock pulse is in a high state and bistable will perform according to the truth table as long as minimum set-up times are observed. Input data is transferred to the outputs on the negative edge of the clock pulse.

The SN54H102 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74H102 is characterized for operation from 0°C to 70°C .

FUNCTION TABLE

INPUTS					OUTPUTS	
PRE	CLR	CLK	J	K	Q	\bar{Q}
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H†	H†
H	H	↓	L	L	Q_0	\bar{Q}_0
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	TOGGLE
H	H	H	X	X	Q_0	\bar{Q}_0

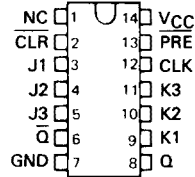
† This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

positive logic

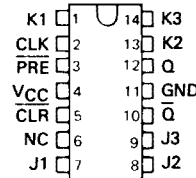
$$J = J1 \cdot J2 \cdot J3$$

$$K = K1 \cdot K2 \cdot K3$$

SN54H102 ... J PACKAGE
SN74H102 ... J OR N PACKAGE
(TOP VIEW)

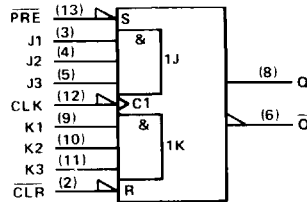


SN54H102 ... W PACKAGE
(TOP VIEW)



NC - No internal connection

logic symbol



Pin numbers shown are for J and N packages.

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TTL DEVICES

PRODUCTION DATA

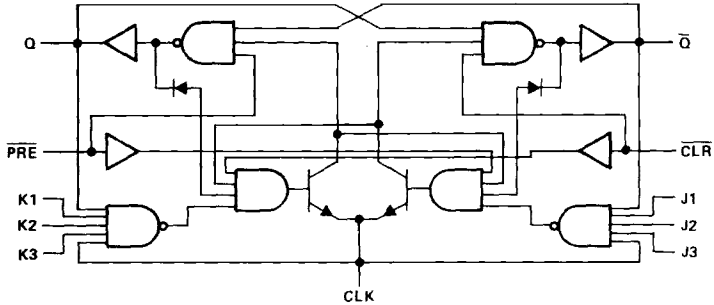
This document contains information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



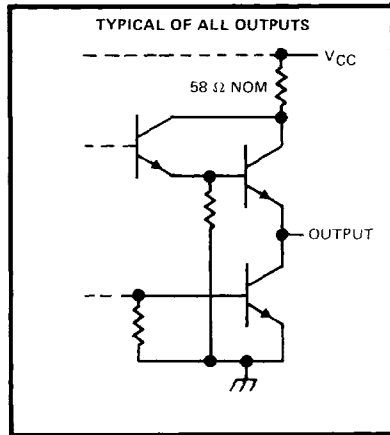
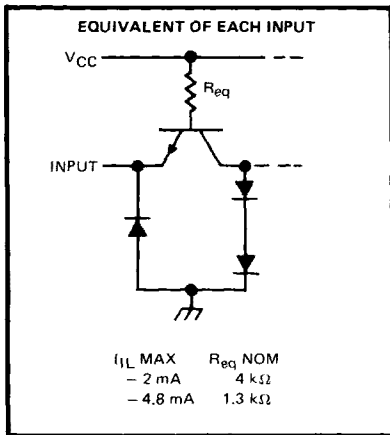
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TYPES SN54H102, SN74H102
AND-GATED J-K NEGATIVE-EDGE-TRIGGERED
FLIP-FLOPS WITH PRESET AND CLEAR

logic diagram



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Operating free-air temperature range: SN54H'	-55°C to 125°C
SN74H'	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

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TYPES SN54H102, SN74H102 AND-GATED J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

recommended operating conditions

		SN54H102			SN74H102			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage				0.8			V
I_{OH}	High-level output current				-0.5			mA
I_{OL}	Low-level output current				20			mA
t_w	Pulse duration	CLK high	10		10			ns
		CLK low	15		15			
		CLR or PRE low	16		16			
t_{su}	Setup time before CLK ↓	High-level data	10		10			ns
		Low-level data	13		13			
t_h	Hold time-data after CLK ↓	0		0			ns	
T_A	Operating free-air temperature	-55	125		0	70		°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54H102			SN74H102			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		$V_{CC} = \text{MIN.}$	$I_I = -8 \text{ mA}$		-1.5			-1.5		V
V_{OH}		$V_{CC} = \text{MIN.}$	$V_{IH} = 2 \text{ V.}$	$V_{IL} = 0.8 \text{ V.}$	2.4	3.4	2.4	3.4		V
V_{OL}		$V_{CC} = \text{MIN.}$	$V_{IH} = 2 \text{ V.}$	$V_{IL} = 0.8 \text{ V.}$	0.2	0.4	0.2	0.4		V
I_I		$V_{CC} = \text{MAX.}$	$V_I = 5.5 \text{ V}$		1			1		mA
I_{IH}	Any J or K	$V_{CC} = \text{MAX.}$	$V_I = 2.4 \text{ V}$	50			50			μA
	CLR			100			100			
	PRE			100			100			
	CLK			0	-1	0	-1	mA		
I_{IL}	Any J or K	$V_{CC} = \text{MAX.}$	$V_I = 0.4 \text{ V}$	-1			-1			mA
	CLR			-1			-1			
	PRE			-1			-1			
	CLK			-3	-4.8	-3	-4.8			
$I_{OS}§$		$V_{CC} = \text{MAX.}$			-40	-100	-40	-100	mA	
I_{CC}		$V_{CC} = \text{MAX.}$	See Note 2		20	38	20	38	mA	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V.}$ $T_A = 25^\circ\text{C.}$

§ Not more than one output should be shorted at a time, and duration of short-circuit should not exceed one second.

NOTE 2: With all outputs open, I_{CC} is measured with the Q and \bar{Q} outputs high in turn. At the time of measurement, the clock input is grounded.

switching characteristics, $V_{CC} = 5 \text{ V, } T_A = 25^\circ\text{C}$ (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}				$R_L = 280 \Omega,$ $C_L = 25 \text{ pF}$	40	50	
t_{PLH}	PRE or CLR	Q or \bar{Q}	8		12		ns
t_{PHL}	PRE or CLR (CLK high)	\bar{Q} or Q	15		20		ns
	PRE or CLR (CLK low)		23		35		
t_{PLH}	CLK	Q or \bar{Q}	10		15		ns
t_{PHL}			16		20		

NOTE 3: See General Information Section for load circuits and voltage waveforms.