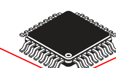
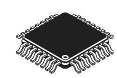
The MPC961 is a 2.5 V or 3.3 V compatible, 1:18 PLL based zero delay buffer. With output frequencies of up to 200 MHz, output skews of 150 ps the device meets the needs of the most demanding clock tree applications.

MPC961P

LOW VOLTAGE ZERO DELAY BUFFER



~~FA SUFFIX~~
~~32-LEAD LQFP PACKAGE~~
~~CASE 873A-03~~



AC SUFFIX
32-LEAD LQFP PACKAGE
Pb-FREE PACKAGE
CASE 873A-03

Features

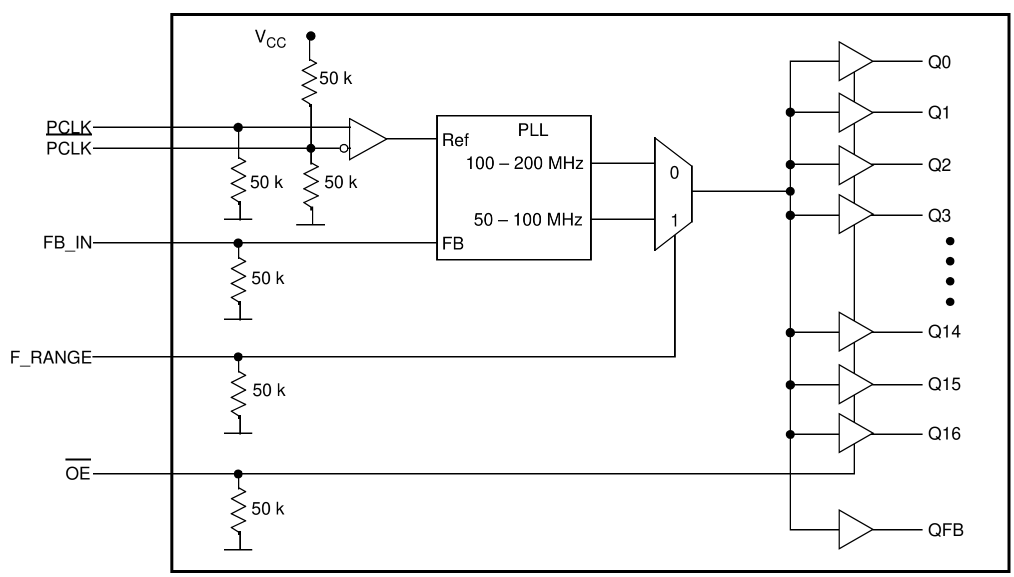
- Fully Integrated PLL
- Up to 200 MHz I/O Frequency
- LVCMOS Outputs
- Outputs Disable in High Impedance
- LVPECL Reference Clock Options
- LQFP Packaging
- 32-lead Pb-free Package Available
- ±50 ps Cycle-Cycle Jitter
- 150 ps Output Skews

Functional Description

The MPC961 is offered with two different input configurations. The MPC961P offers an LVCMOS reference clock while the MPC961P offers an LVPECL reference clock.

When pulled high the $\overline{OE}$ pin will force all of the outputs (except QFB) into a high impedance state. Because the $\overline{OE}$ pin does not affect the QFB output, down stream clocks can be disabled without the internal PLL losing lock.

The MPC961 is fully 2.5 V or 3.3 V compatible and requires no external loop filter components. All control inputs accept LVCMOS compatible levels and the outputs provide low impedance LVCMOS outputs capable of driving terminated 50 Ω transmission lines. For series terminated lines the MPC961 can drive two lines per output giving the device an effective fanout of 1:36. The device is packaged in a 32 lead LQFP package to provide the optimum combination of board density and performance.



The MPC961P requires an external RC filter for the analog power supply pin V_{CCA}. Refer to APPLICATIONS INFORMATION for details.

Figure 1. MPC961P Logic Diagram

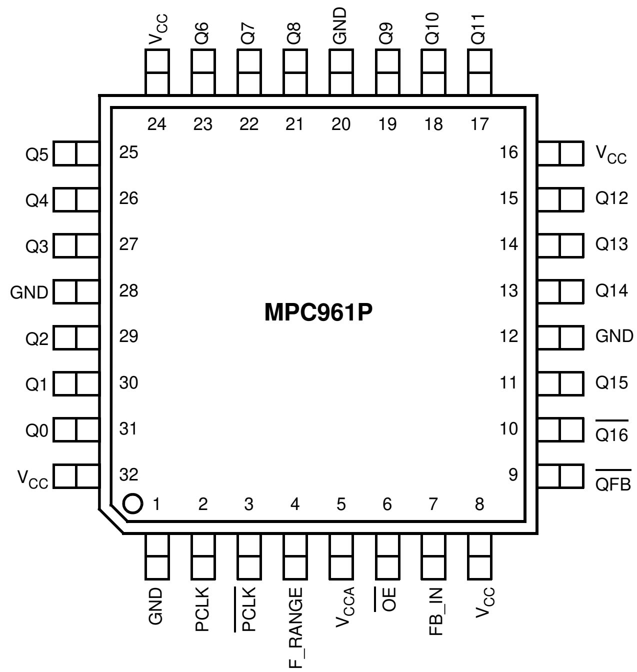


Figure 2. 32-Lead Pinout (Top View)

Table 1. Pin Configurations

Number	Name	Type	Description
PCLK, $\overline{\text{PCLK}}$	Input	LVCMOS	PLL reference clock signal
FB_IN	Input	LVCMOS	PLL feedback signal input, connect to a QFB output
F_RANGE	Input	LVCMOS	PLL frequency range select
$\overline{\text{OE}}$	Input	LVCMOS	Output enable/disable
Q0 – Q16	Output	LVCMOS	Clock outputs
QFB	Output	LVCMOS	PLL feedback signal output, connect to a FB_IN
GND	Supply	Ground	Negative power supply
V_{CCA}	Supply	V_{CC}	PLL positive power supply (analog power supply). The MPC961P requires an external RC filter for the analog power supply pin V_{CCA}. Please see applications section for details.
V_{CC}	Supply	V_{CC}	Positive power supply for I/O and core

Table 2. Function Table

Control	Default	0	1
F_RANGE	0	PLL high frequency range. MPC961P input reference and output clock frequency range is 100 – 200 MHz	PLL low frequency range. MPC961P input reference and output clock frequency range is 50 – 100 MHz
OE	0	Outputs enabled	Outputs disabled (high-impedance state)

Table 3. Absolute Maximum Ratings[1]

Symbol	Characteristics	Min	Max	Unit	Condition
V_{CC}	Supply Voltage	–0.3	3.6	V	
V_{IN}	DC Input Voltage	–0.3	V_{CC} + 0.3	V	
V_{OUT}	DC Output Voltage	–0.3	V_{CC} + 0.3	V	
I_{IN}	DC Input Current		±20	mA	
I_{OUT}	DC Output Current		±50	mA	
T_S	Storage Temperature	–40	125	°C	

1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

Table 4. DC Characteristics (V_{CC} = 3.3 V ± 5%, T_A = –40° to 85°C)

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
V_{IH}	Input HIGH Voltage		2.0		V_{CC} + 0.3	V	LVCMOS
V_{IL}	Input LOW Voltage		–0.3		0.8	V	LVCMOS
V_{PP}	Peak-to-peak input voltage[1]	PECL_CLK, $\overline{PECL\_CLK}$	500		1000	mV	LVPECL
V_{CMR}	Common Mode Range[2]	PECL_CLK, $\overline{PECL\_CLK}$	1.2		V_{CC} – 0.8	V	LVPECL
V_{OH}	Output HIGH Voltage		2.4			V	I_{OH} = –20 mA[2]
V_{OL}	Output LOW Voltage				0.55	V	I_{OL} = 20 mA[2]
Z_{OUT}	Output Impedance			14	20	Ω	
I_{IN}	Input Current				±120	μA	
C_{IN}	Input Capacitance			4.0		pF	
C_{PD}	Power Dissipation Capacitance			8.0	10	pF	Per Output
I_{CCA}	Maximum PLL Supply Current			2.0	5.0	mA	V_{CCA} Pin
I_{CC}	Maximum Quiescent Supply Current					mA	All V_{CC} Pins
V_{TT}	Output Termination Voltage			V_{CC} ÷ 2		V	

1. Exceeding the specified V_{CMR}/V_{PP} window results in a t_{PD} changes of approximately 250 ps.
2. The MPC961P is capable of driving 50 Ω transmission lines on the incident edge. Each output drives one 50 Ω parallel terminated transmission line to a termination voltage of V_{TT}. Alternatively, the device drives up two 50 Ω series terminated transmission lines.

Table 5. AC Characteristics (V_{CC} = 3.3 V ± 5%, T_A = –40° to 85°C)[1]

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
f_{REF}	Input Frequency	F_RANGE = 0 F_RANGE = 1	100 50		200 100	MHz	
f_{MAX}	Maximum Output Frequency	F_RANGE = 0 F_RANGE = 1	100 50		200 100	MHz	
f_{REFDC}	Reference Input Duty Cycle		25		75	%	
$t_{(\varnothing)}$	Propagation Delay[2] (static phase offset)	PECL_CLK to FB_IN	–80		120	ps	PLL locked
$t_{sk(O)}$	Output-to-Output Skew[3]			90	150	ps	
DC_O	Output Duty Cycle	F_RANGE = 0 F_RANGE = 1	40 45	50 50	60 55	%	
t_r, t_f	Output Rise/Fall Time		0.1		1.0	ns	0.6 to 1.8 V
$t_{PLZ,HZ}$	Output Disable Time				10	ns	
$t_{PZL,LZ}$	Output Enable Time				10	ns	
$t_{JIT(CC)}$	Cycle-to-Cycle Jitter	RMS (1σ)[4]			15	ps	
$t_{JIT(PER)}$	Period Jitter	RMS (1σ)		7.0	10	ps	
$t_{JIT(\varnothing)}$	I/O Phase Jitter	RMS (1σ) F_RANGE = 0 F_RANGE = 1			0.0015 · T 0.0010 · T		T = Clock Signal Period
t_{lock}	Maximum PLL Lock Time				10	ms	

1. AC characteristics apply for parallel output termination of 50 Ω to V_{TT}.
2. t_{PD} applies for V_{CMR} = V_{CC} –1.3 V and V_{PP} = 800 mV.
3. Refer to APPLICATIONS INFORMATION for part-to-part skew calculation.
4. Refer to APPLICATIONS INFORMATION for calculation for other confidence factors than 1σ.

Table 6. DC Characteristics (V_{CC} = 2.5 V ± 5%, T_A = –40° to 85°C)

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
V_{IH}	Input HIGH Voltage		1.7		V_{CC} + 0.3	V	LVCMOS
V_{IL}	Input LOW Voltage		–0.3		0.7	V	LVCMOS
V_{PP}	Peak-to-peak input voltage[1]	PECL_CLK, $\overline{\text{PECL\_CLK}}$	500		1000	mV	LVPECL
V_{CMR}	Common Mode Range[1]	PECL_CLK, $\overline{\text{PECL\_CLK}}$	1.2		V_{CC} – 0.7	V	LVPECL
V_{OH}	Output HIGH Voltage		1.8			V	I_{OH} = –15 mA[2]
V_{OL}	Output LOW Voltage				0.6	V	I_{OL} = 15 mA[2]
Z_{OUT}	Output Impedance			18	26	Ω	
I_{IN}	Input Current				±120	μA	
C_{IN}	Input Capacitance			4.0		pF	
C_{PD}	Power Dissipation Capacitance			8.0	10	pF	Per Output
I_{CCA}	Maximum PLL Supply Current			2.0	5.0	mA	V_{CCA} Pin
I_{CC}	Maximum Quiescent Supply Current					mA	All V_{CC} Pins
V_{TT}	Output Termination Voltage			V_{CC} ÷ 2		V	

1. Exceeding the specified V_{CMR}/V_{PP} window results in a t_{PD} changes < 250 ps.
2. The MPC961P is capable of driving 50 Ω transmission lines on the incident edge. Each output drives one 50 Ω parallel terminated transmission line to a termination voltage of V_{TT}. Alternatively, the device drives up two 50 Ω series terminated transmission lines.

Table 7. AC Characteristics (V_{CC} = 2.5 V ± 5%, T_A = –40° to 85°C)[1]

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
f_{REF}	Input Frequency	F_RANGE = 0 F_RANGE = 1	100 50		200 100	MHz	
f_{MAX}	Maximum Output Frequency	F_RANGE = 0 F_RANGE = 1	100 50		200 100	MHz	
f_{REFDC}	Reference Input Duty Cycle		25		75	%	
$t_{(\varnothing)}$	Propagation Delay[2] (static phase offset)	CCLK to FB_IN	–50		175	ps	PLL locked
$t_{sk(O)}$	Output-to-Output Skew[3]			90	150	ps	
DC_O	Output Duty Cycle	F_RANGE = 0 F_RANGE = 1	40 45	50 50	60 55	%	
t_r, t_f	Output Rise/Fall Time		0.1		1.0	ns	0.6 to 1.8 V
$t_{PLZ,HZ}$	Output Disable Time				10	ns	
$t_{PZL,LZ}$	Output Enable Time				10	ns	
$t_{JIT(CC)}$	Cycle-to-Cycle Jitter	RMS (1σ)[4]			15	ps	
$t_{JIT(PER)}$	Period Jitter	RMS (1σ)		7.0	10	ps	
$t_{JIT(\varnothing)}$	I/O Phase Jitter	RMS (1σ) F_RANGE = 0 F_RANGE = 1			0.0015 · T 0.0010 · T		T = Clock Signal Period
t_{lock}	Maximum PLL Lock Time				10	ms	

1. AC characteristics apply for parallel output termination of 50 Ω to V_{TT}.
2. t_{PD} applies for $V_{CMR} = V_{CC}$ –1.3 V and V_{PP} = 800 mV.
3. Refer to APPLICATIONS INFORMATION for part-to-part skew calculation.
4. Refer to APPLICATIONS INFORMATION for calculation for other confidence factors than 1σ.

APPLICATIONS INFORMATION

Power Supply Filtering

The MPC961P is a mixed analog/digital product and as such it exhibits some sensitivities that would not necessarily be seen on a fully digital product. Analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. The MPC961P provides separate power supplies for the output buffers (V_{CC}) and the phase-locked loop (V_{CCA}) of the device. The purpose of this design technique is to isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a controlled environment such as an evaluation board this level of isolation is sufficient. However, in a digital system environment where it is more difficult to minimize noise on the power supplies, a second level of isolation may be required. The simplest form of isolation is a power supply filter on the V_{CCA} pin for the MPC961P.

Figure 3 illustrates a typical power supply filter scheme. The MPC961P is most susceptible to noise with spectral content in the 10 kHz to 5 MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop that will be seen between the V_{CC} supply and the V_{CCA} pin of the MPC961P. From the data sheet the I_{CCA} current (the current sourced through the V_{CCA} pin) is typically 2 mA (5 mA maximum), assuming that a minimum of 2.375 V (V_{CC} = 3.3 V or V_{CC} = 2.5 V) must be maintained on the V_{CCA} pin. The resistor R_F shown in Figure 3 must have a resistance of 270 Ω (V_{CC} = 3.3 V) or 5 to 15 Ω (V_{CC} = 2.5 V) to meet the voltage drop criteria. The RC filter pictured will provide a broadband filter with approximately 100:1 attenuation for noise whose spectral content is above 20 kHz. As the noise frequency crosses the series resonant point of an individual capacitor it's overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL.

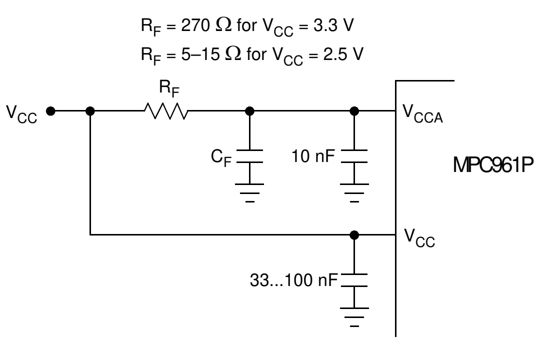


Figure 3. Power Supply Filter

Although the MPC961P has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

Driving Transmission Lines

The MPC961P clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 15 Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to application note AN1091.

In most high performance clock networks point-to-point distribution of signals is the method of choice. In a point-to-point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50 Ω resistance to $V_{CC/}2$. This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC961P clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 4 illustrates an output driving a single series terminated line vs two series terminated lines in parallel. When taken to its extreme the fanout of the MPC961P clock driver is effectively doubled due to its capability to drive multiple lines.

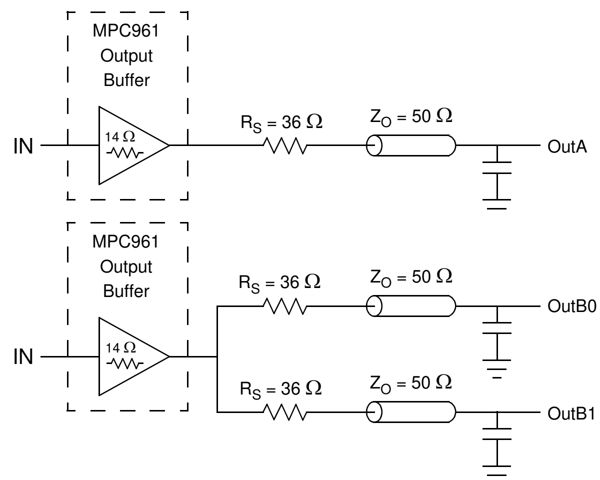


Figure 4. Single versus Dual Transmission Lines

The waveform plots of Figure 5 show the simulation results of an output driving a single line vs two lines. In both cases the drive capability of the MPC961P output buffer is more than sufficient to drive 50 Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43 ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the MPC961P. The output waveform in Figure 5 shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 36 Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$V_L = V_S\,(Z_O / (R_S + R_O + Z_O))$$
$$Z_O = 50\ \Omega\ ||\ 50\ \Omega$$
$$R_S = 36\ \Omega\ ||\ 36\ \Omega$$
$$R_O = 14\ \Omega$$
$$V_L = 3.0\ (25 / (18 + 14 + 25) = 3.0\ (25 / 57)$$
$$= 1.31\ V$$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.62 V. It will then increment towards the quiescent 3.0 V in steps separated by one round trip delay (in this case 4.0 ns).

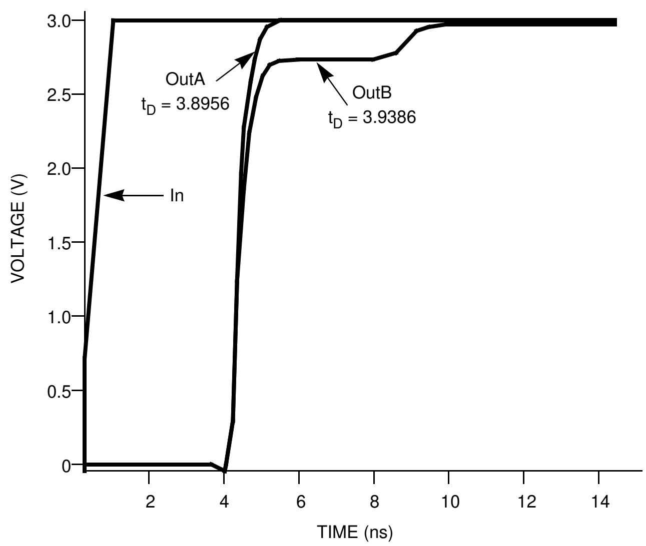
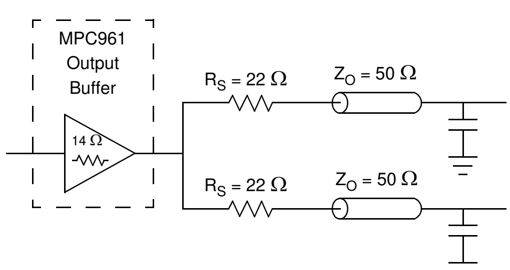


Figure 5. Single versus Dual Waveforms

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 6 should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.



$$14\ \Omega + 22\ \Omega\ ||\ 22\ \Omega = 50\ \Omega\ ||\ 50\ \Omega$$
$$25\ \Omega = 25\ \Omega$$

Figure 6. Optimized Dual Line Termination

SPICE level and IBIS output buffer models are available for engineers who want to simulate their specific interconnect schemes.

Using the MPC961P in Zero-Delay Applications

Nested clock trees are typical applications for the MPC961P. Designs using the MPC961P as LVCMOS PLL fanout buffer with zero insertion delay will show significantly lower clock skew than clock distributions developed from CMOS fanout buffers. The external feedback option of the MPC961P clock driver allows for its use as a zero delay buffer. By using the QFB output as a feedback to the PLL the propagation delay through the device is virtually eliminated. The PLL aligns the feedback clock output edge with the clock input reference edge resulting a near zero delay through the device. The maximum insertion delay of the device in zero-delay applications is measured between the reference clock input and any output. This effective delay consists of the static phase offset, I/O jitter (phase or long-term jitter), feedback path delay and the output-to-output skew error relative to the feedback output.

Calculation of Part-to-Part Skew

The MPC961P zero delay buffer supports applications where critical clock signal timing can be maintained across several devices. If the reference clock inputs of two or more MPC961P are connected together, the maximum overall timing uncertainty from the common PCLK input to any output is:

$$t_{SK(PP)} = t_{(\varnothing)} + t_{SK(O)} + t_{PD,\ LINE(FB)} + t_{JIT(\varnothing)} \cdot CF$$

This maximum timing uncertainty consist of 4 components: static phase offset, output skew, feedback board trace delay and I/O (phase) jitter:

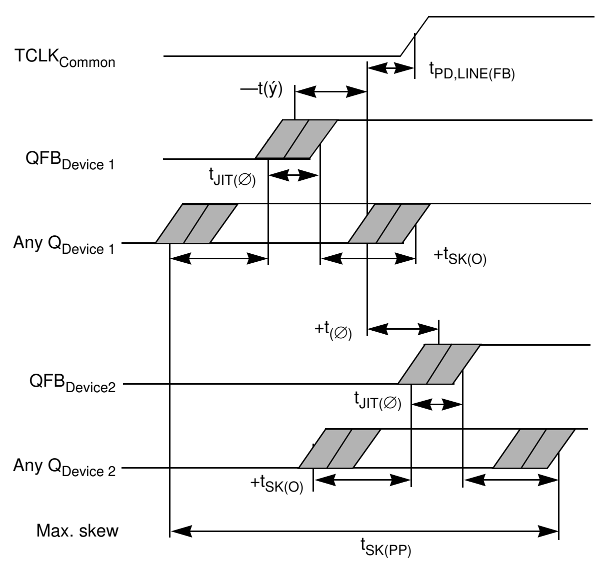


Figure 7. MPC961P Max. Device-to-Device Skew

Due statistical nature of I/O jitter a rms value (1σ) is specified. I/O jitter numbers for other confidence factors (CF) can be derived from Table 8.

Table 8. Confidence Factor CF

CF	Probability of clock edge within the distribution
$\pm 1\sigma$	0.68268948
$\pm 2\sigma$	0.95449988
$\pm 3\sigma$	0.99730007
$\pm 4\sigma$	0.99993663
$\pm 5\sigma$	0.99999943
$\pm 6\sigma$	0.99999999

The feedback trace delay is determined by the board layout and can be used to fine-tune the effective delay through each device. In the following example calculation a I/O jitter confidence factor of 99.7% ($\pm 3\sigma$) is assumed, resulting in a worst case timing uncertainty from input to any output of –236 ps to 361 ps relative to PCLK (f = 125 MHz, V_{CC} = 2.5 V):

$t_{SK(PP)}$ = [-50 ps...175ps] + [-150 ps...150 ps] + [(12ps @ -3)...(12ps @ 3)] + $t_{PD,\ LINE(FB)}$

$t_{SK(PP)}$ = [-236ps...361ps] + $t_{PD,\ LINE(FB)}$

Due to the frequency dependence of the I/O jitter, Figure 8 "Max. I/O Jitter versus frequency" can be used for a more precise timing performance analysis.

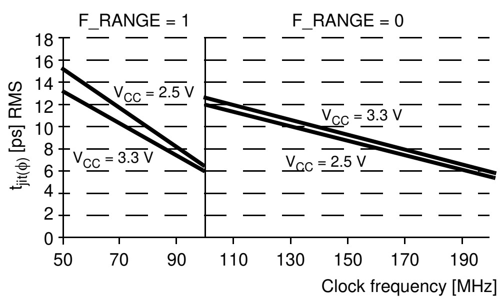


Figure 8. Max. I/O Jitter versus Frequency

Power Consumption of the MPC961P and Thermal Management

The MPC961P AC specification is guaranteed for the entire operating frequency range up to 200 MHz. The MPC961P power consumption and the associated long-term reliability may decrease the maximum frequency limit, depending on operating conditions such as clock frequency, supply voltage, output loading, ambient temperature, vertical convection and thermal conductivity of package and board. This section describes the impact of these parameters on the junction temperature and gives a guideline to estimate the MPC961P die junction temperature and the associated device reliability. For a complete analysis of power consumption as a function of operating conditions and associated long term device reliability refer to the Application Note AN1545. According the AN1545, the long-term device reliability is a function of the die junction temperature:

Table 9. Die Junction Temperature and MTBF

Junction temperature (°C)	MTBF (Years)
100	20.4
110	9.1
120	4.2
130	2.0

Increased power consumption will increase the die junction temperature and impact the device reliability (MTBF). According to the system-defined tolerable MTBF, the die junction temperature of the MPC961P needs to be controlled and the thermal impedance of the board/package should be optimized. The power dissipated in the MPC961P is represented in equation 1.

Where I_{CCQ} is the static current consumption of the MPC961P, C_{PD} is the power dissipation capacitance per output, $(M)\Sigma C_L$ represents the external capacitive output load, N is the number of active outputs (N is always 27 in case of the MPC961P). The MPC961P supports driving transmission lines to maintain high signal integrity and tight timing parameters. Any transmission line will hide the lumped capacitive load at the end of the board trace, therefore, ΣC_L is zero for controlled transmission line systems and can be eliminated from equation 1. Using parallel termination output termination results in equation 2 for power dissipation.

In equation 2, P stands for the number of outputs with a parallel or thevenin termination, V_{OL}, I_{OL}, V_{OH}, and I_{OH} are a function of the output termination technique and DC_Q is the clock signal duty cycle. If transmission lines are used ΣC_L is zero in equation 2 and can be eliminated. In general, the use of controlled transmission line techniques eliminates the impact of the lumped capacitive loads at the end lines and greatly reduces the power dissipation of the device. Equation 3 describes the die junction temperature T_J as a function of the power consumption.

$$P_{TOT} = \left[I_{CCQ} + V_{CC} \cdot f_{CLOCK} \cdot \left(N \cdot C_{PD} + \sum_M C_L \right) \right] \cdot V_{CC} \qquad \text{Equation 1}$$

$$P_{TOT} = V_{CC} \cdot \left[I_{CCQ} + V_{CC} \cdot f_{CLOCK} \cdot \left(N \cdot C_{PD} + \sum_M C_L \right) \right] + \sum_P \left[DC_Q \cdot I_{OH} \cdot (V_{CC} - V_{OH}) + (1 - DC_Q) \cdot I_{OL} \cdot V_{OL} \right] \qquad \text{Equation 2}$$

$$T_J = T_A + P_{TOT} \cdot R_{thja} \qquad \text{Equation 3}$$

$$f_{CLOCK,MAX} = \frac{1}{C_{PD} \cdot N \cdot V^2_{CC}} \cdot \left[\frac{T_{j,MAX} - T_A}{R_{thja}} - (I_{CCQ} \cdot V_{CC}) \right] \qquad \text{Equation 4}$$

Where R_{thja} is the thermal impedance of the package (junction to ambient) and T_A is the ambient temperature. According to Table 9, the junction temperature can be used to estimate the long-term device reliability. Further, combining equation 1 and equation 2 results in a maximum operating frequency for the MPC961P in a series terminated transmission line system.

Table 10. Thermal Package Impedance of the 32ld LQFP

Convection, LFPM	R_{thja} (1P2S board), K/W
Still air	80
100 lfpm	70
200 lfpm	61
300 lfpm	57
400 lfpm	56
500 lfpm	55

$T_{J,MAX}$ should be selected according to the MTBF system requirements and Table 9. R_{thja} can be derived from Table 10. The R_{thja} represent data based on 1S2P boards, using 2S2P boards will result in a lower thermal impedance than indicated below.

If the calculated maximum frequency is below 200 MHz, it becomes the upper clock speed limit for the given application conditions. The following two derating charts describe the safe frequency operation range for the MPC961P. The charts were calculated for a maximum tolerable die junction temperature of 110°C, corresponding to an estimated MTBF of 9.1 years, a supply voltage of 3.3 V and series terminated transmission line or capacitive loading. Depending on a given set of these operating conditions and the available device convection a decision on the maximum operating frequency can be made. There are no operating frequency limitations if a 2.5 V power supply or the system specifications allow for a MTBF of 4 years (corresponding to a max. junction temperature of 120°C.

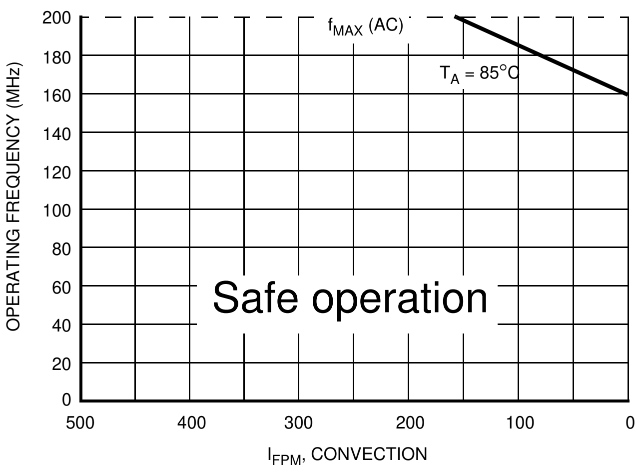


Figure 9. Maximum MPC961P Frequency, V_{CC} = 3.3 V, MTBF 9.1 Years, Driving Series Terminated Transmission Lines

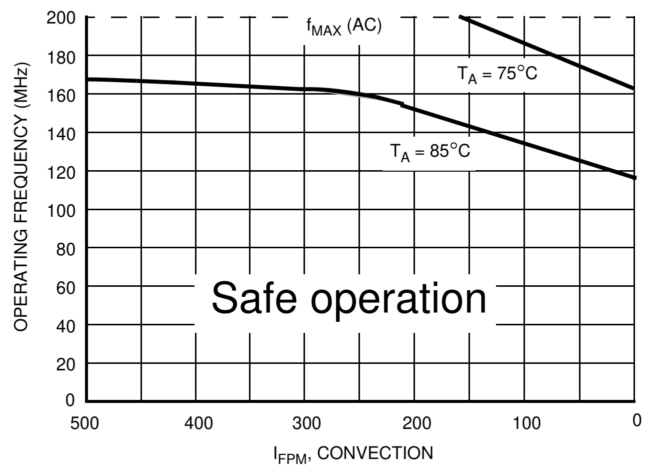


Figure 10. Maximum MPC961P Frequency, V_{CC} = 3.3 V, MTBF 9.1 Years, 4 pF Load per Line

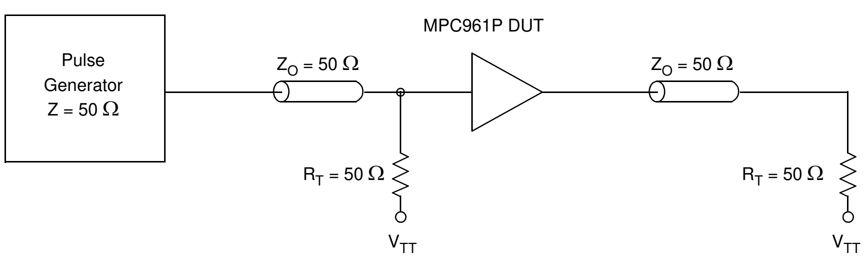


Figure 11. TCLK MPC961P AC Test Reference for V_{CC} = 3.3 V and V_{CC} = 2.5 V

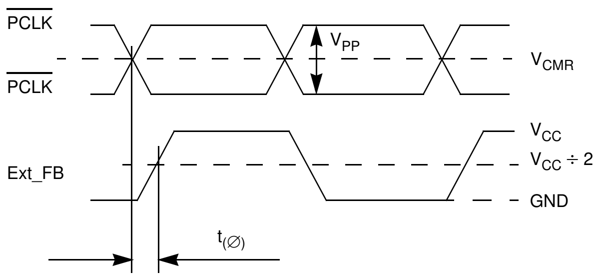


Figure 12. Propagation Delay ($t_{\varnothing}$, static phase offset) Test Reference

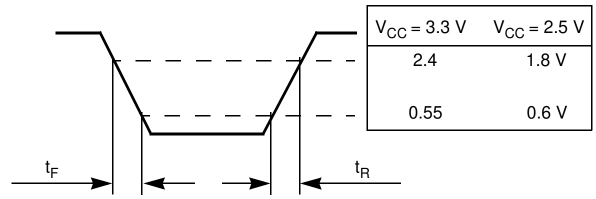
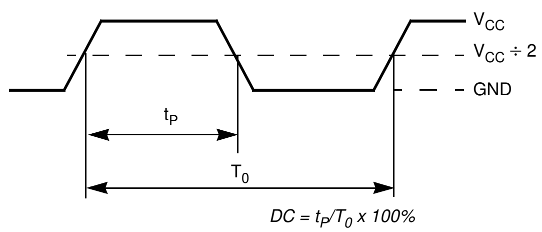
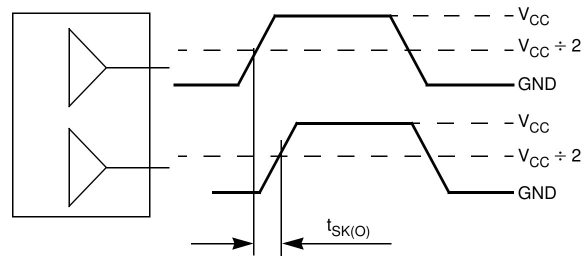


Figure 13. Output Transition Time Test Reference



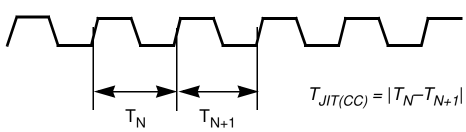
The time from the PLL controlled edge to the non controlled edge, divided by the time between PLL controlled edges, expressed as a percentage

Figure 14. Output Duty Cycle (DC)



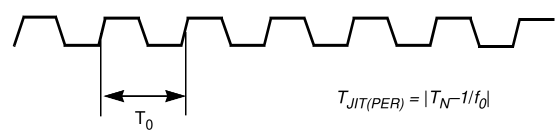
The pin-to-pin skew is defined as the worst case difference in propagation delay between any similar delay path within a single device

Figure 15. Output-to-Output Skew $t_{SK(O)}$



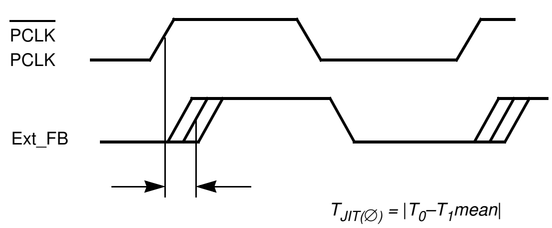
The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs

Figure 16. Cycle-to-Cycle Jitter



The deviation in cycle time of a signal with respect to the ideal period over a random sample of cycles

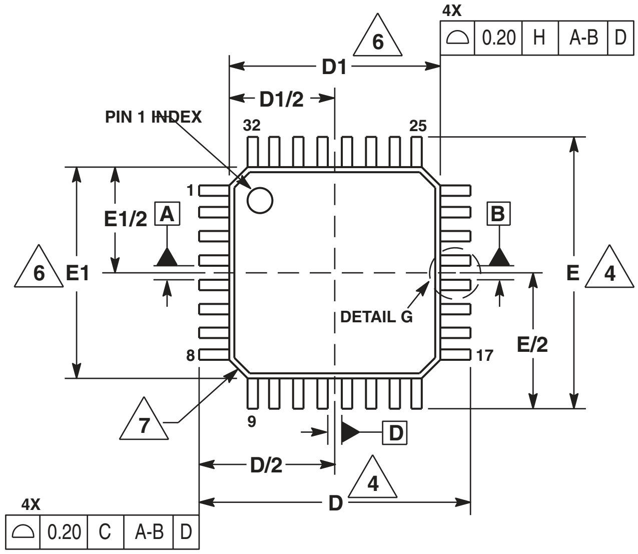
Figure 17. Period Jitter

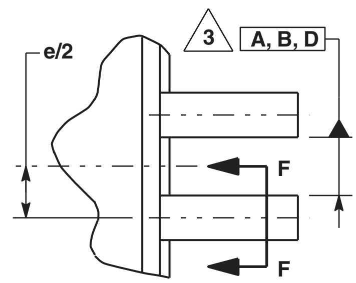


The deviation in t_0 for a controlled edge with respect to a T_0 mean in a random sample of cycles

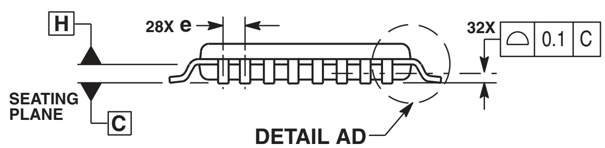
Figure 18. I/O Jitter

PACKAGE DIMENSIONS

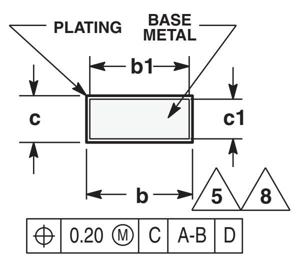




DETAIL G

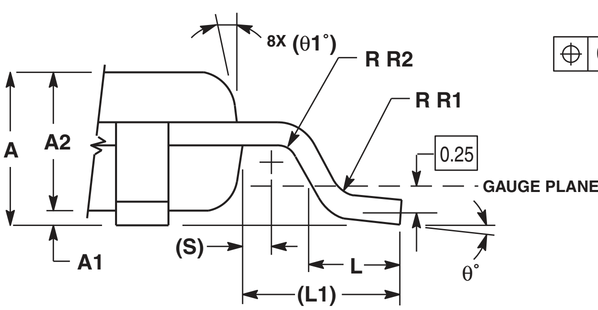


NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DATUMS A, B, AND D TO BE DETERMINED AT DATUM PLANE H.
4. DIMENSIONS D AND E TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08-mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION: 0.07-mm.
6. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25-mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1-mm AND 0.25-mm FROM THE LEAD TIP.



SECTION F-F

DIM	MILLIMETERS	
	MIN	MAX
A	1.40	1.60
A1	0.05	0.15
A2	1.35	1.45
b	0.30	0.45
b1	0.30	0.40
c	0.09	0.20
c1	0.09	0.16
D	9.00 BSC	
D1	7.00 BSC	
e	0.80 BSC	
E	9.00 BSC	
E1	7.00 BSC	
L	0.50	0.70
L1	1.00 REF	
q	0°	7°
q1	12 REF	
R1	0.08	0.20
R2	0.08	---
S	0.20 REF	



DETAIL AD

CASE 873A-03
ISSUE B
32-LEAD LQFP PACKAGE

Revision History Sheet

Rev	Table	Page	Description of Change	Date
5		1	NRND – Not Recommend for New Designs.	1/8/13
5		1	Product Discontinuation Notice - PDN CQ-15-02.	5/6/15
6		1	Obsolete per Product Discontinuation Notice - PDN CQ-15-02.	10/4/16

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