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Continuity of document content

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Continuity of ordering part numbers

Infineon continues to support existing part numbers. Please continue to use the ordering part numbers listed in the datasheet for ordering.

S29JL032J

32-Mb (4M × 8-Bit/2M × 16-Bit), 3 V, Simultaneous Read/Write Flash

Distinctive Characteristics

Architectural Advantages

- Simultaneous Read/Write operations
  - Data can be continuously read from one bank while executing erase/program functions in another bank.
  - Zero latency between read and write operations
- Multiple bank architecture
  - Four bank architectures available (see Table 2 on page 15).
- Boot sectors
  - Top or bottom boot sector configurations available
  - Any combination of sectors can be erased
- Manufactured on 0.11 µm Process Technology
- Secured Silicon Region: **Extra 256 byte sector**
  - Factory locked and identifiable: 16 bytes available for secure, random factory Electronic Serial Number; verifiable as factory locked through autoselect function
  - *Customer lockable:* One-time programmable only. Once locked, data cannot be changed
- Zero power operation
  - Sophisticated power management circuits reduce power consumed during inactive periods to nearly zero.
- Compatible with JEDEC standards
  - Pinout and software compatible with single-power-supply flash standard

Package Options

- 48-ball Fine-pitch BGA
- 48-pin TSOP

Performance Characteristics

- High performance
  - Access time as fast as 60 ns
  - Program time: 6 µs/word typical using accelerated programming function
- Ultra low power consumption (typical values)
  - 2 mA active read current at 1 MHz
  - 10 mA active read current at 5 MHz
  - 200 nA in standby or automatic sleep mode
- Cycling endurance: 100K cycles per sector
- Data retention: 20 years typical

Software Features

- Supports Common Flash Memory Interface (CFI)
- Erase suspend/Erase resume
  - Suspends erase operations to read data from, or program data to, a sector that is not being erased, then resumes the erase operation.
- Data# polling and toggle bits
  - Provides a software method of detecting the status of program or erase operations
- Unlock bypass program command
  - Reduces overall programming time when issuing multiple program command sequences

Hardware Features

- Ready/Busy# output (RY/BY#)
  - Hardware method for detecting program or erase cycle completion
- Hardware reset pin (RESET#)
  - Hardware method of resetting the internal state machine to the read mode
- WP#/ACC input pin
  - Write protect (WP#) function protects the two outermost boot sectors regardless of sector protect status
  - Acceleration (ACC) function accelerates program timing
- Sector protection
  - Hardware method to prevent any program or erase operation within a sector
  - Temporary Sector Unprotect allows changing data in protected sectors in-system

General Description

The S29JL032J is a 32 Mb, 3.0 volt-only flash memory device, organized as 2,097,152 words of 16 bits each or 4,194,304 bytes of 8 bits each. Word mode data appears on DQ15–DQ0; byte mode data appears on DQ7–DQ0. The device is designed to be programmed in-system with the standard 3.0 volt V_{CC} supply, and can also be programmed in standard EPROM programmers. The device is available with an access time of 60, or 70 ns and is offered in a 48-ball FBGA or a 48-pin TSOP package. Standard control pins—chip enable (CE#), write enable (WE#), and output enable (OE#)—control normal read and write operations, and avoid bus contention issues. The device requires only a single 3.0 volt power supply for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations.

Contents

1. Simultaneous Read/Write Operations with Zero Latency

The Simultaneous Read/Write architecture provides **simultaneous operation** by dividing the memory space into separate banks (see Table 2 on page 15). Sector addresses are fixed, system software can be used to form user-defined bank groups.

During an Erase/Program operation, any of the non-busy banks may be read from. *Note that only two banks can operate simultaneously.* The device can improve overall system performance by allowing a host system to program or erase in one bank, then immediately and simultaneously read from the other bank, with zero latency. This releases the system from waiting for the completion of program or erase operations.

The S29JL032J can be organized with either a top or bottom boot sector configuration.

1.1 S29JL032J Features

The **Secured Silicon Region** is an extra 256 byte sector capable of being permanently locked by the customer. The Secured Silicon Customer Indicator Bit (DQ6) is permanently set to 1 if the part has been locked and is 0 if lockable.

Customers may utilize the Secured Silicon Region as bonus space, reading and writing like any other flash sector, or may permanently lock their own code there.

The device offers complete compatibility with the **JEDEC 42.4 single-power-supply Flash command set standard**. Commands are written to the command register using standard microprocessor write timings. Reading data out of the device is similar to reading from other Flash or EPROM devices.

The host system can detect whether a program or erase operation is complete by using the device **status bits:** RY/BY# pin, DQ7 (Data# Polling) and DQ6/DQ2 (toggle bits). After a program or erase cycle has been completed, the device automatically returns to the read mode.

The **sector erase architecture** allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectors. The device is fully erased when shipped from the factory.

Hardware data protection measures include a low V_{CC} detector that automatically inhibits write operations during power transitions. The **hardware sector protection** feature disables both program and erase operations in any combination of the sectors of memory. This can be achieved in-system or via programming equipment.

The Erase Suspend/Erase Resume feature enables the user to put erase on hold for any period of time to read data from, or program data to, any sector that is not selected for erasure. True background erase can thus be achieved. If a read is needed from the Secured Silicon Region area (One Time Program area) after an erase suspend, then the user must use the proper command sequence to enter and exit this region.

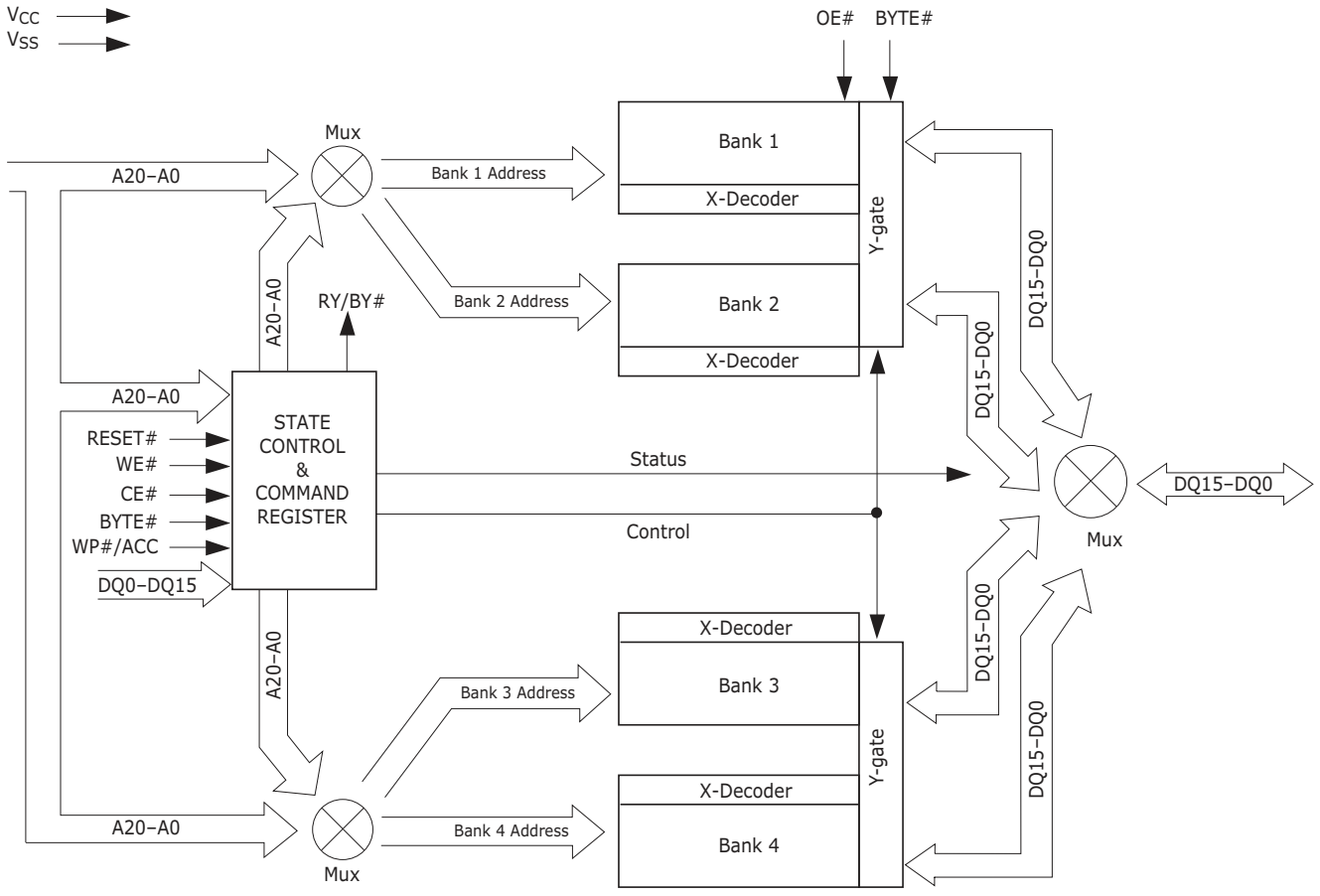
The device offers two power-saving features. When addresses have been stable for a specified amount of time, the device enters the **automatic sleep mode**. The system can also place the device into the **standby mode**. Power consumption is greatly reduced in both modes.

2. Product Selector Guide

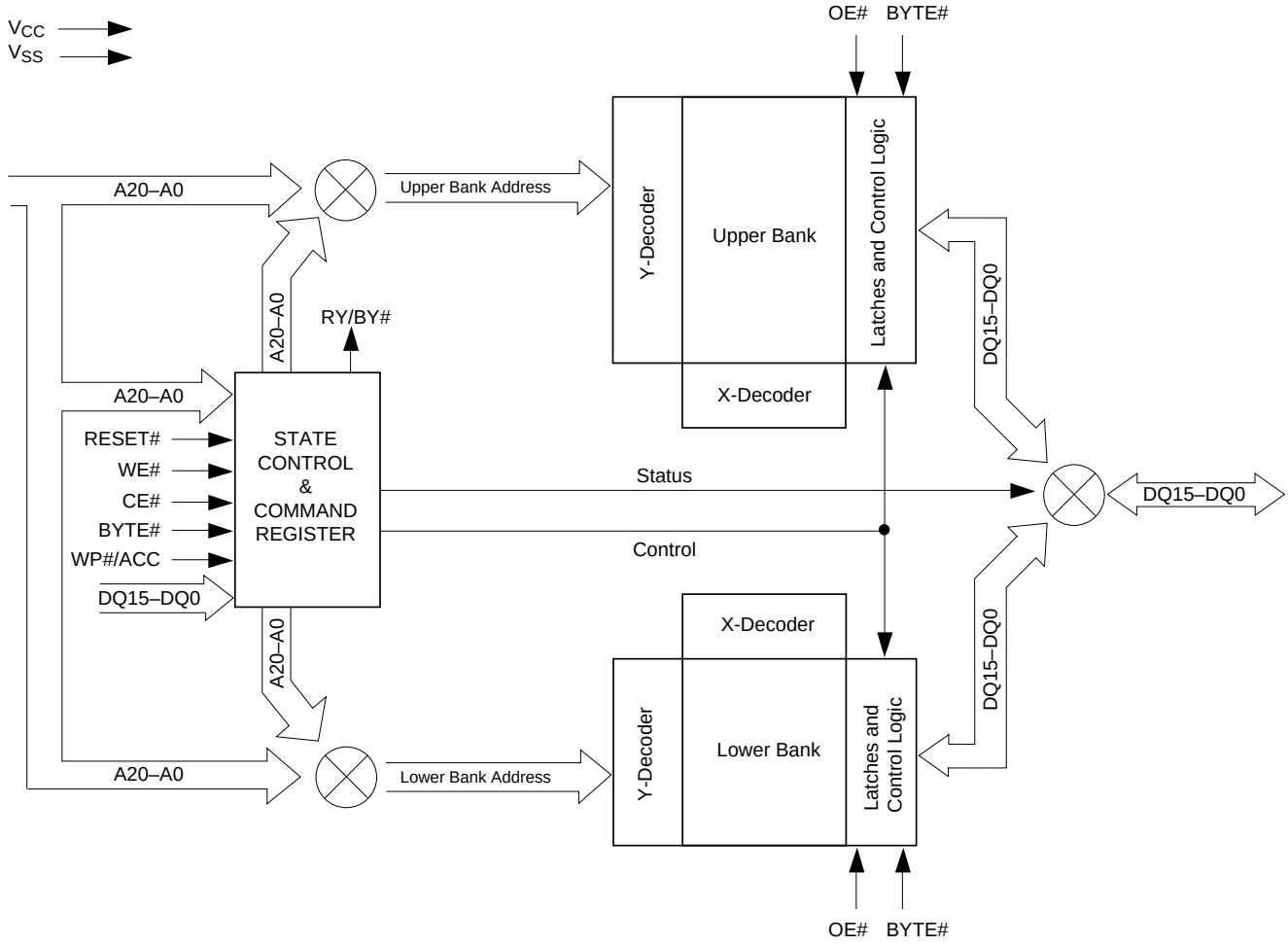
Part Number		S29JL032J	
Speed Option	Standard Voltage Range: V_{CC} = 3.0–3.6 V	60	
	Standard Voltage Range: V_{CC} = 2.7–3.6 V		70
Max Access Time (ns), t_{ACC}		60	70
CE# Access (ns), t_{CE}		60	70
OE# Access (ns), t_{OE}		25	30

3. Block Diagram

3.1 4-Bank Device

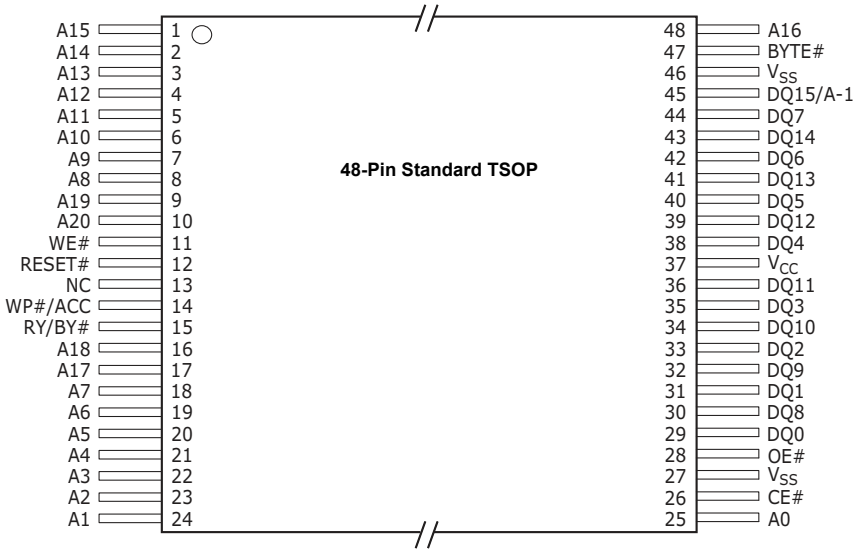


3.2 2-Bank Device

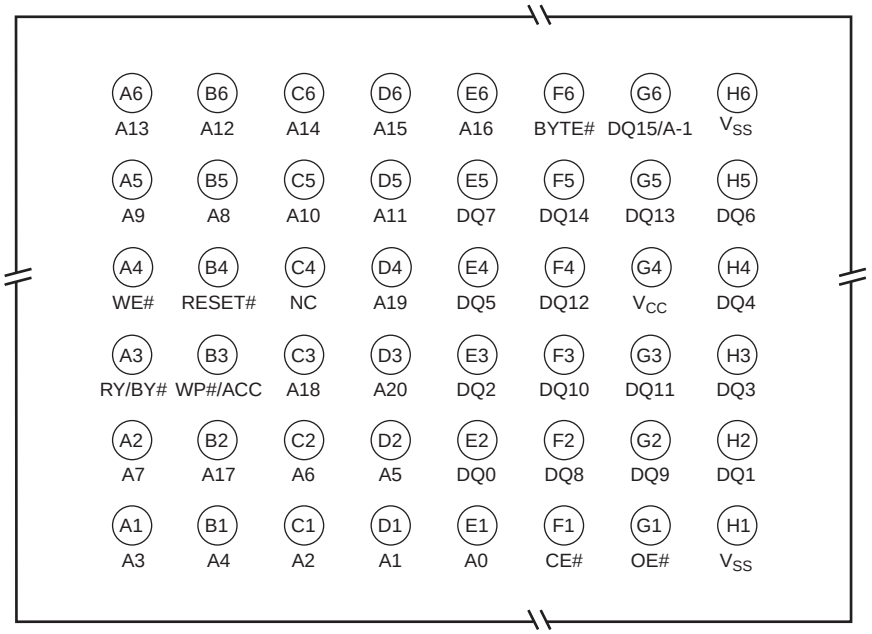


4. Connection Diagrams

4.1 48-pin TSOP Package



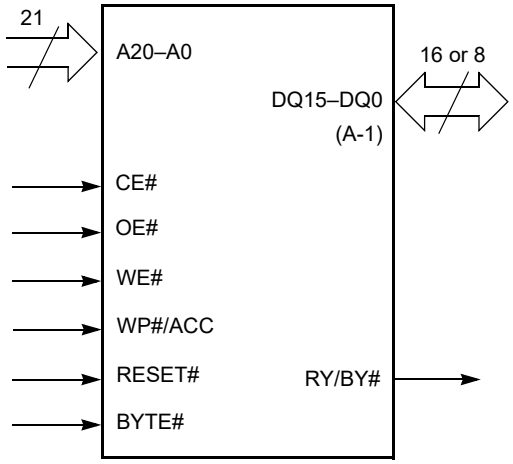
4.2 48-ball FBGA Package



5. Pin Description

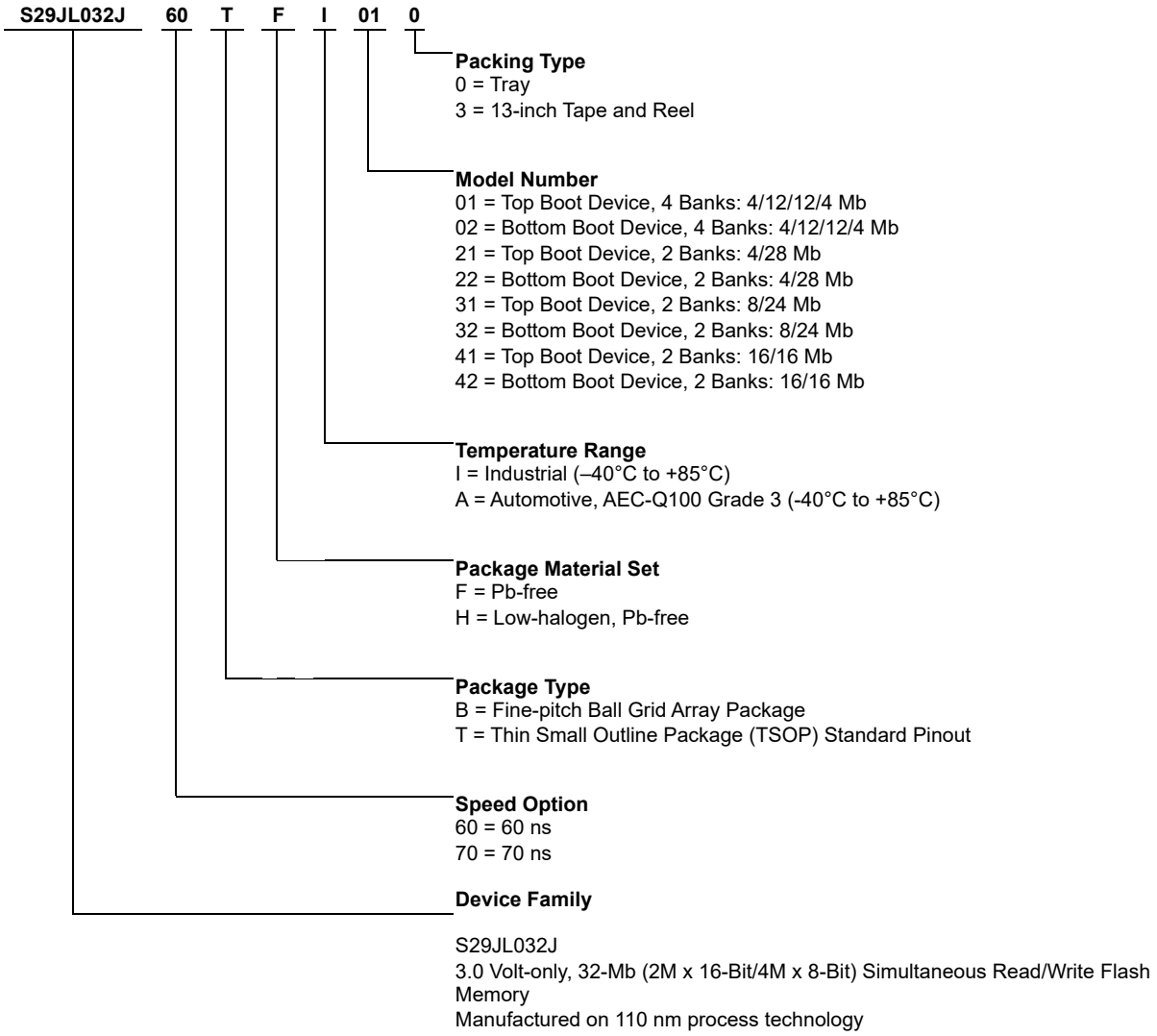
A20–A0	21 Address Pins
DQ14–DQ0	15 Data Inputs/Outputs (x16-only devices)
DQ15/A-1	DQ15 (Data Input/Output, word mode), A-1 (LSB Address Input, byte mode)
CE#	Chip Enable, Active Low
OE#	Output Enable, Active Low
WE#	Write Enable, Active Low
WP#/ACC	Hardware Write Protect/Acceleration Pin.
RESET#	Hardware Reset Pin, Active Low
BYTE#	Selects 8-bit or 16-bit mode, Active Low
RY/BY#	Ready/Busy Output, Active Low
V_{CC}	3.0 volt-only single power supply (see Section 2. Product Selector Guide on page 5 for speed options and voltage supply tolerances)
V_{SS}	Device Ground
NC	Not Connected – No device internal signal is connected to the package connector nor is there any future plan to use the connector for a signal. The connection may safely be used for routing space for a signal on a Printed Circuit Board (PCB).

6. Logic Symbol



7. Ordering Information

The order number (Valid Combination) is formed by the following:



Valid Combinations — Standard

S29JL032J Valid Combinations							
Device Number/ Description	**Speed (ns)**	**Package Type**	**Temperature Range**	**Additional Ordering Options**	**Packing Type**	**Package Description**	
S29JL032J	60, 70	TF	I	01, 02, 21, 22, 31, 32, 41, 42	0, 3[1]	TS048	TSOP
		BH		31, 32		VBK048	FBGA

Note
1. Type 0 is standard. Specify others as required.

Valid Combinations — Automotive Grade / AEC-Q100

The table below lists configurations that are Automotive Grade / AEC-Q100 qualified and are planned to be available in volume. The table will be updated as new combinations are released. Consult your local sales representative to confirm availability of specific combinations and to check on newly released combinations.

Production Part Approval Process (PPAP) support is only provided for AEC-Q100 grade products.

Products to be used in end-use applications that require ISO/TS-16949 compliance must be AEC-Q100 grade products in combination with PPAP. Non–AEC-Q100 grade products are not manufactured or documented in full compliance with ISO/TS-16949 requirements.

AEC-Q100 grade products are also offered without PPAP support for end-use applications that do not require ISO/TS-16949 compliance.

S29JL032J Valid Combinations - Automotive						
Device Number	**Speed (ns)**	**Package Type and Material**	**Temperature Range**	**Model Number**	**Packing Type**	**Package Description**
S29JL032J	70	TF	A	01	0, 3	TSOP

8. Device Bus Operations

This section describes the requirements and use of the device bus operations, which are initiated through the internal command register. The command register itself does not occupy any addressable memory location. The register is a latch used to store the commands, along with the address and data information needed to execute the command. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device. Table 1 lists the device bus operations, the inputs and control levels they require, and the resulting output. The following subsections describe each of these operations in further detail.

Table 1. S29JL032J Device Bus Operations

Operation	CE#	OE#	WE#	RESET#	WP#/ ACC	Addresses[1]	DQ15–DQ8		DQ7–DQ0
							BYTE# = V_{IH}	BYTE# = V_{IL}	
Read	L	L	H	H	L/H	A_{IN}	D_{OUT}	DQ14–DQ8 = High-Z, DQ15 = A-1	D_{OUT}
Write	L	H	L	H	Note [4]	A_{IN}	D_{IN}		D_{IN}
Standby	$V_{CC} \pm 0.3V$	X	X	$V_{CC} \pm 0.3V$	L/H	X	High-Z	High-Z	High-Z
Output Disable	L	H	H	H	L/H	X	High-Z	High-Z	High-Z
Reset	X	X	X	L	L/H	X	High-Z	High-Z	High-Z
Sector Protect[3]	L	H	L	V_{ID}	L/H	SA, A6 = L, A1 = H, A0 = L	X	X	D_{IN}
Sector Unprotect[3]	L	H	L	V_{ID}	Note [4]	SA, A6 = H, A1 = H, A0 = L	X	X	D_{IN}
Temporary Sector Unprotect	X	X	X	V_{ID}	Note [4]	A_{IN}	D_{IN}	High-Z	D_{IN}

Legend

L = Logic Low = V_{IL}
H = Logic High = V_{IH}
V_{ID} = 8.5–12.5V
V_{HH} = 9.0 ± 0.5V
X = Don't Care
SA = Sector Address
A_{IN} = Address In
D_{IN} = Data In
D_{OUT} = Data Out

Notes

2. Addresses are A20:A0 in word mode (BYTE# = V_{IH}), A20:A-1 in byte mode (BYTE# = V_{IL}).
3. The sector protect and sector unprotect functions may also be implemented via programming equipment. See Section 8.10 Boot Sector/Sector Block Protection and Unprotection on page 21.
4. If WP#/ACC = V_{IL}, the two outermost boot sectors remain protected. If WP#/ACC = V_{IH}, protection on the two outermost boot sectors depends on whether they were last protected or unprotected using the method described in Boot Sector/Sector Block Protection and Unprotection. If WP#/ACC = V_{HH}, all sectors will be unprotected.

8.1 Word/Byte Configuration

The BYTE# pin controls whether the device data I/O pins operate in the byte or word configuration. If the BYTE# pin is set at logic '1', the device is in word configuration, DQ15–DQ0 are active and controlled by CE# and OE#.

If the BYTE# pin is set at logic '0', the device is in byte configuration, and only data I/O pins DQ7–DQ0 are active and controlled by CE# and OE#. The data I/O pins DQ14–DQ8 are tristated, and the DQ15 pin is used as an input for the LSB (A-1) address function.

8.2 Requirements for Reading Array Data

To read array data from the outputs, the system must drive the CE# and OE# pins to V_{IL}. CE# is the power control and selects the device. OE# is the output control and gates array data to the output pins. WE# should remain at V_{IH}. The BYTE# pin determines whether the device outputs array data in words or bytes.

The internal state machine is set for reading array data upon device power-up, or after a hardware reset. This ensures that no spurious alteration of the memory content occurs during the power transition. No command is necessary in this mode to obtain array data. Standard microprocessor read cycles that assert valid addresses on the device address inputs produce valid data on the device data outputs. Each bank remains enabled for read access until the command register contents are altered.

Refer to the Section 17.1 Read-Only Operations on page 48 for timing specifications and to Figure 12 on page 48 for the timing diagram. I_{CC1} in Section 14. DC Characteristics on page 44 represents the active current specification for reading array data.

8.3 Writing Commands/Command Sequences

To write a command or command sequence (which includes programming data to the device and erasing sectors of memory), the system must drive WE# and CE# to V_{IL}, and OE# to V_{IH}.

For program operations, the BYTE# pin determines whether the device accepts program data in bytes or words. Refer to Section 8.1 Word/Byte Configuration on page 12 for more information.

The device features an **Unlock Bypass** mode to facilitate faster programming. Once a bank enters the Unlock Bypass mode, only two write cycles are required to program a word or byte, instead of four. Section 10.5 Byte/Word Program Command Sequence on page 31 has details on programming data to the device using both standard and Unlock Bypass command sequences.

An erase operation can erase one sector, multiple sectors, or the entire device. Table 3 on page 16 and Table 4 on page 18 indicate the address space that each sector occupies. Similarly, a “sector address” is the address bits required to uniquely select a sector. Section 10. Command Definitions on page 30 has details on erasing a sector or the entire chip, or suspending/resuming the erase operation.

The device address space is divided into four banks. A “bank address” is the address bits required to uniquely select a bank.

I_{CC2} in the DC Characteristics table represents the active current specification for the write mode. Section 17. AC Characteristics on page 48 contains timing specification tables and timing diagrams for write operations.

8.3.1 Accelerated Program Operation

The device offers accelerated program operations through the ACC function. This is one of two functions provided by the WP#/ACC pin. This function is primarily intended to allow faster manufacturing throughput at the factory.

If the system asserts V_{HH} on this pin, the device automatically enters the aforementioned Unlock Bypass mode, temporarily unprotects any protected sectors, and uses the higher voltage on the pin to reduce the time required for program operations. The system would use a two-cycle program command sequence as required by the Unlock Bypass mode. Removing V_{HH} from the WP#/ACC pin returns the device to normal operation. *Note that V_{HH} must not be asserted on WP#/ACC for operations other than accelerated programming, or device damage may result. In addition, the WP#/ACC pin must not be left floating or unconnected; inconsistent behavior of the device may result. See Section 8.11 Write Protect (WP#) on page 23 for related information.*

8.3.2 Autoselect Functions

If the system writes the autoselect command sequence, the device enters the autoselect mode. The system can then read autoselect codes from the internal register (which is separate from the memory array) on DQ15–DQ0. Standard read cycle timings apply in this mode. Refer to Section 8.9 Autoselect Mode on page 20 and Section 10.3 Autoselect Command Sequence on page 31 for more information.

8.4 Simultaneous Read/Write Operations with Zero Latency

This device is capable of reading data from one bank of memory while programming or erasing in another bank of memory. An erase operation may also be suspended to read from or program to another location within the same bank (except the sector being erased). Figure 17 on page 53 shows how read and write cycles may be initiated for simultaneous operation with zero latency. I_{CC6} and I_{CC7} in Section 14. DC Characteristics on page 44 represent the current specifications for read-while-program and read-while-erase, respectively.

8.5 Standby Mode

When the system is not reading or writing to the device, it can place the device in the standby mode. In this mode, current consumption is greatly reduced, and the outputs are placed in the high impedance state, independent of the OE# input.

The device enters the CMOS standby mode when the CE# and RESET# pins are both held at V_{CC} ± 0.3V. *Note that this is a more restricted voltage range than V_{IH}.* If CE# and RESET# are held at V_{IH}, but not within V_{CC} ± 0.3V, the device will be in the standby mode, but the standby current will be greater. The device requires standard access time (t_{CE}) for read access when the device is in either of these standby modes, before it is ready to read data.

If the device is deselected during erasure or programming, the device draws active current until the operation is completed.

I_{CC3} in Section 14. DC Characteristics on page 44 represents the standby current specification.

8.6 Automatic Sleep Mode

The automatic sleep mode minimizes Flash device energy consumption. The device automatically enables this mode when addresses remain stable for t_{ACC} + 30 ns. The automatic sleep mode is independent of the CE#, WE#, and OE# control signals. Standard address access timings provide new data when addresses are changed. While in sleep mode, output data is latched and always available to the system. I_{CC5} in DC Characteristics represents the automatic sleep mode current specification.

8.7 RESET#: Hardware Reset Pin

The RESET# pin provides a hardware method of resetting the device to reading array data. When the RESET# pin is driven low for at least a period of t_{RP}, the device immediately terminates any operation in progress, tristates all output pins, and ignores all read/write commands for the duration of the RESET# pulse. The device also resets the internal state machine to reading array data. The operation that was interrupted should be reinitiated once the device is ready to accept another command sequence, to ensure data integrity.

Current is reduced for the duration of the RESET# pulse. When RESET# is held at V_{SS}±0.3V, the device draws CMOS standby current (I_{CC4}). If RESET# is held at V_{IL} but not within V_{SS}±0.3V, the standby current will be greater.

The RESET# pin may be tied to the system reset circuitry. A system reset would thus also reset the Flash memory, enabling the system to read the boot-up firmware from the Flash memory.

If RESET# is asserted during a program or erase operation, the RY/BY# pin remains a “0” (busy) until the internal reset operation is complete, which requires a time of t_{READY} (during Embedded Algorithms). The system can thus monitor RY/BY# to determine whether the reset operation is complete. If RESET# is asserted when a program or erase operation is not executing (RY/BY# pin is “1”), the reset operation is completed within a time of t_{READY} (not during Embedded Algorithms). The system can read data t_{RH} after the RESET# pin returns to V_{IH}.

Refer to Section 17.2 Hardware Reset (RESET#) on page 49 for RESET# parameters and to Figure 13 on page 49 for the timing diagram.

8.8 Output Disable Mode

When the OE# input is at V_{IH}, output from the device is disabled. The output pins are placed in the high impedance state.

Table 2. S29JL032J Bank Architecture

Device Model Number	Bank 1		Bank 2		Bank 3		Bank 4	
	Mb	Sector Size	Mb	Sector Size	Mb	Sector Size	Mb	Sector Size
01, 02	4 Mb	Eight 8 KB/ 4 kword, seven 64 KB/ 32 kword	12 Mb	Twenty-four 64 KB/ 32 kword	12 Mb	Twenty-four 64 KB/ 32 kword	4 Mb	Eight 64 KB/ 32 kword

Device Model Number	Bank 1		Bank 2	
	Mbs	Sector Size	Mb	Sector Size
21, 22	4 Mb	Eight 8 KB/4 kword, seven 64 KB/32 kword	28 Mb	Fifty-six 64 KB/32 kword
31, 32	8 Mb	Eight 8 KB/4 kword, fifteen 64 KB/32 kword	24 Mb	Forty-eight 64 KB/32 kword
41, 42	16 Mb	Eight 8 KB/4 kword, thirty-one 64 KB/32 kword	16 Mb	Thirty-two 64 KB/32 kword

Table 3. S29JL032J Sector Addresses - Top Boot Devices

S29JL032J (Model 41)	S29JL032J (Model 31)	S29JL032J (Model 21)	S29JL032J (Model 01)	Sector	Sector Address A20–A12	Sector Size (KB/kwords)	(x8) Address Range	(x16) Address Range
Bank 2	Bank 2	Bank 2	Bank 4	SA0	000000xxx	64/32	000000h-00FFFFh	000000h-07FFFh
				SA1	000001xxx	64/32	010000h-01FFFFh	008000h-0FFFFh
				SA2	000010xxx	64/32	020000h-02FFFFh	010000h-17FFFh
				SA3	000011xxx	64/32	030000h-03FFFFh	018000h-01FFFFh
				SA4	000100xxx	64/32	040000h-04FFFFh	020000h-027FFFh
				SA5	000101xxx	64/32	050000h-05FFFFh	028000h-02FFFFh
				SA6	000110xxx	64/32	060000h-06FFFFh	030000h-037FFFh
				SA7	000111xxx	64/32	070000h-07FFFFh	038000h-03FFFFh
			Bank 3	SA8	001000xxx	64/32	080000h-08FFFFh	040000h-047FFFh
				SA9	001001xxx	64/32	090000h-09FFFFh	048000h-04FFFFh
				SA10	001010xxx	64/32	0A0000h-0AFFFFh	050000h-057FFFh
				SA11	001011xxx	64/32	0B0000h-0BFFFFh	058000h-05FFFFh
				SA12	001100xxx	64/32	0C0000h-0CFFFFh	060000h-067FFFh
				SA13	001101xxx	64/32	0D0000h-0DFFFFh	068000h-06FFFFh
				SA14	001110xxx	64/32	0E0000h-0EFFFFh	070000h-077FFFh
				SA15	001111xxx	64/32	0F0000h-0FFFFFh	078000h-07FFFFh
				SA16	010000xxx	64/32	100000h-10FFFFh	080000h-087FFFh
				SA17	010001xxx	64/32	110000h-11FFFFh	088000h-08FFFFh
				SA18	010010xxx	64/32	120000h-12FFFFh	090000h-097FFFh
				SA19	010011xxx	64/32	130000h-13FFFFh	098000h-09FFFFh
				SA20	010100xxx	64/32	140000h-14FFFFh	0A0000h-0A7FFFh
				SA21	010101xxx	64/32	150000h-15FFFFh	0A8000h-0AFFFFh
				SA22	010110xxx	64/32	160000h-16FFFFh	0B0000h-0B7FFFh
				SA23	010111xxx	64/32	170000h-17FFFFh	0B8000h-0BFFFFh
				SA24	011000xxx	64/32	180000h-18FFFFh	0C0000h-0C7FFFh
				SA25	011001xxx	64/32	190000h-19FFFFh	0C8000h-0CFFFFh
				SA26	011010xxx	64/32	1A0000h-1AFFFFh	0D0000h-0D7FFFh
				SA27	011011xxx	64/32	1B0000h-1BFFFFh	0D8000h-0DFFFFh
				SA28	011100xxx	64/32	1C0000h-1CFFFFh	0E0000h-0E7FFFh
				SA29	011101xxx	64/32	1D0000h-1DFFFFh	0E8000h-0EFFFFh
				SA30	011110xxx	64/32	1E0000h-1EFFFFh	0F0000h-0F7FFFh
				SA31	011111xxx	64/32	1F0000h-1FFFFFh	0F8000h-0FFFFFh

Table 3. S29JL032J Sector Addresses - Top Boot Devices (Continued)

S29JL032J (Model 41)	S29JL032J (Model 31)	S29JL032J (Model 21)	S29JL032J (Model 01)	Sector	Sector Address A20–A12	Sector Size (KB/kwords)	(x8) Address Range	(x16) Address Range
Bank 1	Bank 2 (continued)	Bank 2 (continued)	Bank 2	SA32	100000xxx	64/32	200000h-20FFFFh	100000h-107FFFh
				SA33	100001xxx	64/32	210000h-21FFFFh	108000h-10FFFFh
				SA34	100010xxx	64/32	220000h-22FFFFh	110000h-117FFFh
				SA35	100011xxx	64/32	230000h-23FFFFh	118000h-11FFFFh
				SA36	100100xxx	64/32	240000h-24FFFFh	120000h-127FFFh
				SA37	100101xxx	64/32	250000h-25FFFFh	128000h-12FFFFh
				SA38	100110xxx	64/32	260000h-26FFFFh	130000h-137FFFh
				SA39	100111xxx	64/32	270000h-27FFFFh	138000h-13FFFFh
				SA40	101000xxx	64/32	280000h-28FFFFh	140000h-147FFFh
				SA41	101001xxx	64/32	290000h-29FFFFh	148000h-14FFFFh
				SA42	101010xxx	64/32	2A0000h-2AFFFFh	150000h-157FFFh
				SA43	101011xxx	64/32	2B0000h-2BFFFFh	158000h-15FFFFh
				SA44	101100xxx	64/32	2C0000h-2CFFFFh	160000h-167FFFh
				SA45	101101xxx	64/32	2D0000h-2DFFFFh	168000h-16FFFFh
				SA46	101110xxx	64/32	2E0000h-2EFFFFh	170000h-177FFFh
				SA47	101111xxx	64/32	2F0000h-2FFFFFh	178000h-17FFFFh
	Bank 1			SA48	110000xxx	64/32	300000h-30FFFFh	180000h-187FFFh
				SA49	110001xxx	64/32	310000h-31FFFFh	188000h-18FFFFh
				SA50	110010xxx	64/32	320000h-32FFFFh	190000h-197FFFh
				SA51	110011xxx	64/32	330000h-33FFFFh	198000h-19FFFFh
				SA52	110100xxx	64/32	340000h-34FFFFh	1A0000h-1A7FFFh
				SA53	110101xxx	64/32	350000h-35FFFFh	1A8000h-1AFFFFh
				SA54	110110xxx	64/32	360000h-36FFFFh	1B0000h-1BFFFFh
				SA55	110111xxx	64/32	370000h-37FFFFh	1B8000h-1BFFFFh
		Bank 1	Bank 1	SA56	111000xxx	64/32	380000h-38FFFFh	1C0000h-1C7FFFh
				SA57	111001xxx	64/32	390000h-39FFFFh	1C8000h-1CFFFFh
				SA58	111010xxx	64/32	3A0000h-3AFFFFh	1D0000h-1DFFFFh
				SA59	111011xxx	64/32	3B0000h-3BFFFFh	1D8000h-1DFFFFh
				SA60	111100xxx	64/32	3C0000h-3CFFFFh	1E0000h-1E7FFFh
				SA61	111101xxx	64/32	3D0000h-3DFFFFh	1E8000h-1EFFFFh
				SA62	111110xxx	64/32	3E0000h-3EFFFFh	1F0000h-1F7FFFh
				SA63	111111000	8/4	3F0000h-3F1FFFh	1F8000h-1F8FFFh
				SA64	111111001	8/4	3F2000h-3F3FFFh	1F9000h-1F9FFFh
				SA65	111111010	8/4	3F4000h-3F5FFFh	1FA000h-1FAFFFh
				SA66	111111011	8/4	3F6000h-3F7FFFh	1FB000h-1FBFFFh
				SA67	111111100	8/4	3F8000h-3F9FFFh	1FC000h-1FCFFFh
				SA68	111111101	8/4	3FA000h-3FBFFFh	1FD000h-1FDFFFh
				SA69	111111110	8/4	3FC000h-3FDFFFh	1FE000h-1FEFFFh
				SA70	111111111	8/4	3FE000h-3FFFFFh	1FF000h-1FFFFFh

Table 4. S29JL032J Sector Addresses - Bottom Boot Devices

S29JL032J (Model 42)	S29JL032J (Model 32)	S29JL032J (Model 22)	S29JL032J (Model 02)	Sector	Sector Address A20–A12	Sector Size (KB/kwords)	(x8) Address Range	(x16) Address Range
Bank 1	Bank 1	Bank 1	Bank 1	SA0	000000000	8/4	000000h-001FFFh	000000h-000FFFh
				SA1	000000001	8/4	002000h-003FFFh	001000h-001FFFh
				SA2	000000010	8/4	004000h-005FFFh	002000h-002FFFh
				SA3	000000011	8/4	006000h-007FFFh	003000h-003FFFh
				SA4	000000100	8/4	008000h-009FFFh	004000h-004FFFh
				SA5	000000101	8/4	00A000h-00BFFFh	005000h-005FFFh
				SA6	000000110	8/4	00C000h-00DFFFh	006000h-006FFFh
				SA7	000000111	8/4	00E000h-00FFFFh	007000h-007FFFh
				SA8	000001xxx	64/32	010000h-01FFFFh	008000h-00FFFFh
				SA9	000010xxx	64/32	020000h-02FFFFh	010000h-017FFFh
				SA10	000011xxx	64/32	030000h-03FFFFh	018000h-01FFFFh
				SA11	000100xxx	64/32	040000h-04FFFFh	020000h-027FFFh
				SA12	000101xxx	64/32	050000h-05FFFFh	028000h-02FFFFh
				SA13	000110xxx	64/32	060000h-06FFFFh	030000h-037FFFh
				SA14	000111xxx	64/32	070000h-07FFFFh	038000h-03FFFFh
		Bank 2	Bank 2	SA15	001000xxx	64/32	080000h-08FFFFh	040000h-047FFFh
				SA16	001001xxx	64/32	090000h-09FFFFh	048000h-04FFFFh
				SA17	001010xxx	64/32	0A0000h-0AFFFFh	050000h-057FFFh
				SA18	001011xxx	64/32	0B0000h-0BFFFFh	058000h-05FFFFh
				SA19	001100xxx	64/32	0C0000h-0CFFFFh	060000h-067FFFh
				SA20	001101xxx	64/32	0D0000h-0DFFFFh	068000h-06FFFFh
				SA21	001110xxx	64/32	0E0000h-0EFFFFh	070000h-077FFFh
				SA22	001111xxx	64/32	0F0000h-0FFFFFh	078000h-07FFFFh
	Bank 2			SA23	010000xxx	64/32	100000h-10FFFFh	080000h-087FFFh
				SA24	010001xxx	64/32	110000h-11FFFFh	088000h-08FFFFh
				SA25	010010xxx	64/32	120000h-12FFFFh	090000h-097FFFh
				SA26	010011xxx	64/32	130000h-13FFFFh	098000h-09FFFFh
				SA27	010100xxx	64/32	140000h-14FFFFh	0A0000h-0A7FFFh
				SA28	010101xxx	64/32	150000h-15FFFFh	0A8000h-0AFFFFh
				SA29	010110xxx	64/32	160000h-16FFFFh	0B0000h-0B7FFFh
				SA30	010111xxx	64/32	170000h-17FFFFh	0B8000h-0BFFFFh
				SA31	011000xxx	64/32	180000h-18FFFFh	0C0000h-0C7FFFh
				SA32	011001xxx	64/32	190000h-19FFFFh	0C8000h-0CFFFFh
				SA33	011010xxx	64/32	1A0000h-1AFFFFh	0D0000h-0D7FFFh
				SA34	011011xxx	64/32	1B0000h-1BFFFFh	0D8000h-0DFFFFh
				SA35	011100xxx	64/32	1C0000h-1CFFFFh	0E0000h-0E7FFFh
				SA36	011101xxx	64/32	1D0000h-1DFFFFh	0E8000h-0EFFFFh
				SA37	011110xxx	64/32	1E0000h-1EFFFFh	0F0000h-0F7FFFh
				SA38	011111xxx	64/32	1F0000h-1FFFFFh	0F8000h-0FFFFFh

Table 4. S29JL032J Sector Addresses - Bottom Boot Devices (Continued)

S29JL032J (Model 42)	S29JL032J (Model 32)	S29JL032J (Model 22)	S29JL032J (Model 02)	Sector	Sector Address A20–A12	Sector Size (KB/kwords)	(x8) Address Range	(x16) Address Range
Bank 2	Bank 2 (continued)	Bank 2 (continued)	Bank 3	SA39	100000xxx	64/32	200000h-20FFFFh	100000h-107FFFh
				SA40	100001xxx	64/32	210000h-21FFFFh	108000h-10FFFFh
				SA41	100010xxx	64/32	220000h-22FFFFh	110000h-117FFFh
				SA42	100011xxx	64/32	230000h-23FFFFh	118000h-11FFFFh
				SA43	100100xxx	64/32	240000h-24FFFFh	120000h-127FFFh
				SA44	100101xxx	64/32	250000h-25FFFFh	128000h-12FFFFh
				SA45	100110xxx	64/32	260000h-26FFFFh	130000h-137FFFh
				SA46	100111xxx	64/32	270000h-27FFFFh	138000h-13FFFFh
				SA47	101000xxx	64/32	280000h-28FFFFh	140000h-147FFFh
				SA48	101001xxx	64/32	290000h-29FFFFh	148000h-14FFFFh
				SA49	101010xxx	64/32	2A0000h-2AFFFFh	150000h-157FFFh
				SA50	101011xxx	64/32	2B0000h-2BFFFFh	158000h-15FFFFh
				SA51	101100xxx	64/32	2C0000h-2CFFFFh	160000h-167FFFh
				SA52	101101xxx	64/32	2D0000h-2DFFFFh	168000h-16FFFFh
				SA53	101110xxx	64/32	2E0000h-2EFFFFh	170000h-177FFFh
				SA54	101111xxx	64/32	2F0000h-2FFFFFh	178000h-17FFFFh
				SA55	110000xxx	64/32	300000h-30FFFFh	180000h-187FFFh
				SA56	110001xxx	64/32	310000h-31FFFFh	188000h-18FFFFh
				SA57	110010xxx	64/32	320000h-32FFFFh	190000h-197FFFh
				SA58	110011xxx	64/32	330000h-33FFFFh	198000h-19FFFFh
				SA59	110100xxx	64/32	340000h-34FFFFh	1A0000h-1A7FFFh
				SA60	110101xxx	64/32	350000h-35FFFFh	1A8000h-1AFFFFh
				SA61	110110xxx	64/32	360000h-36FFFFh	1B0000h-1B7FFFh
				SA62	110111xxx	64/32	370000h-37FFFFh	1B8000h-1BFFFFh
			Bank 4	SA63	111000xxx	64/32	380000h-38FFFFh	1C0000h-1C7FFFh
				SA64	111001xxx	64/32	390000h-39FFFFh	1C8000h-1CFFFFh
				SA65	111010xxx	64/32	3A0000h-3AFFFFh	1D0000h-1D7FFFh
				SA66	111011xxx	64/32	3B0000h-3BFFFFh	1D8000h-1DFFFFh
				SA67	111100xxx	64/32	3C0000h-3CFFFFh	1E0000h-1E7FFFh
				SA68	111101xxx	64/32	3D0000h-3DFFFFh	1E8000h-1EFFFFh
				SA69	111110xxx	64/32	3E0000h-3EFFFFh	1F0000h-1F7FFFh
				SA70	111111xxx	64/32	3F0000h-3F1FFFh	1F8000h-1FFFFFh

8.9 Autoselect Mode

The autoselect mode provides manufacturer and device identification, and sector protection verification, through identifier codes output on DQ7–DQ0. This mode is primarily intended for programming equipment to automatically match a device to be programmed with its corresponding programming algorithm. However, the autoselect codes can also be accessed in-system through the command register.

When using programming equipment, the autoselect mode requires V_{ID} on address pin A9. Address pins must be as shown in Table 5. In addition, when verifying sector protection, the sector address must appear on the appropriate highest order address bits. Table 5 shows the remaining address bits that are don't care. When all necessary bits have been set as required, the programming equipment may then read the corresponding identifier code on DQ7–DQ0. However, the autoselect codes can also be accessed in-system through the command register, for instances when the S29JL032J is erased or programmed in a system without access to high voltage on the A9 pin. The command sequence is illustrated in Table 13 on page 35. *Note that if a Bank Address (BA) on address bits A20, A19 and A18 is asserted during the third write cycle of the autoselect command, the host system can read autoselect data from that bank and then immediately read array data from another bank, without exiting the autoselect mode.*

To access the autoselect codes in-system, the host system can issue the autoselect command via the command register, as shown in Table 13 on page 35. This method does not require V_{ID}. Refer to Section 10.3 Autoselect Command Sequence on page 31 for more information.

Table 5. S29JL032J Autoselect Codes (High Voltage Method)

Description		CE#	OE#	WE#	A20 to A12	A11 to A10	A9	A8 to A7	A6	A5 to A4	A3	A2	A1	A0	DQ15 to DQ8		DQ7 to DQ0
															BYTE# = V_{IH}	BYTE# = V_{IL}	
Manufacturer ID: Cypress Products		L	L	H	BA	X	V_{ID}	X	L	X	L	L	L	L	X	X	01h
Device ID (Models 01, 02)	Read Cycle 1	L	L	H	BA	X	V_{ID}	X	L	X	L	L	L	H	22h	X	7Eh
	Read Cycle 2								L		H	H	H	L	22h		0Ah
	Read Cycle 3								L		H	H	H	H	22h		00h (bottom boot) 01h (top boot)
Device ID (Models 21, 22)		L	L	H	BA	X	V_{ID}	X	L	X	X	X	L	H	22h	X	56h (bottom boot) 55h (top boot)
Device ID (Models 31, 32)		L	L	H	BA	X	V_{ID}	X	L	X	X	X	L	H	22h	X	53h (bottom boot) 50h (top boot)
Device ID (Models 41, 42)		L	L	H	BA	X	V_{ID}	X	L	X	X	X	L	H	22h	X	5Fh (bottom boot) 5Ch (top boot)
Sector Protection Verification		L	L	H	SA	X	V_{ID}	X	L	X	L	L	H	L	X	X	01h (protected), 00h (unprotected)
Secured Silicon Indicator Bit (DQ6, DQ7)		L	L	H	BA	X	V_{ID}	X	L	X	L	L	H	H	X	X	82h (Factory Locked), 42h (Customer Locked), 02h (Not Locked)

Legend

L = Logic Low = V_{IL}

H = Logic High = V_{IH}

BA = Bank Address

SA = Sector Address

X = Don't care.

8.10 Boot Sector/Sector Block Protection and Unprotection

Note: For the following discussion, the term "sector" applies to both boot sectors and sector blocks. A sector block consists of two or more adjacent sectors that are protected or unprotected at the same time (see Table 6).

The hardware sector protection feature disables both program and erase operations in any sector. The hardware sector unprotection feature re-enables both program and erase operations in previously protected sectors. Sector protection/unprotection can be implemented via two methods.

Table 6. S29JL032J Boot Sector/Sector Block Addresses for Protection/Unprotection (Top Boot Devices)

Sector	A20-A12	Sector/ Sector Block Size
SA0	000000XXX	64 KB
SA1-SA3	000001XXX 000010XXX 000011XXX	192 (3X64) KB
SA4-SA7	0001XXXXX	256 (4X64) KB
SA8-SA11	0010XXXXX	256 (4X64) KB
SA12-SA15	0011XXXXX	256 (4X64) KB
SA16-SA19	0100XXXXX	256 (4X64) KB
SA20-SA23	0101XXXXX	256 (4X64) KB
SA24-SA27	0110XXXXX	256 (4X64) KB
SA28-SA31	0111XXXXX	256 (4X64) KB
SA32-SA35	1000XXXXX	256 (4X64) KB
SA36-SA39	1001XXXXX	256 (4X64) KB
SA40-SA43	1010XXXXX	256 (4X64) KB
SA44-SA47	1011XXXXX	256 (4X64) KB
SA48-SA51	1100XXXXX	256 (4X64) KB
SA52-SA55	1101XXXXX	256 (4X64) KB
SA56-SA59	1110XXXXX	256 (4X64) KB
SA60-SA62	111100XXX 111101XXX 111110XXX	192 (3X64) KB
SA63	111111000	8 KB
SA64	111111001	8 KB
SA65	111111010	8 KB
SA66	111111011	8 KB
SA67	111111100	8 KB
SA68	111111101	8 KB
SA69	111111110	8 KB
SA70	111111111	8 KB

Table 7. S29JL032J Sector/Sector Block Addresses for Protection/Unprotection (Bottom Boot Devices)

Sector	A20-A12	Sector/ Sector Block Size
SA70	111111XXX	64 KB
SA69-SA67	111110XXX 111101XXX 111100XXX	192 (3X64) KB
SA66-SA63	1110XXXXX	256 (4X64) KB
SA62-SA59	1101XXXXX	256 (4X64) KB
SA58-SA55	1100XXXXX	256 (4X64) KB
SA54-SA51	1011XXXXX	256 (4X64) KB
SA50-SA47	1010XXXXX	256 (4X64) KB
SA46-SA43	1001XXXXX	256 (4X64) KB
SA42-SA39	1000XXXXX	256 (4X64) KB
SA38-SA35	0111XXXXX	256 (4X64) KB
SA34-SA31	0110XXXXX	256 (4X64) KB
SA30-SA27	0101XXXXX	256 (4X64) KB
SA26-SA23	0100XXXXX	256 (4X64) KB
SA22-SA19	0011XXXXX	256 (4X64) KB
SA18-SA15	0010XXXXX	256 (4X64) KB
SA14-SA11	0001XXXXX	256 (4X64) KB
SA10-SA8	000011XXX 000010XXX 000001XXX	192 (3X64) KB
SA7	000000111	8 KB
SA6	000000110	8 KB
SA5	000000101	8 KB
SA4	000000100	8 KB
SA3	000000011	8 KB
SA2	000000010	8 KB
SA1	000000001	8 KB
SA0	000000000	8 KB

Sector Protect/Sector Unprotect requires V_{ID} on the RESET# pin only, and can be implemented either in-system or via programming equipment. Figure 2 on page 24 shows the algorithms and Figure 17.4 on page 56 shows the timing diagram. For sector unprotect, all unprotected sectors must first be protected prior to the first sector unprotect write cycle. *Note that the sector unprotect algorithm unprotects all sectors in parallel.* All previously protected sectors must be individually re-protected. To change data in protected sectors efficiently, the temporary sector unprotect function is available. See Section 8.12 Temporary Sector Unprotect on page 23.

The device is shipped with all sectors unprotected. Optional Cypress programming service enable programming and protecting sectors at the factory prior to shipping the device. Contact your local sales office for details.

It is possible to determine whether a sector is protected or unprotected. See Section 8.9 Autoselect Mode on page 20 for details.

8.11 Write Protect (WP#)

The Write Protect function provides a hardware method of protecting certain boot sectors without using V_{ID}. This function is one of two provided by the WP#/ACC pin.

If the system asserts V_{IL} on the WP#/ACC pin, the device disables program and erase functions in the two outermost 8 KB boot sectors independently of whether those sectors were protected or unprotected using the method described in Section 8.10 Boot Sector/Sector Block Protection and Unprotection on page 21. The two outermost 8 KB boot sectors are the two sectors containing the lowest addresses in a bottom-boot-configured device, or the two sectors containing the highest addresses in a top-boot-configured device.

If the system asserts V_{IH} on the WP#/ACC pin, the device reverts to whether the two outermost 8K Byte boot sectors were last set to be protected or unprotected. That is, sector protection or unprotection for these two sectors depends on whether they were last protected or unprotected using the method described in Section 8.10 Boot Sector/Sector Block Protection and Unprotection on page 21.

Note that the WP#/ACC pin must not be left floating or unconnected; inconsistent behavior of the device may result.

Table 8. WP#/ACC Modes

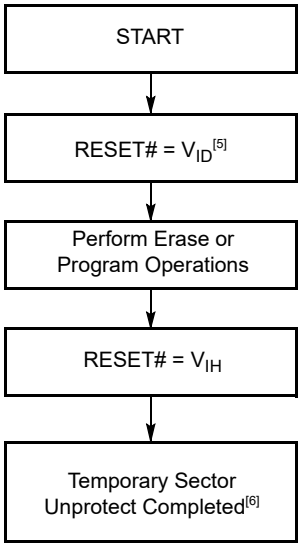
WP# Input Voltage	Device Mode
V_{IL}	Disables programming and erasing in the two outermost boot sectors
V_{IH}	Enables programming and erasing in the two outermost boot sectors, dependent on whether they were last protected or unprotected
V_{HH}	Enables accelerated programming (ACC). See Section 8.3.1 Accelerated Program Operation on page 13.

8.12 Temporary Sector Unprotect

Note: For the following discussion, the term "sector" applies to both sectors and sector blocks. A sector block consists of two or more adjacent sectors that are protected or unprotected at the same time (see Table 6 on page 21 and Table 7 on page 22).

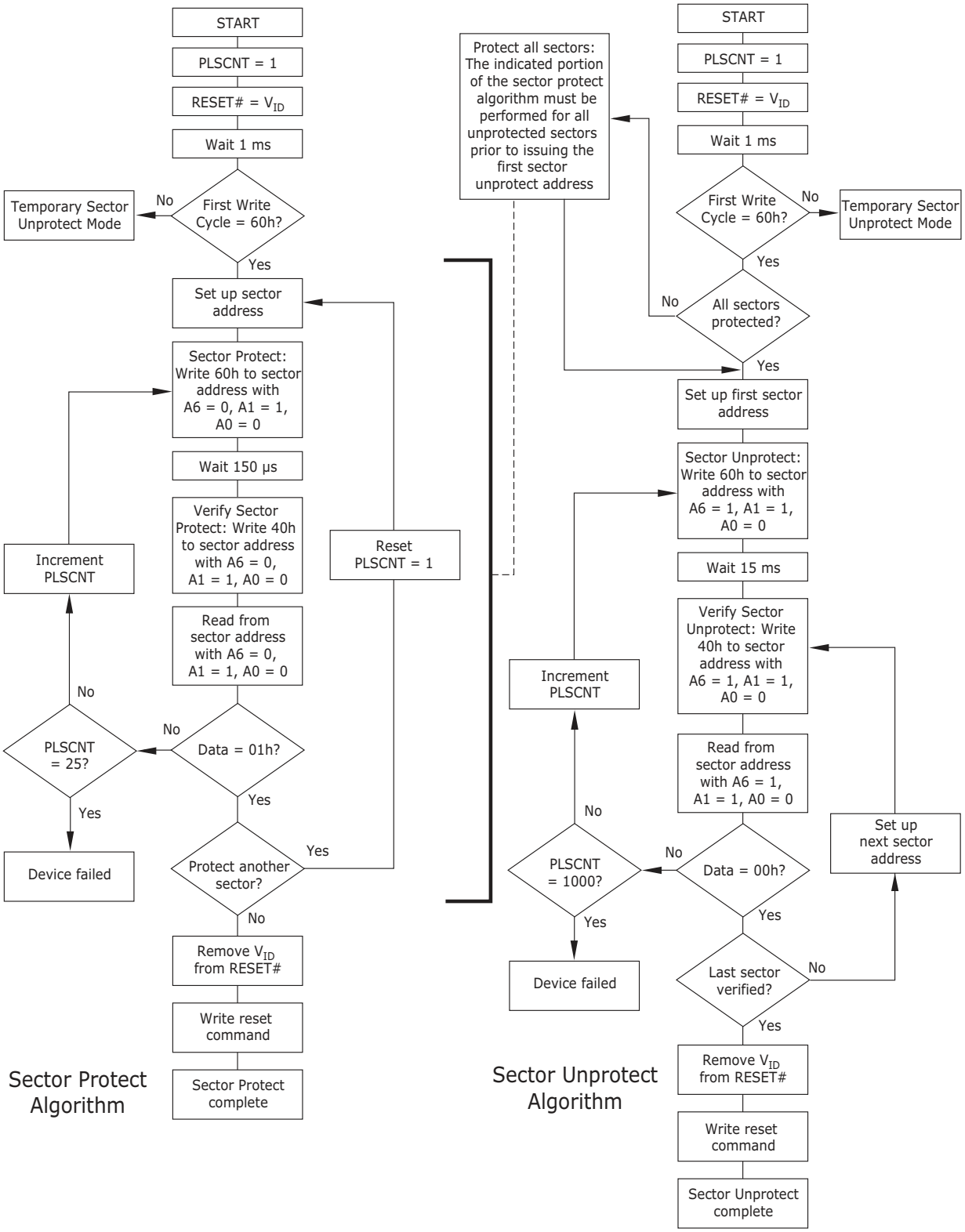
This feature allows temporary unprotection of previously protected sectors to change data in-system. The Temporary Sector Unprotect mode is activated by setting the RESET# pin to V_{ID}. During this mode, formerly protected sectors can be programmed or erased by selecting the sector addresses. Once V_{ID} is removed from the RESET# pin, all the previously protected sectors are protected again. Figure 1 on page 23 shows the algorithm, and Figure 17.3 on page 55 shows the timing diagrams, for this feature. If the WP#/ACC pin is at V_{IL}, the two outermost boot sectors will remain protected during the Temporary sector Unprotect mode.

Figure 1. Temporary Sector Unprotect Operation



Notes
5. All protected sectors unprotected (If WP#/ACC = V_{IL}, the outermost two boot sectors will remain protected).
6. All previously protected sectors are protected once again.

Figure 2. In-System Sector Protect/Unprotect Algorithms



8.13 Secured Silicon Region

The Secured Silicon Region feature provides a Flash memory region that enables permanent part identification through an Electronic Serial Number (ESN). The Secured Silicon Region is 256 bytes in length, and may shipped unprotected, allowing customers to utilize that sector in any manner they choose, or may shipped locked at the factory (upon customer request). The Secured Silicon Indicator Bit data will be 82h if factory locked, 42h if customer locked, or 02h if neither. Refer to Table 5 on page 20 for more details.

The system accesses the Secured Silicon through a command sequence (see Section 10.4 Enter Secured Silicon Region/Exit Secured Silicon Region Command Sequence on page 31). After the system has written the Enter Secured Silicon Region command sequence, it may read the Secured Silicon Region by using the addresses normally occupied by the boot sectors. This mode of operation continues until the system issues the Exit Secured Silicon Region command sequence, or until power is removed from the device. On power-up, or following a hardware reset, the device reverts to sending commands to the first 256 bytes of Sector 0. *Note that the ACC function and unlock bypass modes are not available when the Secured Silicon Region is enabled.*

8.13.1 Factory Locked: Secured Silicon Region Programmed and Protected At the Factory

In a factory locked device, the Secured Silicon Region is protected when the device is shipped from the factory. The Secured Silicon Region cannot be modified in any way. The device is preprogrammed with both a random number and a secure ESN. The 8-word random number is at addresses 000000h-000007h in word mode (or 000000h-00000Fh in byte mode). The secure ESN is programmed in the next 8 words at addresses 000008h-00000Fh (or 000010h-00001Fh in byte mode). The device is available preprogrammed with one of the following:

- A random, secure ESN only
- Customer code through Cypress programming services
- Both a random, secure ESN and customer code through Cypress programming services

Contact an your local sales office for details on using Cypress programming services.

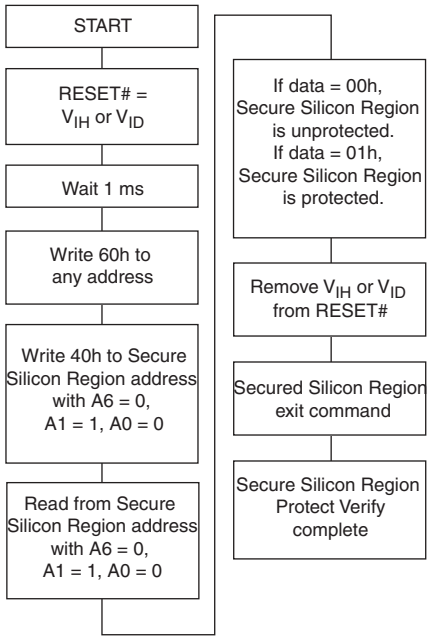
8.13.2 Customer Lockable: Secured Silicon Region NOT Programmed or Protected At the Factory

If the security feature is not required, the Secured Silicon Region can be treated as an additional Flash memory space. The Secured Silicon Region can be read any number of times, but can be programmed and locked only once. *Note that the accelerated programming (ACC) and unlock bypass functions are not available when programming the Secured Silicon Region.*

- Write the three-cycle Enter Secured Silicon Region command sequence, and then follow the insystem sector protect algorithm as shown in Figure 2 on page 24, except that RESET# may be at either V_{IH} or V_{ID}. This allows in-system protection of the Secured Silicon Region without raising any device pin to a high voltage. *Note that this method is only applicable to the Secured Silicon Region.*
- To verify the protect/unprotect status of the Secured Silicon Region, follow the algorithm shown in Figure 3 on page 26.

Once the Secured Silicon Region is locked and verified, the system must write the Exit Secured Silicon Region command sequence to return to reading and writing the remainder of the array. The Secured Silicon Region lock must be used with caution since, once locked, there is no procedure available for unlocking the Secured Silicon Region area and none of the bits in the Secured Silicon Region memory space can be modified in any way.

Figure 3. Secured Silicon Region Protect Verify



8.14 Hardware Data Protection

The command sequence requirement of unlock cycles for programming or erasing provides data protection against inadvertent writes (refer to Table 13 on page 35 for command definitions). In addition, the following hardware data protection measures prevent accidental erasure or programming, which might otherwise be caused by spurious system level signals during V_{CC} power-up and power-down transitions, or from system noise.

8.14.1 Low V_{CC} Write Inhibit

When V_{CC} is less than V_{LKO}, the device does not accept any write cycles. This protects data during V_{CC} power-up and power-down. The command register and all internal program/erase circuits are disabled, and the device resets to the read mode. Subsequent writes are ignored until V_{CC} is greater than V_{LKO}. The system must provide the proper signals to the control pins to prevent unintentional writes when V_{CC} is greater than V_{LKO}.

8.14.2 Write Pulse “Glitch” Protection

Noise pulses of less than 5 ns (typical) on OE#, CE# or WE# do not initiate a write cycle.

8.14.3 Logical Inhibit

Write cycles are inhibited by holding any one of OE# = V_{IL}, CE# = V_{IH} or WE# = V_{IH}. To initiate a write cycle, CE# and WE# must be a logical zero while OE# is a logical one.

8.14.4 Power-Up Write Inhibit

If WE# = CE# = V_{IL} and OE# = V_{IH} during power up, the device does not accept commands on the rising edge of WE#. The internal state machine is automatically reset to the read mode on power-up.

9. Common Flash Memory Interface (CFI)

The Common Flash Interface (CFI) specification outlines device and host system software interrogation handshake, which allows specific vendor-specified software algorithms to be used for entire families of devices. Software support can then be device-independent, JEDEC ID-independent, and forward- and backward-compatible for the specified flash device families. Flash vendors can standardize their existing interfaces for long-term compatibility.

This device enters the CFI Query mode when the system writes the CFI Query command, 98h, to address 55h in word mode (or address AAh in byte mode), any time the device is ready to read array data. The system can read CFI information at the addresses given in Table 9. To terminate reading CFI data, the system must write the reset command. The CFI Query mode is not accessible when the device is executing an Embedded Program or embedded Erase algorithm.

The system can also write the CFI query command when the device is in the autoselect mode via the command register only (high voltage method does not apply). The device enters the CFI query mode, and the system can read CFI data at the addresses given in Table 9. The system must write the reset command to return to reading array data.

For further information, please refer to the CFI Specification and *CFI Publication 100*. Contact your local sales office for copies of these documents.

Table 9. CFI Query Identification String

Addresses (Word Mode)	Addresses (Byte Mode)	Data	Description
10h 11h 12h	20h 22h 24h	0051h 0052h 0059h	Query Unique ASCII string “QRY”
13h 14h	26h 28h	0002h 0000h	Primary OEM Command Set
15h 16h	2Ah 2Ch	0040h 0000h	Address for Primary Extended Table
17h 18h	2Eh 30h	0000h 0000h	Alternate OEM Command Set (00h = none exists)
19h 1Ah	32h 34h	0000h 0000h	Address for Alternate OEM Extended Table (00h = none exists)

Table 10. System Interface String

Addresses (Word Mode)	Addresses (Byte Mode)	Data	Description
1Bh	36h	0027h	V_{CC} Min. (write/erase) D7–D4: volt, D3–D0: 100 millivolt
1Ch	38h	0036h	V_{CC} Max. (write/erase) D7–D4: volt, D3–D0: 100 millivolt
1Dh	3Ah	0000h	V_{PP} Min. voltage (00h = no V_{PP} pin present)
1Eh	3Ch	0000h	V_{PP} Max. voltage (00h = no V_{PP} pin present)
1Fh	3Eh	0003h	Typical timeout per single byte/word write 2^N µs
20h	40h	0000h	Typical timeout for Min. size buffer write 2^N µs (00h = not supported)
21h	42h	0009h	Typical timeout per individual block erase 2^N ms
22h	44h	000Fh	Typical timeout for full chip erase 2^N ms (00h = not supported)
23h	46h	0004h	Max. timeout for byte/word write 2^N times typical
24h	48h	0000h	Max. timeout for buffer write 2^N times typical
25h	4Ah	0004h	Max. timeout per individual block erase 2^N times typical
26h	4Ch	0000h	Max. timeout for full chip erase 2^N times typical (00h = not supported)

Table 11. Device Geometry Definition

Addresses (Word Mode)	Addresses (Byte Mode)	Data	Description
27h	4Eh	0016h	Device Size = 2^N byte
28h 29h	50h 52h	0002h 0000h	Flash Device Interface description (refer to CFI publication 100)
2Ah 2Bh	54h 56h	0000h 0000h	Max. number of byte in multi-byte write = 2^N (00h = not supported)
2Ch	58h	0002h	Number of Erase Block Regions within device
2Dh 2Eh 2Fh 30h	5Ah 5Ch 5Eh 60h	0007h 0000h 0020h 0000h	Erase Block Region 1 Information (refer to the CFI specification or CFI publication 100)
31h 32h 33h 34h	62h 64h 66h 68h	003Eh 0000h 0000h 0001h	Erase Block Region 2 Information (refer to the CFI specification or CFI publication 100)
35h 36h 37h 38h	6Ah 6Ch 6Eh 70h	0000h 0000h 0000h 0000h	Erase Block Region 3 Information (refer to the CFI specification or CFI publication 100)
39h 3Ah 3Bh 3Ch	72h 74h 76h 78h	0000h 0000h 0000h 0000h	Erase Block Region 4 Information (refer to the CFI specification or CFI publication 100)

Table 12. Primary Vendor-Specific Extended Query

Addresses (Word Mode)	Addresses (Byte Mode)	Data	Description
40h 41h 42h	80h 82h 84h	0050h 0052h 0049h	Query-unique ASCII string “PRI”
43h	86h	0031h	Major version number, ASCII (reflects modifications to the silicon)
44h	88h	0033h	Minor version number, ASCII (reflects modifications to the CFI table)
45h	8Ah	000Ch	Address Sensitive Unlock (Bits 1-0) 0 = Required, 1 = Not Required Process Technology (Bits 7-2) 0011 = 0.11 µm Floating Gate
46h	8Ch	0002h	Erase Suspend 0 = Not Supported, 1 = To Read Only, 2 = To Read & Write
47h	8Eh	0001h	Sector Protect 0 = Not Supported, X = Number of sectors in per group
48h	90h	0001h	Sector Temporary Unprotect 00 = Not Supported, 01 = Supported
49h	92h	0004h	Sector Protect/Unprotect scheme 01 = 29F040 mode, 02 = 29F016 mode, 03 = 29F400, 04 = 29LV800 mode
4Ah	94h	00XXh	Number of sectors (excluding Bank 1) XX = 38 (models 01, 02, 21, 22) XX = 30 (models 31, 32) XX = 20 (models 41, 42)
4Bh	96h	0000h	Burst Mode Type 00 = Not Supported, 01 = Supported

Table 12. Primary Vendor-Specific Extended Query (Continued)

Addresses (Word Mode)	Addresses (Byte Mode)	Data	Description
4Ch	98h	0000h	Page Mode Type 00 = Not Supported, 01 = 4 Word Page, 02 = 8 Word Page
4Dh	9Ah	0085h	ACC (Acceleration) Supply Minimum 00h = Not Supported, D7-D4: Volt, D3-D0: 100 mV
4Eh	9Ch	0095h	ACC (Acceleration) Supply Maximum 00h = Not Supported, D7-D4: Volt, D3-D0: 100 mV
4Fh	9Eh	000Xh	Top/Bottom Boot Sector Flag 02h = Bottom Boot Device, 03h = Top Boot Device
50h	A0h	0000h	Program Suspend 0 = Not supported, 1 = Supported
57h	AEh	000Xh	Bank Organization 00 = Data at 4Ah is zero X = 4 (4 banks, models 01, 02) X = 2 (2 banks, all other models)
58h	B0h	00XXh	Bank 1 Region Information - Number of sectors on Bank 1 XX = 0F (models 01, 02, 21, 22) XX = 17 (models 31, 32) XX = 27 (models 41, 42)
59h	B2h	00XXh	Bank 2 Region Information - Number of sectors in Bank 2 XX = 18 (models 01, 02) XX = 38 (models 21, 22) XX = 30 (models 31, 32) XX = 20 (models 41, 42)
5Ah	B4h	00XXh	Bank 3 Region Information - Number of sectors in Bank 3 XX = 18 (models 01, 02) XX = 00 (all other models)
5Bh	B6h	00XXh	Bank 4 Region Information - Number of sectors in Bank 4 XX = 08 (models 01, 02) XX = 00 (all other models)

10. Command Definitions

Writing specific address and data sequences into the command register initiates device operations. Table 13 on page 35 defines the valid register command sequences. *Writing incorrect address and data values or writing them in the improper sequence may place the device in an unknown state. A hardware reset may be required to return the device to reading array data.*

All addresses are latched on the falling edge of WE# or CE#, whichever happens later. All data is latched on the rising edge of WE# or CE#, whichever happens first. Refer to Section 17. AC Characteristics on page 48 for timing diagrams.

10.1 Reading Array Data

The device is automatically set to reading array data after device power-up. No commands are required to retrieve data. Each bank is ready to read array data after completing an Embedded Program or Embedded Erase algorithm.

After the device accepts an Erase Suspend command, the corresponding bank enters the erase-suspend-read mode, after which the system can read data from any non-erase-suspended sector within the same bank. The system can read array data using the standard read timing, except that if it reads at an address within erase-suspended sectors, the device outputs status data. After completing a programming operation in the Erase Suspend mode, the system may once again read array data with the same exception. See Section 10.8 Erase Suspend/Erase Resume Commands on page 35 for more information.

The system *must* issue the reset command to return a bank to the read (or erase-suspend-read) mode if DQ5 goes high during an active program or erase operation, or if the bank is in the autoselect mode. See Section 10.2 Reset Command on page 30, for more information.

See also Section 8.2 Requirements for Reading Array Data on page 13 for more information. Section 17.1 Read-Only Operations on page 48 provides the read parameters, and Figure 12 on page 48 shows the timing diagram.

10.2 Reset Command

Writing the reset command resets the banks to the read or erase-suspend-read mode.

The reset command may be written between the sequence cycles in an erase command sequence before erasing begins. This resets the bank to which the system was writing to the read mode. Once erasure begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in a program command sequence before programming begins. This resets the bank to which the system was writing to the read mode. If the program command sequence is written to a bank that is in the Erase Suspend mode, writing the reset command returns that bank to the erase-suspend-read mode. Once programming begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in an autoselect command sequence. Once in the autoselect mode, the reset command must be written to return to the read mode. If a bank entered the autoselect mode while in the Erase Suspend mode, writing the reset command returns that bank to the erase-suspend-read mode.

If DQ5 goes high during a program or erase operation, writing the reset command returns the bank to the read mode (or erase-suspend-read mode if that bank was in Erase Suspend). Please note that the RY/BY# signal remains low until this reset is issued.

10.3 Autoselect Command Sequence

The autoselect command sequence allows the host system to access the manufacturer and device codes, and determine whether or not a sector is protected. The autoselect command sequence may be written to an address within a bank that is either in the read or erase-suspend-read mode. The autoselect command may not be written while the device is actively programming or erasing in another bank.

The autoselect command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle that contains the bank address and the autoselect command. The bank then enters the autoselect mode. The system may read any number of autoselect codes without reinitiating the command sequence.

Table 13 on page 35 shows the address and data requirements. To determine sector protection information, the system must write to the appropriate bank address (BA) and sector address (SA). Table 3 on page 16 and Table 4 on page 18 show the address range and bank number associated with each sector.

The system must write the reset command to return to the read mode (or erase-suspend-read mode if the bank was previously in Erase Suspend).

10.4 Enter Secured Silicon Region/Exit Secured Silicon Region Command Sequence

The system can access the Secured Silicon Region region by issuing the three-cycle Enter Secured Silicon Region command sequence. The device continues to access the Secured Silicon Region until the system issues the four-cycle Exit Secured Silicon Region command sequence. The Exit Secured Silicon Region command sequence returns the device to normal operation. The Secured Silicon Region is not accessible when the device is executing an Embedded Program or embedded Erase algorithm. Table 13 on page 35 shows the address and data requirements for both command sequences. See also Section 8.13 Secured Silicon Region on page 25 for further information. *Note that the ACC function and unlock bypass modes are not available when the Secured Silicon Region is enabled.*

10.5 Byte/Word Program Command Sequence

The system may program the device by word or byte, depending on the state of the BYTE# pin. Programming is a four-bus-cycle operation. The program command sequence is initiated by writing two unlock write cycles, followed by the program set-up command. The program address and data are written next, which in turn initiate the Embedded Program algorithm. The system is *not* required to provide further controls or timings. The device automatically provides internally generated program pulses and verifies the programmed cell margin. Table 13 on page 35 shows the address and data requirements for the byte program command sequence.

When the Embedded Program algorithm is complete, that bank then returns to the read mode and addresses are no longer latched. The system can determine the status of the program operation by using DQ7, DQ6, or RY/BY#. Refer to Section 11. Write Operation Status on page 37 for information on these status bits.

Any commands written to the device during the Embedded Program Algorithm are ignored. *Note that a* ***hardware reset*** *immediately terminates the program operation.* The program command sequence should be reinitiated once that bank has returned to the read mode, to ensure data integrity. *Note that the Secured Silicon Region, autoselect, and CFI functions are unavailable when a program operation is in progress.*

Programming is allowed in any sequence and across sector boundaries. **A bit cannot be programmed from “0” back to a “1.”** Attempting to do so may cause that bank to set DQ5 = 1, or cause the DQ7 and DQ6 status bits to indicate the operation was successful. However, a succeeding read will show that the data is still “0.” Only erase operations can convert a “0” to a “1.”

10.5.1 Unlock Bypass Command Sequence

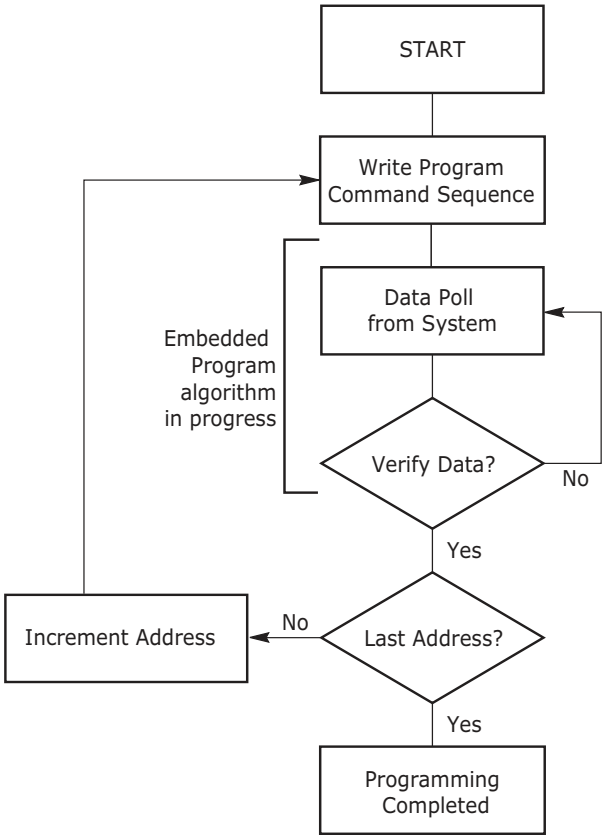
The unlock bypass feature allows the system to program bytes or words to a bank faster than using the standard program command sequence. The unlock bypass command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle containing the unlock bypass command, 20h. That bank then enters the unlock bypass mode. A two-cycle unlock bypass program command sequence is all that is required to program in this mode. The first cycle in this sequence contains the unlock bypass program command, A0h; the second cycle contains the program address and data. Additional data is programmed in the same manner. This mode dispenses with the initial two unlock cycles required in the standard program command sequence, resulting in faster total programming time. Table 13 on page 35 shows the requirements for the command sequence.

During the unlock bypass mode, only the Unlock Bypass Program and Unlock Bypass Reset commands are valid. To exit the unlock bypass mode, the system must issue the two-cycle unlock bypass reset command sequence (see Table 13).

The device offers accelerated program operations through the WP#/ACC pin. When the system asserts V_{HH} on the WP#/ACC pin, the device automatically enters the Unlock Bypass mode. The system may then write the two-cycle Unlock Bypass program command sequence. The device uses the higher voltage on the WP#/ACC pin to accelerate the operation. *Note that the WP#/ACC pin must not be at V_{HH} for any operation other than accelerated programming, or device damage may result. In addition, the WP#/ACC pin must not be left floating or unconnected; inconsistent behavior of the device may result.*

Figure 4 illustrates the algorithm for the program operation. Refer to Section 17.4 Erase and Program Operations on page 51 for parameters, and Figure 14 for timing diagrams.

Figure 4. Program Operation



Note
7. See Table 13 on page 35 for program command sequence.

10.6 Chip Erase Command Sequence

Chip erase is a six bus cycle operation. The chip erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock write cycles are then followed by the chip erase command, which in turn invokes the Embedded Erase algorithm. The device does *not* require the system to preprogram prior to erase. The Embedded Erase algorithm automatically preprograms and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations. Table 13 on page 35 shows the address and data requirements for the chip erase command sequence.

When the Embedded Erase algorithm is complete, that bank returns to the read mode and addresses are no longer latched. The system can determine the status of the erase operation by using DQ7, DQ6, DQ2, or RY/BY#. Refer to Section 11. Write Operation Status on page 37 for information on these status bits.

Any commands written during the chip erase operation are ignored. However, note that a **hardware reset** immediately terminates the erase operation. If that occurs, the chip erase command sequence should be reinitiated once that bank has returned to reading array data, to ensure data integrity. *Note that the Secured Silicon Region, autoselect, and CFI functions are unavailable when an erase operation is in progress.*

Figure 5 on page 34 illustrates the algorithm for the erase operation. Refer to Section 17.4 Erase and Program Operations on page 51 for parameters, and Figure 16 on page 53 for timing diagrams.

10.7 Sector Erase Command Sequence

Sector erase is a six bus cycle operation. The sector erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock cycles are written, and are then followed by the address of the sector to be erased, and the sector erase command. Table 13 on page 35 shows the address and data requirements for the sector erase command sequence.

The device does *not* require the system to preprogram prior to erase. The Embedded Erase algorithm automatically programs and verifies the entire sector for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations.

After the command sequence is written, a sector erase time-out of 50 µs occurs. During the time-out period, additional sector addresses and sector erase commands may be written. However, these additional erase commands are only one bus cycle long and should be identical to the sixth cycle of the standard erase command explained above. Loading the sector erase buffer may be done in any sequence, and the number of sectors may be from one sector to all sectors. The time between these additional cycles must be less than 50 µs, otherwise erasure may begin. Any sector erase address and command following the exceeded time-out may or may not be accepted. It is recommended that processor interrupts be disabled during this time to ensure all commands are accepted. The interrupts can be re-enabled after the last Sector Erase command is written. **If any command other than 30h, B0h, F0h is input during the time-out period, the normal operation will not be guaranteed.** The system must rewrite the command sequence and any additional addresses and commands.

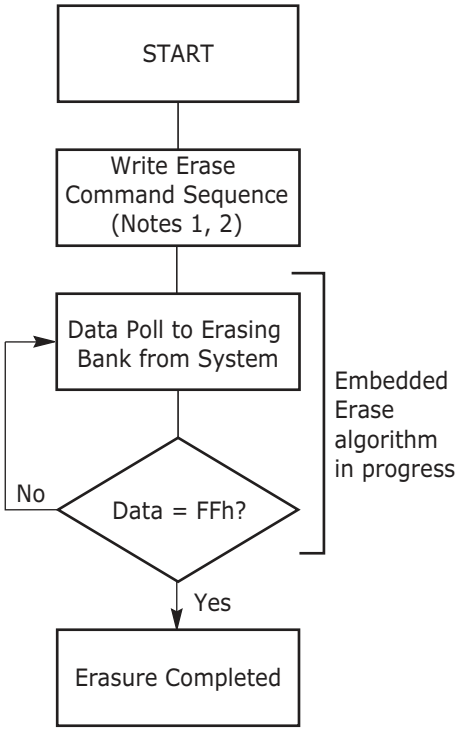
The system can monitor DQ3 to determine if the sector erase timer has timed out (See Section 11.7 DQ3: Sector Erase Timer on page 42.). The time-out begins from the rising edge of the final WE# or CE# pulse (first rising edge) in the command sequence.

When the Embedded Erase algorithm is complete, the bank returns to reading array data and addresses are no longer latched. *Note that while the Embedded Erase operation is in progress, the system can read data from the non-erasing bank.* The system can determine the status of the erase operation by reading DQ7, DQ6, DQ2, or RY/BY# in the erasing bank. Refer to Section 11. Write Operation Status on page 37 for information on these status bits.

Once the sector erase operation has begun, only the Erase Suspend command is valid. All other commands are ignored. However, note that a **hardware reset** immediately terminates the erase operation. If that occurs, the sector erase command sequence should be reinitiated once that bank has returned to reading array data, to ensure data integrity. *Note that the Secured Silicon Region, autoselect, and CFI functions are unavailable when an erase operation is in progress.*

Figure 5 on page 34 illustrates the algorithm for the erase operation. Refer to Section 17.4 Erase and Program Operations on page 51 for parameters, and Figure 16 on page 53 for timing diagrams.

Figure 5. Erase Operation



Notes
8. See Table 13 on page 35 for erase command sequence.
9. See Section 11.7 DQ3: Sector Erase Timer on page 42 for information on the sector erase timer.

10.8 Erase Suspend/Erase Resume Commands

The Erase Suspend command, B0h, allows the system to interrupt a sector erase operation and then read data from, or program data to, any sector not selected for erasure. The bank address is required when writing this command. This command is valid only during the sector erase operation, including the 50 µs time-out period during the sector erase command sequence. The Erase Suspend command is ignored if written during the chip erase operation or Embedded Program algorithm. The bank address must contain one of the sectors currently selected for erase.

When the Erase Suspend command is written during the sector erase operation, the device requires a maximum of 35 µs to suspend the erase operation. However, when the Erase Suspend command is written during the sector erase time-out, the device immediately terminates the time-out period and suspends the erase operation.

After the erase operation has been suspended, the bank enters the erase-suspend-read mode. The system can read data from or program data to any sector not selected for erasure. (The device “erase suspends” all sectors selected for erasure.) It is not recommended to program the Secured Silicon Region after an erase suspend, as proper device functionality cannot be guaranteed. Reading at any address within erase-suspended sectors produces status information on DQ7–DQ0. The system can use DQ7, or DQ6 and DQ2 together, to determine if a sector is actively erasing or is erase-suspended. Refer to Section 11. Write Operation Status on page 37 for information on these status bits.

After an erase-suspended program operation is complete, the bank returns to the erase-suspend-read mode. The system can determine the status of the program operation using the DQ7 or DQ6 status bits, just as in the standard Byte Program operation. Refer to Section 11. Write Operation Status on page 37 for more information.

In the erase-suspend-read mode, the system can also issue the autoselect command sequence. The device allows reading autoselect codes even at addresses within erasing sectors, since the codes are not stored in the memory array. When the device exits the autoselect mode, the device reverts to the Erase Suspend mode, and is ready for another valid operation. Refer to Section 8.9 Autoselect Mode on page 20 and Section 10.3 Autoselect Command Sequence on page 31 for details.

To resume the sector erase operation, the system must write the Erase Resume command. The bank address of the erase-suspended bank is required when writing this command. Further writes of the Resume command are ignored. Another Erase Suspend command can be written after the chip has resumed erasing.

Table 13. S29JL032J Command Definitions

Command Sequence[10]			Cycles	Bus Cycles (Notes 11–14)											
				First		Second		Third		Fourth		Fifth		Sixth	
				Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read[15]			1	RA	RD										
Reset[16]			1	XXX	F0										
Autoselect [17]	Manufacturer ID	Word	4	555	AA	2AA	55	(BA)555	90	(BA)X00	01				
		Byte		AAA		555		(BA)AAA							
	Device ID[18]	Word	6	555	AA	2AA	55	(BA)555	90	(BA)X01	See Table 5	(BA)X0E	See Table 5	(BA)X0F	See Table 5
		Byte		AAA		555		(BA)AAA		(BA)X02		(BA)X1C		(BA)X1E	
	Secured Silicon Region Factory Protect[10]	Word	4	555	AA	2AA	55	(BA)555	90	(BA)X03	82/02				
		Byte		AAA		555		(BA)AAA		(BA)X06					
	Boot Sector/Sector Block Protect Verify[10]	Word	4	555	AA	2AA	55	(BA)555	90	(SA)X02	00/01				
		Byte		AAA		555		(BA)AAA		(SA)X04					
Enter Secured Silicon Region		Word	3	555	AA	2AA	55	555	88						
		Byte		AAA		555		AAA							
Exit Secured Silicon Region		Word	4	555	AA	2AA	55	555	90	XXX	00				
		Byte		AAA		555		AAA							
Program		Word	4	555	AA	2AA	55	555	A0	PA	PD				
		Byte		AAA		555		AAA							
Unlock Bypass		Word	3	555	AA	2AA	55	555	20						
		Byte		AAA		555		AAA							
Unlock Bypass Program[21]			2	XXX	A0	PA	PD								
Unlock Bypass Reset[22]			2	XXX	90	XXX	00								

Table 13. S29JL032J Command Definitions (Continued)

Command Sequence[10]		Cycles	Bus Cycles (Notes 11–14)											
			First		Second		Third		Fourth		Fifth		Sixth	
			Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Chip Erase	Word	6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10
	Byte		AAA		555		AAA		AAA		555		AAA	
Sector Erase[26]	Word	6	555	AA	2AA	55	555	80	555	AA	2AA	55	SA	30
	Byte		AAA		555		AAA		AAA		555			
Erase Suspend[23]		1	BA	B0										
Erase Resume[24]		1	BA	30										
CFI Query[25]	Word	1	55	98										
	Byte		AA											

Legend:

X = Don't care

RA = Address of the memory location to be read.

RD = Data read from location RA during read operation.

PA = Address of the memory location to be programmed. Addresses latch on the falling edge of the WE# or CE# pulse, whichever happens later.

PD = Data to be programmed at location PA. Data latches on the rising edge of WE# or CE# pulse, whichever happens first.

SA = Address of the sector to be verified (in autoselect mode) or erased. Address bits A20–A12 uniquely select any sector. Refer to Table 3 on page 16 and Table 4 on page 18 for information on sector addresses.

BA = Address of the bank that is being switched to autoselect mode, is in bypass mode, or is being erased. A20–A18 uniquely select a bank.

Notes

10. See Table 1 on page 12 for description of bus operations.
11. All values are in hexadecimal.
12. Except for the read cycle and the fourth, fifth, and sixth cycle of the autoselect command sequence, all bus cycles are write cycles.
13. Data bits DQ15–DQ8 are don't care in command sequences, except for RD and PD.
14. Unless otherwise noted, address bits A20–A11 are don't cares for unlock and command cycles, unless SA or PA is required.
15. No unlock or command cycles required when bank is reading array data.
16. The Reset command is required to return to the read mode (or to the erase-suspend-read mode if previously in Erase Suspend) when a bank is in the autoselect mode, or if DQ5 goes high (while the bank is providing status information).
17. The fourth cycle of the autoselect command sequence is a read cycle. The system must provide the bank address to obtain the manufacturer ID, device ID, or Secured Silicon Region factory protect information. Data bits DQ15–DQ8 are don't care. While reading the autoselect addresses, the bank address must be the same until a reset command is given. See Section 10.3 Autoselect Command Sequence on page 31 for more information.
18. For models 01, 02, the device ID must be read across the fourth, fifth, and sixth cycles.
19. The data is 82h for factory locked, 42h for customer locked, and 02h for not factory/customer locked.
20. The data is 00h for an unprotected sector/sector block and 01h for a protected sector/sector block.
21. The Unlock Bypass command is required prior to the Unlock Bypass Program command.
22. The Unlock Bypass Reset command is required to return to the read mode when the bank is in the unlock bypass mode.
23. The system may read and program in non-erasing sectors, or enter the autoselect mode, when in the Erase Suspend mode. The Erase Suspend command is valid only during a sector erase operation, and requires the bank address.
24. The Erase Resume command is valid only during the Erase Suspend mode, and requires the bank address.
25. Command is valid when device is ready to read array data or when device is in autoselect mode.
26. Additional sector erase commands during the time-out period after an initial sector erase are one cycle long and identical to the sixth cycle of the sector erase command sequence (SA / 30).

11. Write Operation Status

The device provides several bits to determine the status of a program or erase operation: DQ2, DQ3, DQ5, DQ6, and DQ7. Table 14 on page 42 and the following subsections describe the function of these bits. DQ7 and DQ6 each offer a method for determining whether a program or erase operation is complete or in progress. The device also provides a hardware-based output signal, RY/BY#, to determine whether an Embedded Program or Erase operation is in progress or has been completed.

11.1 DQ7: Data# Polling

The Data# Polling bit, DQ7, indicates to the host system whether an Embedded Program or Erase algorithm is in progress or completed, or whether a bank is in Erase Suspend. Data# Polling is valid after the rising edge of the final WE# pulse in the command sequence.

During the Embedded Program algorithm, the device outputs on DQ7 the complement of the datum programmed to DQ7. This DQ7 status also applies to programming during Erase Suspend. When the Embedded Program algorithm is complete, the device outputs the datum programmed to DQ7. The system must provide the program address to read valid status information on DQ7. If a program address falls within a protected sector, Data# Polling on DQ7 is active for approximately 1 µs, then that bank returns to the read mode.

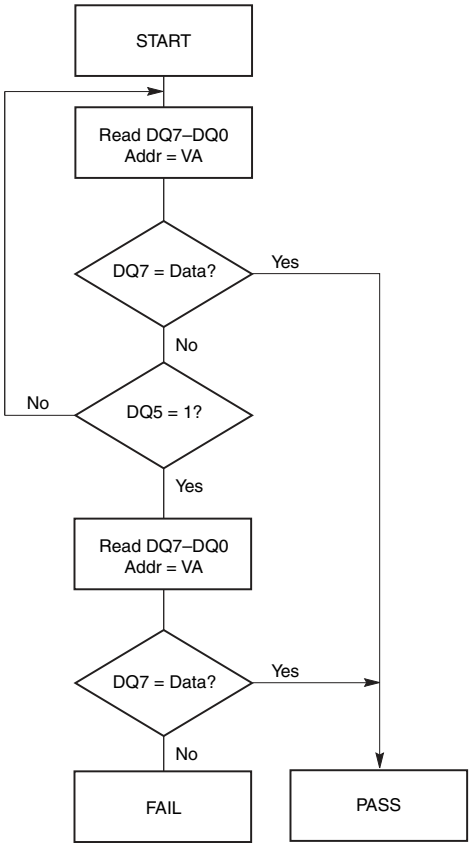
During the Embedded Erase algorithm, Data# Polling produces a “0” on DQ7. When the Embedded Erase algorithm is complete, or if the bank enters the Erase Suspend mode, Data# Polling produces a “1” on DQ7. The system must provide an address within any of the sectors selected for erasure to read valid status information on DQ7.

After an erase command sequence is written, if all sectors selected for erasing are protected, Data# Polling on DQ7 is active for approximately 3 ms, then the bank returns to the read mode. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected. However, if the system reads DQ7 at an address within a protected sector, the status may not be valid.

When the system detects DQ7 has changed from the complement to true data, it can read valid data at DQ15–DQ0 (or DQ7–DQ0 for x8-only device) on the *following* read cycles. Just prior to the completion of an Embedded Program or Erase operation, DQ7 may change asynchronously with DQ15–DQ8 (DQ7–DQ0 for x8-only device) while Output Enable (OE#) is asserted low. That is, the device may change from providing status information to valid data on DQ7. Depending on when the system samples the DQ7 output, it may read the status or valid data. Even if the device has completed the program or erase operation and DQ7 has valid data, the data outputs on DQ15–DQ0 may be still invalid. Valid data on DQ15–DQ0 (or DQ7–DQ0 for x8-only device) will appear on successive read cycles.

Table 14 shows the outputs for Data# Polling on DQ7. Figure 6 on page 38 shows the Data# Polling algorithm. Figure 18 on page 54 shows the Data# Polling timing diagram.

Figure 6. Data# Polling Algorithm[27, 28]



Notes
27. VA = Valid address for programming. During a sector erase operation, a valid address is any sector address within the sector being erased. During chip erase, a valid address is any non-protected sector address.
28. DQ7 should be rechecked even if DQ5 = “1” because DQ7 may change simultaneously with DQ5.

11.2 RY/BY#: Ready/Busy#

The RY/BY# is a dedicated, open-drain output pin which indicates whether an Embedded Algorithm is in progress or complete. The RY/BY# status is valid after the rising edge of the final WE# pulse in the command sequence. Since RY/BY# is an open-drain output, several RY/BY# pins can be tied together in parallel with a pull-up resistor to V_{CC}.

If the output is low (Busy), the device is actively erasing or programming. (This includes programming in the Erase Suspend mode.) If the output is high (Ready), the device is in the read mode, the standby mode, or one of the banks is in the erase-suspend-read mode.

Table 14 on page 42 shows the outputs for RY/BY#. When DQ5 is set to “1”, RY/BY# will be in the BUSY state, or “0”.

11.3 DQ6: Toggle Bit I

Toggle Bit I on DQ6 indicates whether an Embedded Program or Erase algorithm is in progress or complete, or whether the device has entered the Erase Suspend mode. Toggle Bit I may be read at any address, and is valid after the rising edge of the final WE# pulse in the command sequence (prior to the program or erase operation), and during the sector erase time-out.

During an Embedded Program or Erase algorithm operation, successive read cycles to any address cause DQ6 to toggle. The system may use either OE# or CE# to control the read cycles. When the operation is complete, DQ6 stops toggling.

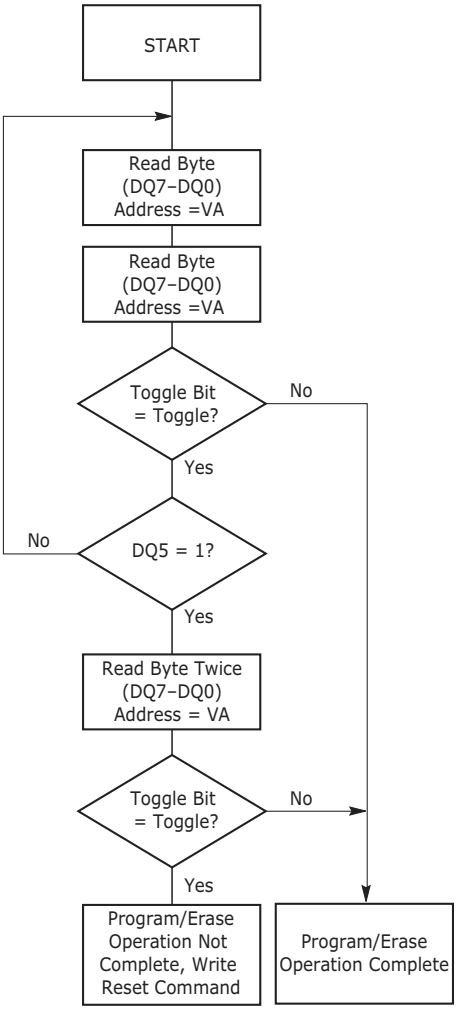
After an erase command sequence is written, if all sectors selected for erasing are protected, DQ6 toggles for approximately 3 ms, then returns to reading array data. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

The system can use DQ6 and DQ2 together to determine whether a sector is actively erasing or is erase-suspended. When the device is actively erasing (that is, the Embedded Erase algorithm is in progress), DQ6 toggles. When the device enters the Erase Suspend mode, DQ6 stops toggling. However, the system must also use DQ2 to determine which sectors are erasing or erase-suspended. Alternatively, the system can use DQ7 (see Section 11.1 DQ7: Data# Polling on page 37).

If a program address falls within a protected sector, DQ6 toggles for approximately 1 µs after the program command sequence is written, then returns to reading array data.

DQ6 also toggles during the erase-suspend-program mode, and stops toggling once the Embedded Program algorithm is complete.

Figure 7. Toggle Bit Algorithm[29]



11.4 DQ2: Toggle Bit II

The “Toggle Bit II” on DQ2, when used with DQ6, indicates whether a particular sector is actively erasing (that is, the Embedded Erase algorithm is in progress), or whether that sector is erase-suspended. Toggle Bit II is valid after the rising edge of the final WE# pulse in the command sequence.

DQ2 toggles when the system reads at addresses within those sectors that have been selected for erasure. (The system may use either OE# or CE# to control the read cycles.) But DQ2 cannot distinguish whether the sector is actively erasing or is erase-suspended. DQ6, by comparison, indicates whether the device is actively erasing, or is in Erase Suspend, but cannot distinguish which sectors are selected for erasure. Thus, both status bits are required for sector and mode information. Refer to Table 14 on page 42 to compare outputs for DQ2 and DQ6.

Figure 7 on page 40 shows the toggle bit algorithm in flowchart form, and Section 11.4 DQ2: Toggle Bit II on page 40 explains the algorithm. See also Section 11.3 DQ6: Toggle Bit I on page 39. Figure 19 on page 54 shows the toggle bit timing diagram. Figure 20 on page 55 shows the differences between DQ2 and DQ6 in graphical form.

Note
29. The system should recheck the toggle bit even if DQ5 = “1” because the toggle bit may stop toggling as DQ5 changes to “1.” See the subsections on DQ6 and DQ2 for more information.

11.5 Reading Toggle Bits DQ6/DQ2

Refer to Figure 7 on page 40 for the following discussion. Whenever the system initially begins reading toggle bit status, it must read DQ15–DQ0 (or DQ7–DQ0 for x8-only device) at least twice in a row to determine whether a toggle bit is toggling. Typically, the system would note and store the value of the toggle bit after the first read. After the second read, the system would compare the new value of the toggle bit with the first. If the toggle bit is not toggling, the device has completed the program or erase operation. The system can read array data on DQ15–DQ0 (or DQ7–DQ0 for x8-only device) on the following read cycle.

However, if after the initial two read cycles, the system determines that the toggle bit is still toggling, the system also should note whether the value of DQ5 is high (see the section on DQ5). If it is, the system should then determine again whether the toggle bit is toggling, since the toggle bit may have stopped toggling just as DQ5 went high. If the toggle bit is no longer toggling, the device has successfully completed the program or erase operation. If it is still toggling, the device did not completed the operation successfully, and the system must write the reset command to return to reading array data.

The remaining scenario is that the system initially determines that the toggle bit is toggling and DQ5 has not gone high. The system may continue to monitor the toggle bit and DQ5 through successive read cycles, determining the status as described in the previous paragraph. Alternatively, it may choose to perform other system tasks. In this case, the system must start at the beginning of the algorithm when it returns to determine the status of the operation (top of Figure 7).

11.6 DQ5: Exceeded Timing Limits

DQ5 indicates whether the program or erase time has exceeded a specified internal pulse count limit. Under these conditions DQ5 produces a “1,” indicating that the program or erase cycle was not successfully completed.

The device may output a “1” on DQ5 if the system tries to program a “1” to a location that was previously programmed to “0.” **Only an erase operation can change a “0” back to a “1.”** Under this condition, the device halts the operation, and when the timing limit has been exceeded, DQ5 produces a “1.” The
RDY/BSY# pin will be in the BUSY state under this condition.

Under both these conditions, the system must write the reset command to return to the read mode (or to the erase-suspend-read mode if a bank was previously in the erase-suspend-program mode).

11.7 DQ3: Sector Erase Timer

After writing a sector erase command sequence, the system may read DQ3 to determine whether or not erasure has begun. (The sector erase timer does not apply to the chip erase command.) If additional sectors are selected for erasure, the entire time-out also applies after each additional sector erase command. When the time-out period is complete, DQ3 switches from a “0” to a “1.” If the time between additional sector erase commands from the system can be assumed to be less than 50 µs, the system need not monitor DQ3. See also Section 10.7 Sector Erase Command Sequence on page 33.

After the sector erase command is written, the system should read the status of DQ7 (Data# Polling) or DQ6 (Toggle Bit I) to ensure that the device has accepted the command sequence, and then read DQ3. If DQ3 is “1,” the Embedded Erase algorithm has begun; all further commands (except Erase Suspend) are ignored until the erase operation is complete. If DQ3 is “0,” the device will accept additional sector erase commands. To ensure the command has been accepted, the system software should check the status of DQ3 prior to and following each subsequent sector erase command. If DQ3 is high on the second status check, the last command might not have been accepted.

Table 14 shows the status of DQ3 relative to the other status bits.

Table 14. Write Operation Status

Status			DQ7[31]	DQ6	DQ5[30]	DQ3	DQ2[31]	RY/BY#
Standard Mode	Embedded Program Algorithm		DQ7#	Toggle	0	N/A	No toggle	0
	Embedded Erase Algorithm	In busy erasing sector	0	Toggle	0	1	Toggle	0
		In not busy erasing sector	0	Toggle	0	1	No toggle	0
Erase Suspend Mode	Erase-Suspend-Read	Erase Suspended Sector	1	No toggle	0	N/A	Toggle	1
		Non-Erase Suspended Sector	Data	Data	Data	Data	Data	1
	Erase-Suspend-Program		DQ7#	Toggle	0	N/A	N/A	0

Notes

30. DQ5 switches to ‘1’ when an Embedded Program or Embedded Erase operation has exceeded the maximum timing limits. Refer to the section on DQ5 for more information.
31. DQ7 and DQ2 require a valid address when reading status information. Refer to the appropriate subsection for further details.
32. When reading write operation status bits, the system must always provide the bank address where the Embedded Algorithm is in progress. The device outputs array data if the system addresses a non-busy bank.

12. Absolute Maximum Ratings

Storage Temperature, Plastic Packages	–65°C to +150°C
Ambient Temperature with Power Applied	–65°C to +125°C
Voltage with Respect to Ground, V_{CC}[33]	–0.5V to +4.0V
A9 and RESET#[34]	–0.5V to +12.5V
WP#/ACC	–0.5V to +9.5V
All other pins[33]	–0.5V to V_{CC} +0.5V
Output Short Circuit Curren[35]	200 mA

Notes

33. Minimum DC voltage on input or I/O pins is –0.5V. During voltage transitions, input or I/O pins may overshoot V_{SS} to –2.0V for periods of up to 20 ns. Maximum DC voltage on input or I/O pins is V_{CC} +0.5V. See Figure 8 on page 43. During voltage transitions, input or I/O pins may overshoot to V_{CC} +2.0V for periods up to 20 ns. See Figure 9 on page 43.
34. Minimum DC input voltage on pins A9, OE#, RESET#, and WP#/ACC is –0.5V. During voltage transitions, A9, OE#, WP#/ACC, and RESET# may overshoot V_{SS} to –2.0V for periods of up to 20 ns. See Figure 8 on page 43. Maximum DC input voltage on pin A9 is +12.5V which may overshoot to +14.0V for periods up to 20 ns. Maximum DC input voltage on WP#/ACC is +9.5V which may overshoot to +12.0V for periods up to 20 ns.
35. No more than one output may be shorted to ground at a time. Duration of the short circuit should not be greater than one second.
36. Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 8. Maximum Negative Overshoot Waveform

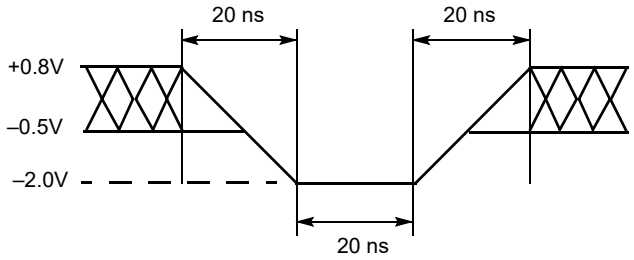
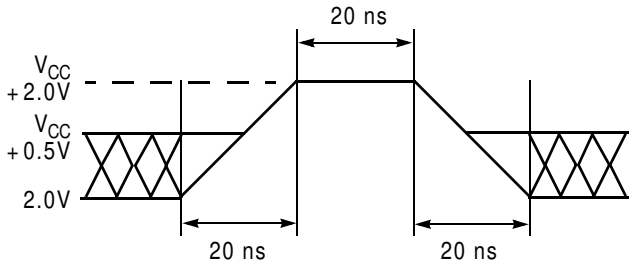


Figure 9. Maximum Positive Overshoot Waveform



13. Operating Ranges

Industrial (I) Devices

Ambient Temperature (T_A) –40°C to +85°C

Automotive (A) Devices

Ambient Temperature (T_A) –40°C to +85°C

V_{CC} Supply Voltages

V_{CC} for standard voltage range 2.7V to 3.6V

Operating ranges define those limits between which the functionality of the device is guaranteed.

14. DC Characteristics

14.1 CMOS Compatible

Parameter Symbol	Parameter Description	Test Conditions		Min	Typ	Max	Unit
I_{LI}	Input Load Current	$V_{IN} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC\ max}$				±1.0	µA
I_{LIT}	A9 and RESET# Input Load Current	$V_{CC} = V_{CC\ max}$, OE# = V_{IH}; A9 or RESET# = 12.5V				35	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC\ max}$, OE# = V_{IH}				±1.0	µA
I_{LR}	Reset Leakage Current	$V_{CC} = V_{CC\ max}$; RESET# = 12.5V				35	µA
I_{CC1}	V_{CC} Active Read Current[14.2, 38]	CE# = V_{IL}, OE# = V_{IH}, Byte Mode	5 MHz		10	16	mA
			1 MHz		2	4	
		CE# = V_{IL}, OE# = V_{IH}, Word Mode	5 MHz		10	16	
			1 MHz		2	4	
I_{CC2}	V_{CC} Active Write Current[38, 39]	CE# = V_{IL}, OE# = V_{IH}, WE# = V_{IL}			15	30	mA
I_{CC3}	V_{CC} Standby Current[38]	CE#, RESET# = V_{CC} ± 0.3V			0.2	5	µA
I_{CC4}	V_{CC} Reset Current[38]	RESET# = V_{SS} ± 0.3V			0.2	5	µA
I_{CC5}	Automatic Sleep Mode[38, 40]	$V_{IH} = V_{CC}$ ± 0.3V; $V_{IL} = V_{SS}$ ± 0.3V			0.2	5	µA
I_{CC6}	V_{CC} Active Read-While-Program Current[38]	CE# = V_{IL}, OE# = V_{IH}, 1 MHz	Byte		21	45	mA
			Word		21	45	
I_{CC7}	V_{CC} Active Read-While-Erase Current[38]	CE# = V_{IL}, OE# = V_{IH}, 1 MHz	Byte		21	45	mA
			Word		21	45	
I_{CC8}	V_{CC} Active Program-While-Erase-Suspended Current[38, 41]	CE# = V_{IL}, OE# = V_{IH}			17	35	mA
V_{IL}	Input Low Voltage			–0.5		0.8	V
V_{IH}	Input High Voltage			0.7 x V_{CC}		V_{CC} + 0.3	V
V_{HH}	Voltage for WP#/ACC Sector Protect/Unprotect and Program Acceleration	V_{CC} = 3.0V ± 10%		8.5		9.5	V
V_{ID}	Voltage for Autoselect and Temporary Sector Unprotect	V_{CC} = 3.0V ± 10%		8.5		12.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.0 mA, $V_{CC} = V_{CC\ min}$				0.45	V

Notes

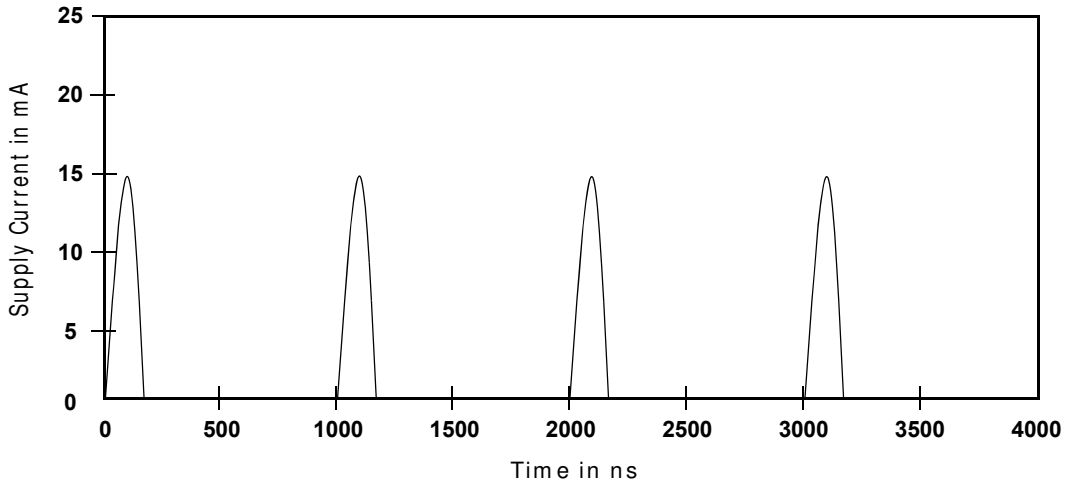
37. The I_{CC} current listed is typically less than 2 mA/MHz, with OE# at V_{IH}.
38. Maximum I_{CC} specifications are tested with $V_{CC} = V_{CC}$max.
39. I_{CC} active while Embedded Erase or Embedded Program is in progress.
40. Automatic sleep mode enables the low power mode when addresses remain stable for t_{ACC} + 30 ns. Typical sleep mode current is 200 nA.
41. Not 100% tested.

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
V_{OH1}	Output High Voltage	I_{OH} = –2.0 mA, V_{CC} = $V_{CC\ min}$	0.85 x V_{CC}			V
V_{OH2}		I_{OH} = –100 µA, V_{CC} = $V_{CC\ min}$	V_{CC}–0.4			
V_{LKO}	Low V_{CC} Lock-Out Voltage[41]		1.8	2.0	2.5	V

Notes
37. The I_{CC} current listed is typically less than 2 mA/MHz, with OE# at V_{IH}.
38. Maximum I_{CC} specifications are tested with V_{CC} = V_{CC}max.
39. I_{CC} active while Embedded Erase or Embedded Program is in progress.
40. Automatic sleep mode enables the low power mode when addresses remain stable for t_{ACC} + 30 ns. Typical sleep mode current is 200 nA.
41. Not 100% tested.

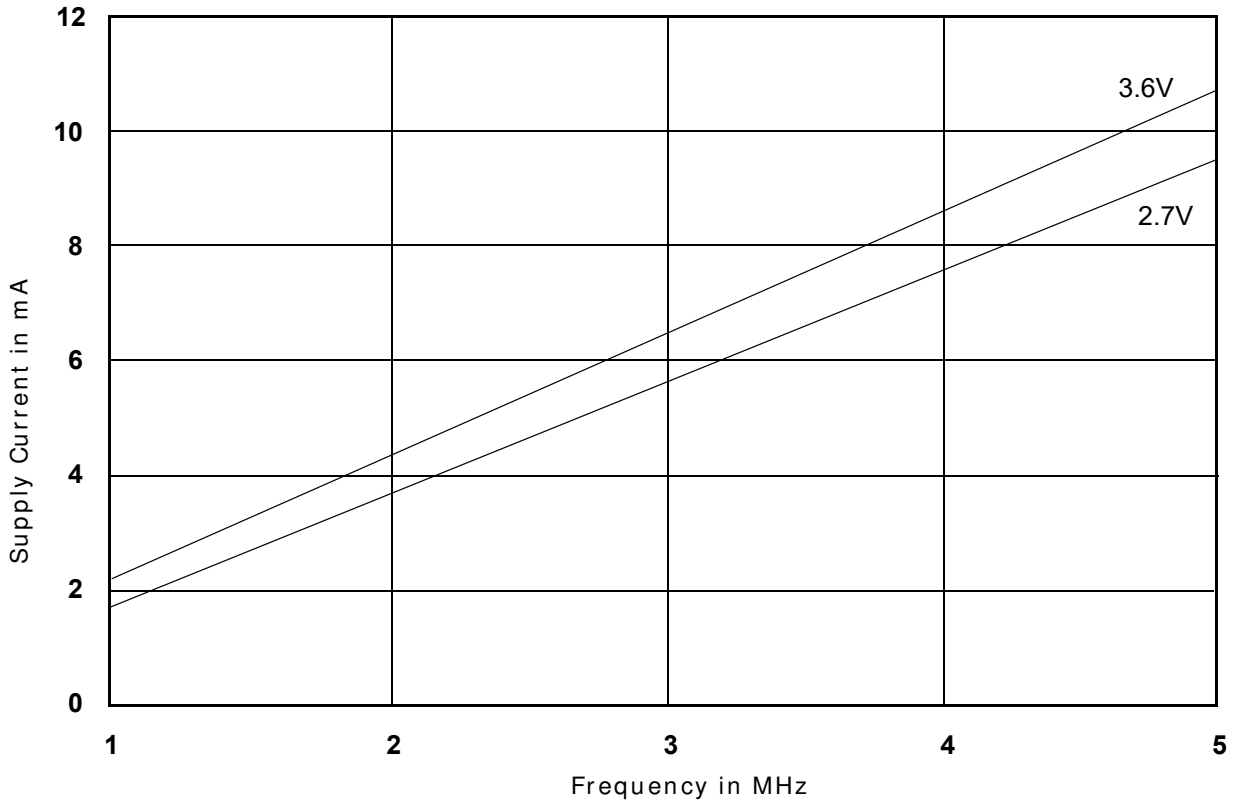
14.2 Zero-Power Flash

Figure 10. I_{CC1} Current vs. Time (Showing Active and Automatic Sleep Currents)[42]



Note
42. Addresses are switching at 1 MHz.

Figure 11. Typical I_{CC1} vs. Frequency[43]



Note
43. T = 25°C

15. Test Conditions

Figure 15.1 Test Setup[44]

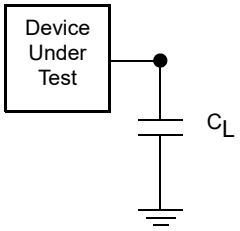


Table 15. Test Specifications

Test Condition	60	70	Unit
Output Load Capacitance, C_L	30	100	pF
Input Rise and Fall Times[44]	5		ns
Input Pulse Levels	0.0 or Vcc		V
Input timing measurement reference levels	0.5 Vcc		V
Output timing measurement reference levels	0.5 Vcc		V

Note
45. Input rise and fall times are 0-100%.

16. Key To Switching Waveforms

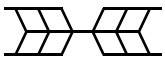
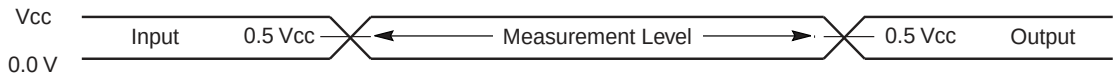
Waveform	Inputs	Outputs
	Steady	
	Changing from H to L	
	Changing from L to H	
	Don’t Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High Impedance State (High-Z)

Figure 16.1 Input Waveforms and Measurement Levels



Note
44. Diodes are IN3064 or equivalent.

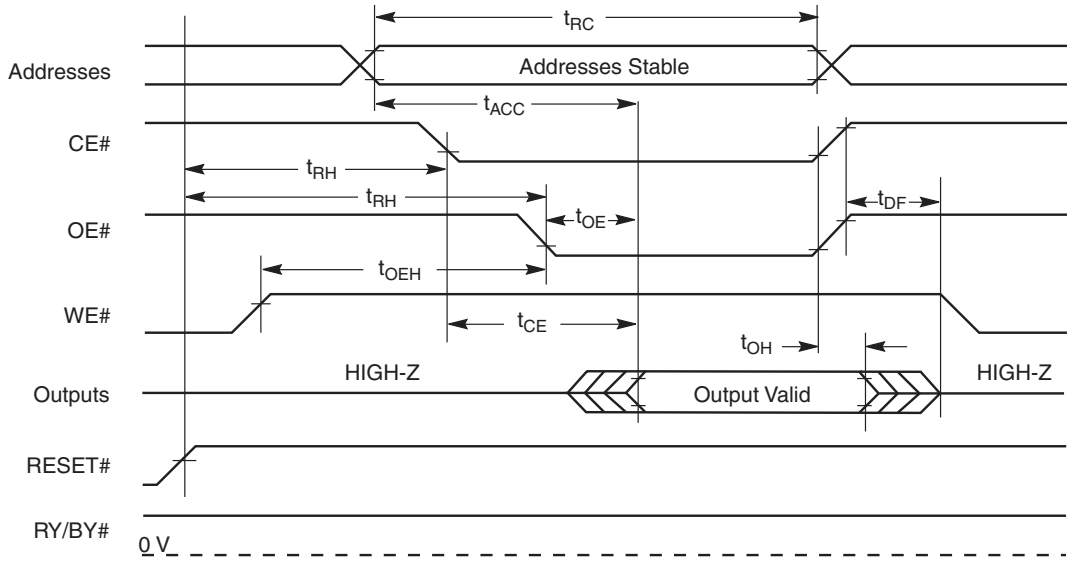
17. AC Characteristics

17.1 Read-Only Operations

Parameter		Description		Test Setup		Speed Options		
JEDEC	Std.					60	70	Unit
t_{AVAV}	t_{RC}	Read Cycle Time[46]			Min	60	70	ns
t_{AVQV}	t_{ACC}	Address to Output Delay		CE#, OE# = V_{IL}	Max	60	70	ns
t_{ELQV}	t_{CE}	Chip Enable to Output Delay		OE# = V_{IL}	Max	60	70	ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay			Max	25	30	ns
t_{EHQZ}	t_{DF}	Chip Enable to Output High-Z[46, 48]			Max	16		ns
t_{GHQZ}	t_{DF}	Output Enable to Output High-Z[46, 48]			Max	16		ns
t_{AXQX}	t_{OH}	Output Hold Time From Addresses, CE# or OE#, Whichever Occurs First			Min	0		ns
	t_{OEH}	Output Enable Hold Time[46]	Read		Min	0		ns
			Toggle and Data# Polling		Min	5	10	ns

Notes
46. Not 100% tested.
47. See Figure 15.1 on page 47 and Table 15 on page 47 for test specifications
48. Measurements performed by placing a 50 ohm termination on the data pin with a bias of $V_{CC}/2$. The time from OE# high to the data bus driven to $V_{CC}/2$ is taken as t_{DF}.

Figure 12. Read Operation Timings

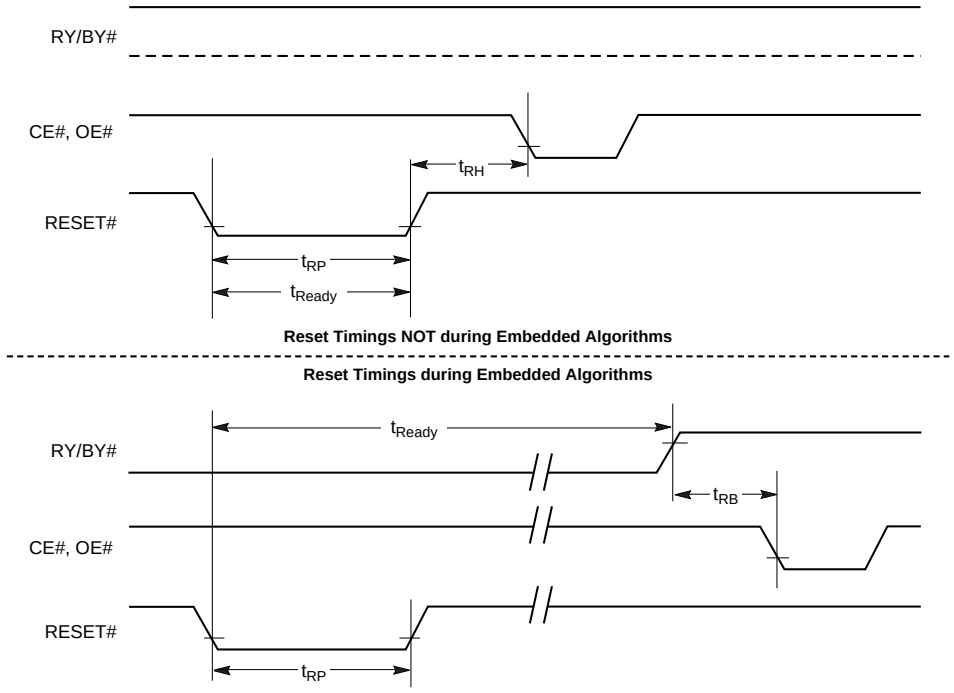


17.2 Hardware Reset (RESET#)

Parameter		Description		All Speed Options	Unit
JEDEC	Std				
	t_{Ready}	RESET# Pin Low (During Embedded Algorithms) to Read Mode[49]	Max	35	µs
	t_{Ready}	RESET# Pin Low (NOT During Embedded Algorithms) to Read Mode[49]	Max	500	ns
	t_{RP}	RESET# Pulse Width	Min	500	ns
	t_{RH}	Reset High Time Before Read[49]	Min	50	ns
	t_{RPD}	RESET# Low to Standby Mode	Min	35	µs
	t_{RB}	RY/BY# Recovery Time	Min	0	ns

Note
49. Not 100% tested.

Figure 13. Reset Timings



17.3 Word/Byte Configuration (BYTE#)

Parameter				Speed Options		
JEDEC	Std.	Description		60	70	Unit
	t_{ELFL}/t_{ELFH}	CE# to BYTE# Switching Low or High	Max	5		ns
	t_{FLQZ}	BYTE# Switching Low to Output HIGH-Z	Max	16		ns
	t_{FHQV}	BYTE# Switching High to Output Active	Max	60	70	ns

Figure 17.1 BYTE# Timings for Read Operations

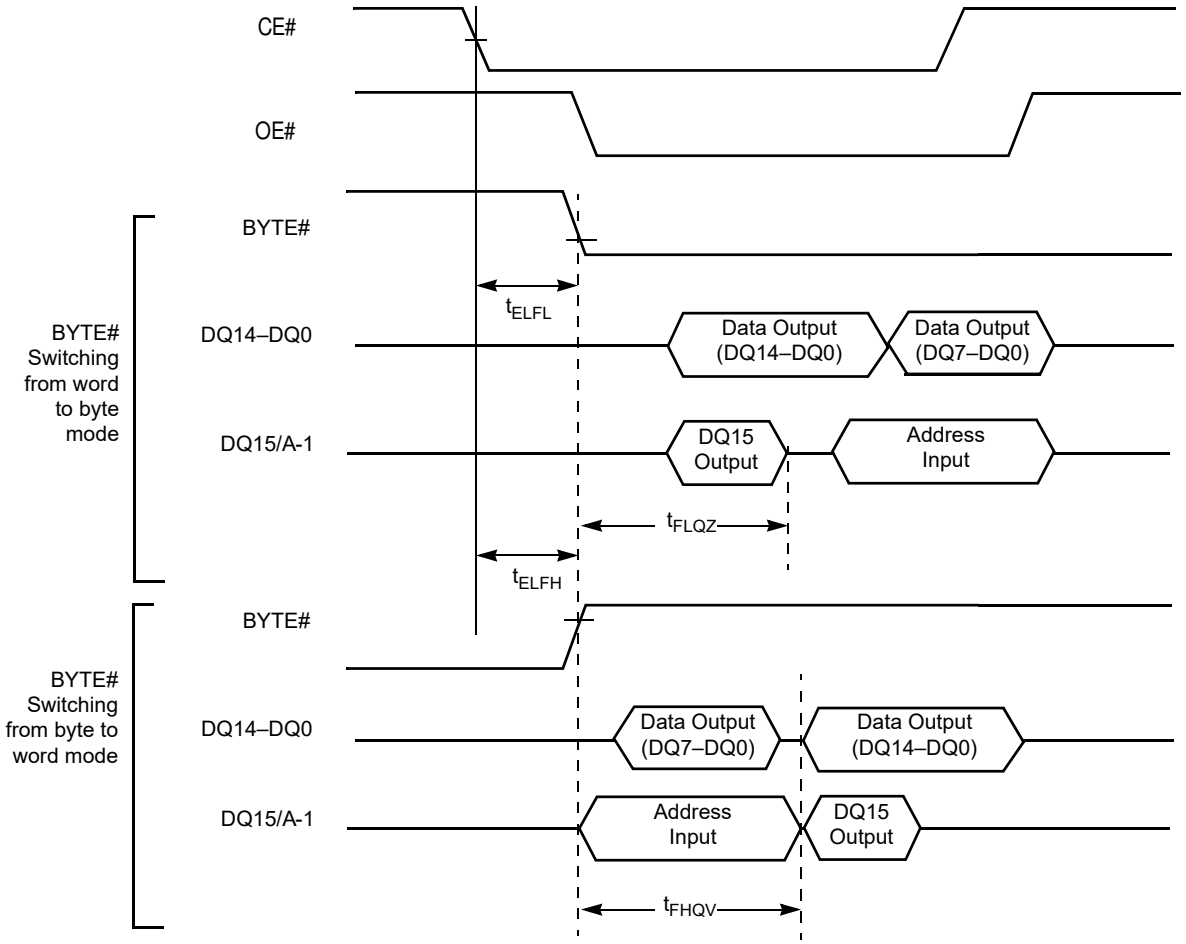
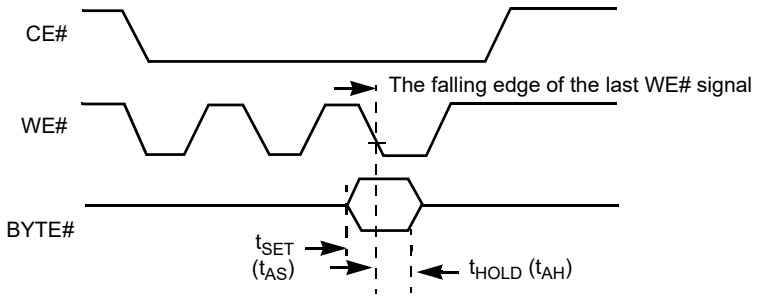


Figure 17.2 BYTE# Timings for Write Operations[50]



17.4 Erase and Program Operations

Parameter		Description			Speed Options		
JEDEC	Std				60	70	Unit
t_{AVAV}	t_{WC}	Write Cycle Time[51]		Min	60	70	ns
t_{AVWL}	t_{AS}	Address Setup Time		Min	0		ns
	t_{ASO}	Address Setup Time to OE# low during toggle bit polling		Min	12		ns
t_{WLAX}	t_{AH}	Address Hold Time		Min	35	35	ns
	t_{AHT}	Address Hold Time From CE# or OE# high during toggle bit polling		Min	0		ns
t_{DVWH}	t_{DS}	Data Setup Time		Min	35	40	ns
t_{WHDX}	t_{DH}	Data Hold Time		Min	0		ns
	t_{OEPH}	Output Enable High during toggle bit polling		Min	20		ns
t_{GHWL}	t_{GHWL}	Read Recovery Time Before Write (OE# High to WE# Low)		Min	0		ns
t_{ELWL}	t_{CS}	CE# Setup Time		Min	0		ns
t_{WHEH}	t_{CH}	CE# Hold Time		Min	0		ns
t_{WLWH}	t_{WP}	Write Pulse Width		Min	25	30	ns
t_{WHDL}	t_{WPH}	Write Pulse Width High		Min	25	30	ns
	$t_{SR/W}$	Latency Between Read and Write Operations		Min	0		ns
t_{WHWH1}	t_{WHWH1}	Programming Operation[52]	Byte	Typ	6		µs
			Word	Typ	6		
t_{WHWH1}	t_{WHWH1}	Accelerated Programming Operation, Byte or Word[52]		Typ	4		µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation[52]		Typ	0.5		sec
	t_{VCS}	V_{CC} Setup Time[51]		Min	50		µs
	t_{RB}	Write Recovery Time from RY/BY#		Min	0		ns
	t_{BUSY}	Program/Erase Valid to RY/BY# Delay		Max	90		ns
	t_{ESL}	Erase Suspend Latency		Max	35		µs

Notes
50. Refer to the table in Section 17.4 Erase and Program Operations on page 51 for t_{AS} and t_{AH} specifications.
51. Not 100% tested.
52. See Section 18. Data Integrity on page 58 for more information.

Figure 14. Program Operation Timings[53, 54]

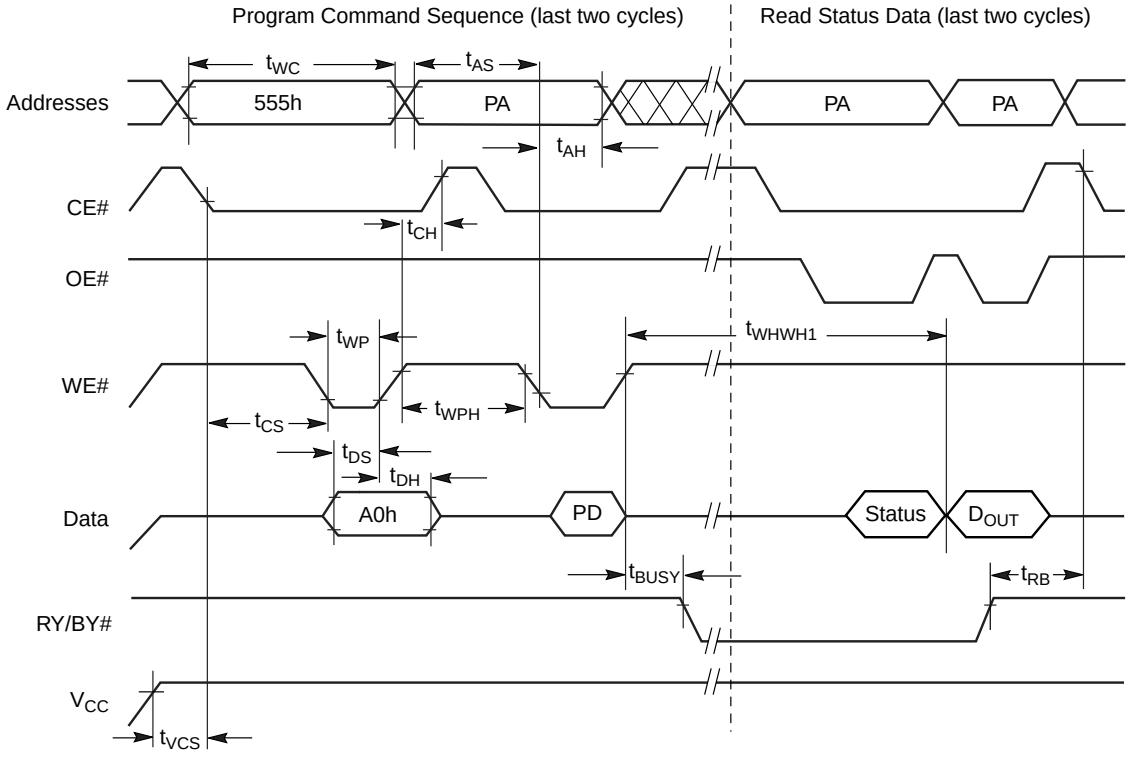
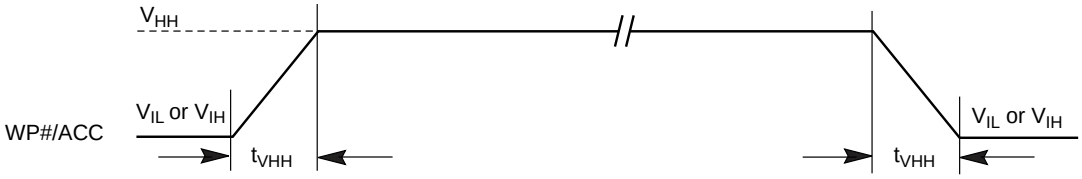


Figure 15. Accelerated Program Timing Diagram



Notes
53. PA = program address, PD = program data, D_{OUT} is the true data at the program address.
54. Illustration shows device in word mode.

Figure 16. Chip/Sector Erase Operation Timings[55, 56]

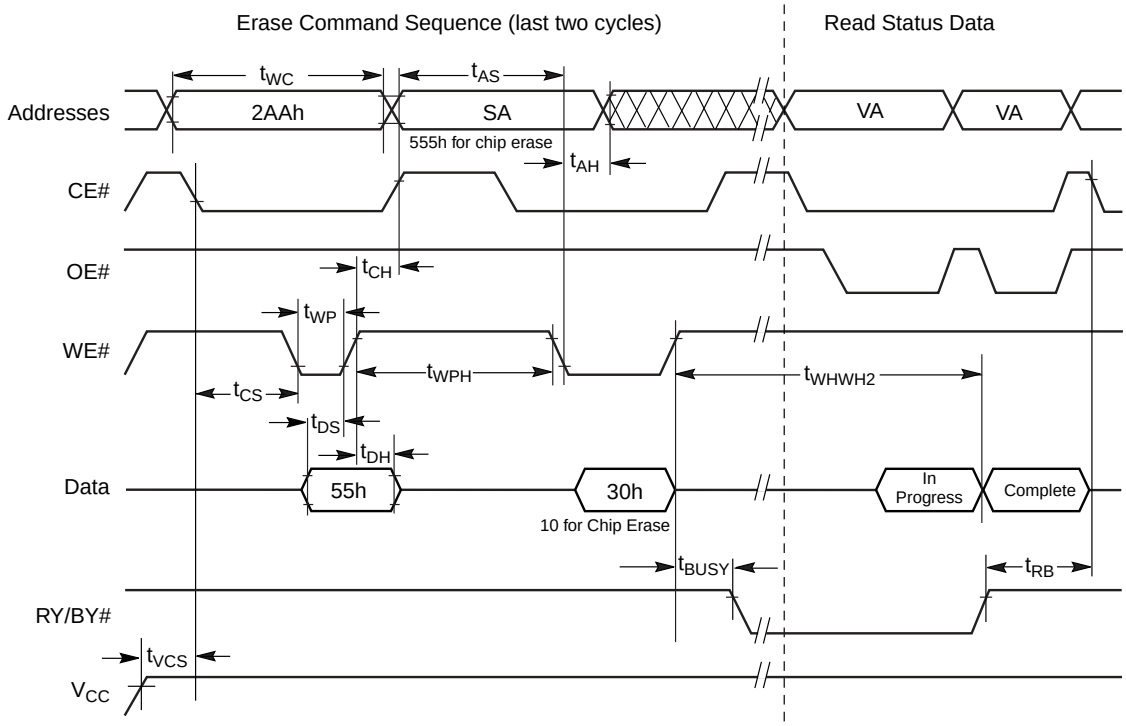
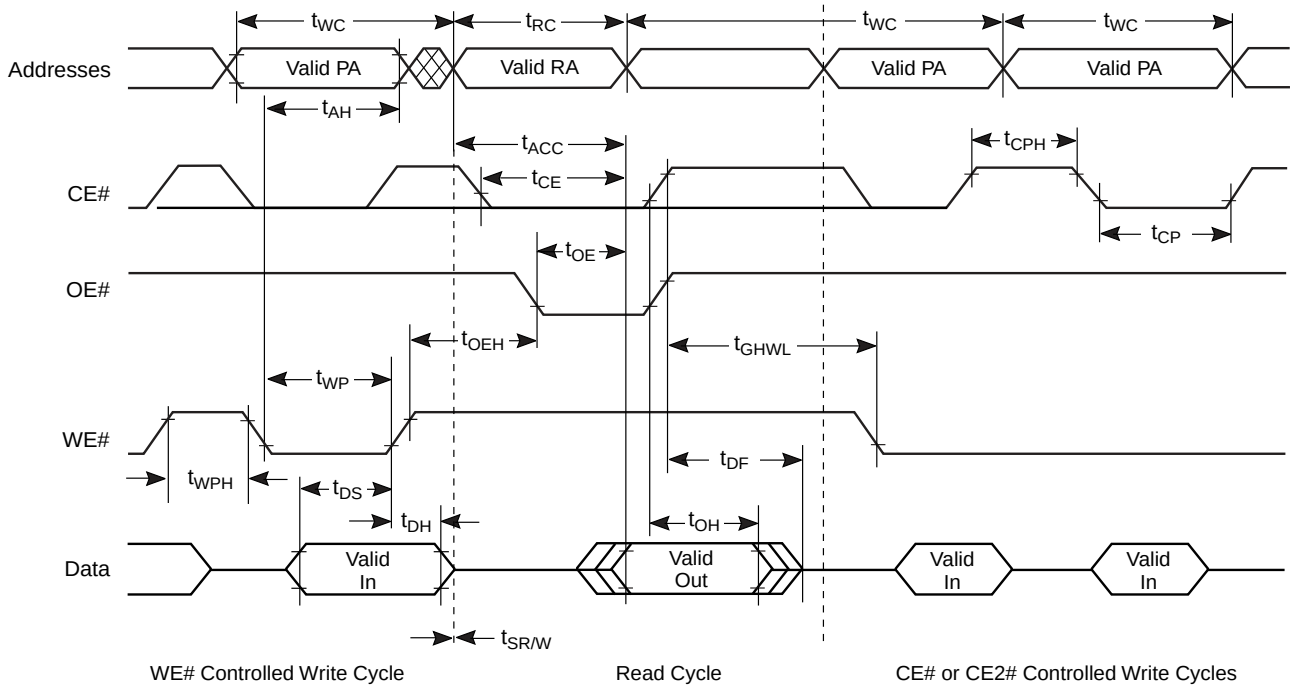


Figure 17. Back-to-back Read/Write Cycle Timings



Notes
55. SA = sector address (for Sector Erase), VA = Valid Address for reading status data (see Section 11. Write Operation Status on page 37).
56. These waveforms are for the word mode.

Figure 18. Data# Polling Timings (During Embedded Algorithms)[57]

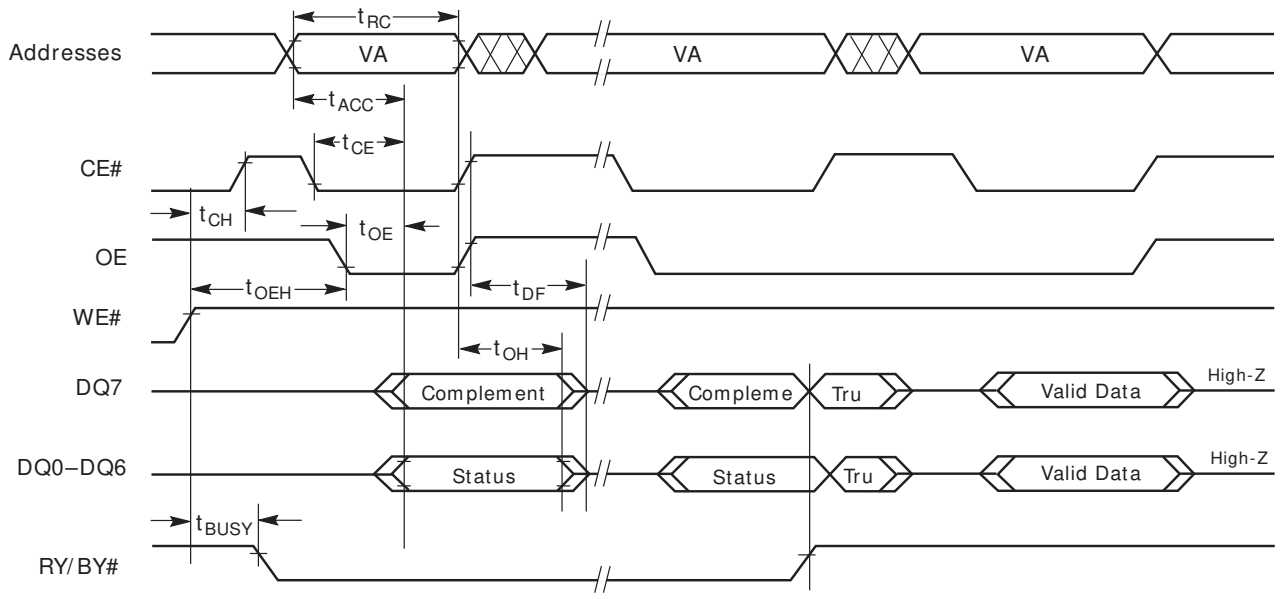
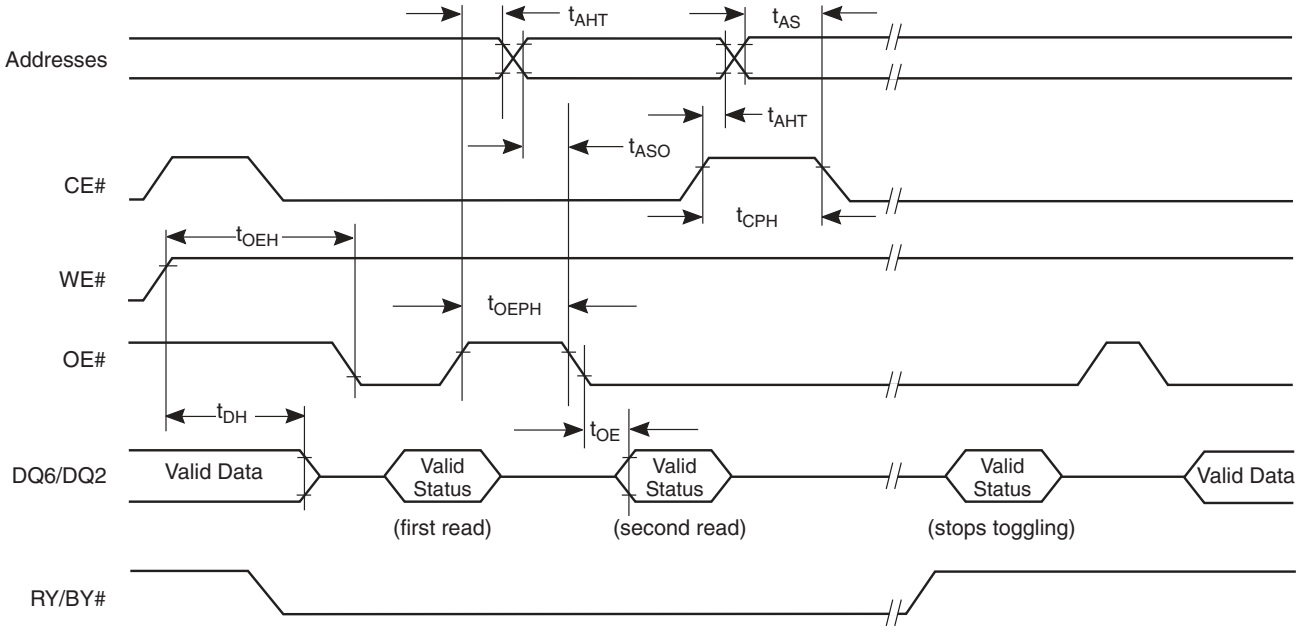
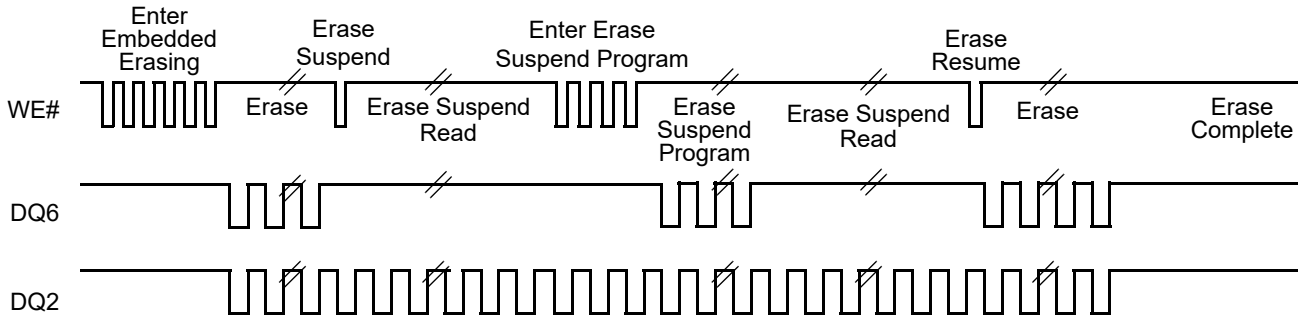


Figure 19. Toggle Bit Timings (During Embedded Algorithms)[58]



Notes
57. VA = Valid address. Illustration shows first status cycle after command sequence, last status read cycle, and array data read cycle.
58. VA = Valid address; not required for DQ6. Illustration shows first two status cycle after command sequence, last status read cycle, and array data read cycle.

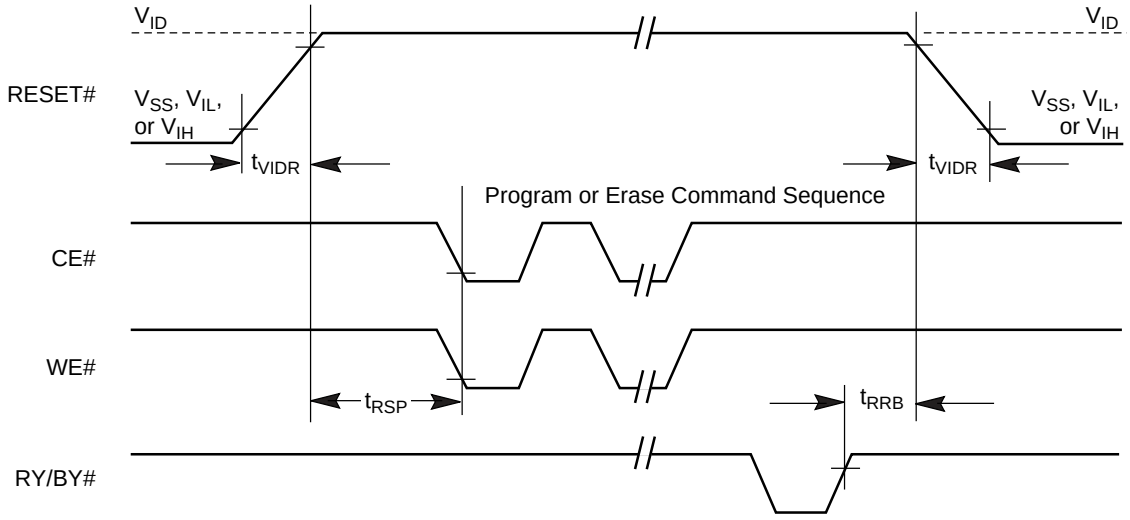
Figure 20. DQ2 vs. DQ6[59]



17.5 Temporary Sector Unprotect

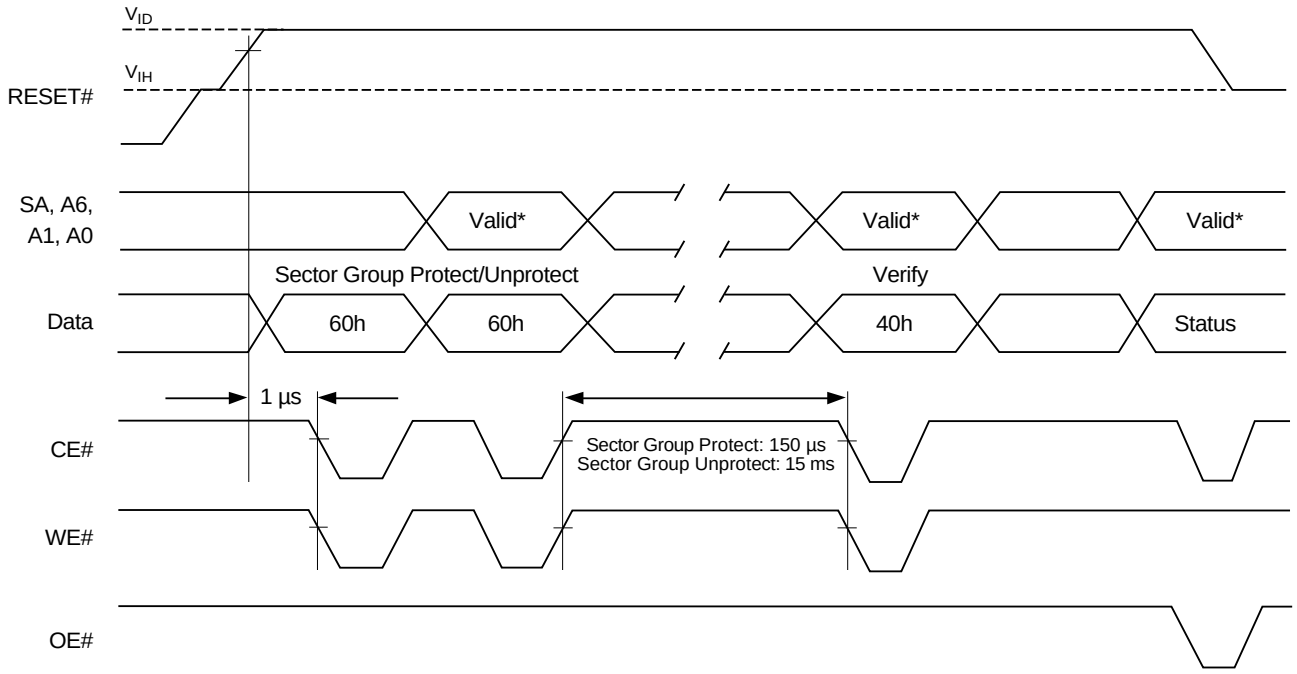
Parameter		Description		All Speed Options	Unit
JEDEC	Std				
	t_{VIDR}	V_{ID} Rise and Fall Time[60]	Min	500	ns
	t_{VHH}	V_{HH} Rise and Fall Time[60]	Min	250	ns
	t_{RSP}	RESET# Setup Time for Temporary Sector Unprotect	Min	4	µs
	t_{RRB}	RESET# Hold Time from RY/BY# High for Temporary Sector Unprotect	Min	4	µs

Figure 17.3 Temporary Sector Unprotect Timing Diagram



Notes
59. DQ2 toggles only when read at an address within an erase-suspended sector. The system may use OE# or CE# to toggle DQ2 and DQ6.
60. Not 100% tested.

Figure 17.4 Sector/Sector Block Protect and Unprotect Timing Diagram[61]

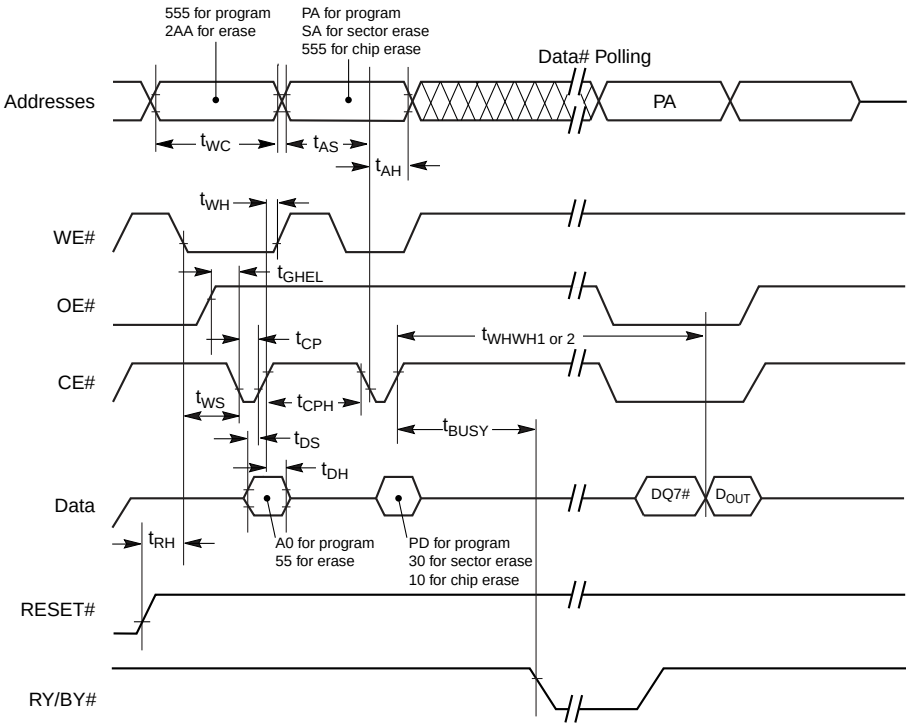


17.6 Alternate CE# Controlled Erase and Program Operations

Parameter					Speed Options		
JEDEC	Std.	Description			60	70	Unit
t_{AVAV}	t_{WC}	Write Cycle Time[62]		Min	60	70	ns
t_{AVWL}	t_{AS}	Address Setup Time		Min	0		ns
t_{ELAX}	t_{AH}	Address Hold Time		Min	35	35	ns
t_{DVEH}	t_{DS}	Data Setup Time		Min	30	30	ns
t_{EHDX}	t_{DH}	Data Hold Time		Min	0		ns
t_{GHEL}	t_{GHEL}	Read Recovery Time Before Write (OE# High to WE# Low)		Min	0		ns
t_{WLEL}	t_{WS}	WE# Setup Time		Min	0		ns
t_{EHWH}	t_{WH}	WE# Hold Time		Min	0		ns
t_{ELEH}	t_{CP}	CE# Pulse Width		Min	25	35	ns
t_{EHEL}	t_{CPH}	CE# Pulse Width High		Min	25	30	ns
t_{WHWH1}	t_{WHWH1}	Programming Operation[63]	Byte	Typ	6		µs
			Word	Typ	6		
t_{WHWH1}	t_{WHWH1}	Accelerated Programming Operation, Byte or Word[63]		Typ	4		µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation[63]		Typ	0.5		sec

Notes
61. For sector protect, A6 = 0, A1 = 1, A0 = 0. For sector unprotect, A6 = 1, A1 = 1, A0 = 0.
62. Not 100% tested.
63. See *Data Integrity* on page 58 for more information.

Figure 21. Alternate CE# Controlled Write (Erase/Program) Operation Timings[64, 65, 66, 67]



Notes
64. Figure indicates last two bus cycles of a program or erase operation.
65. PA = program address, SA = sector address, PD = program data.
66. DQ7# is the complement of the data written to the device. D_{OUT} is the data written to the device.
67. Waveforms are for the word mode.

18. Data Integrity

18.1 Erase Endurance

Table 16. Erase Endurance

Parameter	Minimum	Unit
Program/Erase cycles per main Flash array sectors	100K	PE cycle
Program/Erase cycles per PPB array or non-volatile register array[68]	100K	PE cycle

Note
68. Each write command to a non-volatile register causes a PE cycle on the entire non-volatile register array.

18.2 Data Retention

Table 17. Data Retention

Parameter	Test Conditions	Minimum Time	Unit
Data Retention Time	10K Program/Erase Cycles	20	Years
	100K Program/Erase Cycles	2	Years

Contact Cypress Sales and FAE for further information on the data integrity. An application note is available at: http://www.cypress.com/appnotes.

19. Erase and Programming Performance

Parameter	Typ[69]	Max[70]	Unit	Comments
Sector Erase Time	0.5	5	sec	Excludes 00h programming prior to erasure[71]
Chip Erase Time	39		sec	
Byte Program Time	6	80	µs	Excludes system level overhead[72]
Word Program Time	6	80	µs	
Accelerated Byte/Word Program Time	4	70	µs	

Notes
69. Typical program and erase times assume the following conditions: 25°C, V_{CC} = 3.0V, 100,000 cycles; checkerboard data pattern.
70. Under worst case conditions of 90°C, V_{CC} = 2.7V, 1,000,000 cycles.
71. In the pre-programming step of the Embedded Erase algorithm, all bytes are programmed to 00h before erasure.
72. System-level overhead is the time required to execute the two- or four-bus-cycle sequence for the program command. See Table 13 on page 35 for further information on command definitions.
73. The device has a minimum program and erase cycle endurance of 100,000 cycles per sector.

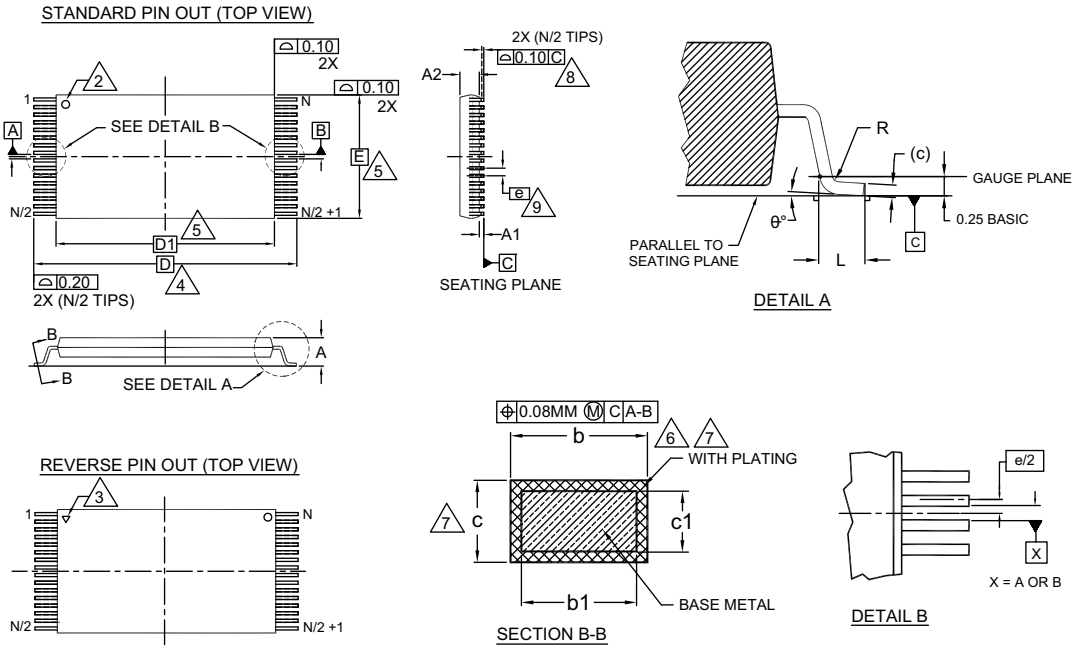
20. Pin Capacitance

Parameter Symbol	Parameter Description	Test Setup	Max	Unit
C_{IN}	Input Capacitance (applies to A20-A0, DQ15-DQ0)	V_{IN} = 0	8.5	pF
C_{OUT}	Output Capacitance (applies to DQ15-DQ0, RY/BY#)	V_{OUT} = 0	5.5	pF
C_{IN2}	Control Pin Capacitance (applies to CE#, WE#, OE#, WP#/ACC, RESET#, BYTE#)	V_{IN} = 0	12	pF

Notes
74. Sampled, not 100% tested.
75. Test conditions T_A = 25°C, f = 1.0 MHz.

21. Physical Dimensions

21.1 TS 048—48-Pin TSOP



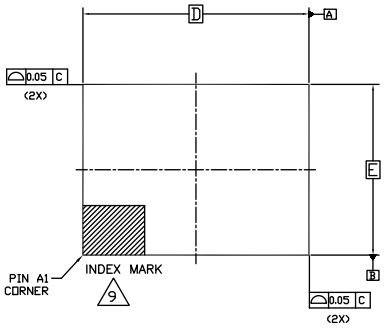
SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.20
A1	0.05	—	0.15
A2	0.95	1.00	1.05
b1	0.17	0.20	0.23
b	0.17	0.22	0.27
c1	0.10	—	0.16
c	0.10	—	0.21
D	20.00 BASIC		
D1	18.40 BASIC		
E	12.00 BASIC		
e	0.50 BASIC		
L	0.50	0.60	0.70
θ	0°	—	8
R	0.08	—	0.20
N	48		

NOTES:

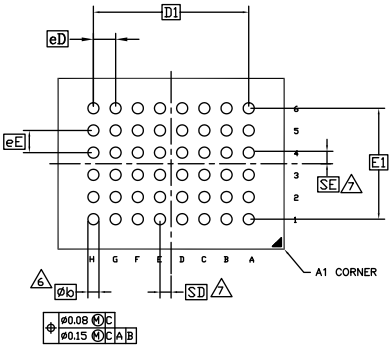
1. DIMENSIONS ARE IN MILLIMETERS (mm).
2. PIN 1 IDENTIFIER FOR STANDARD PIN OUT (DIE UP).
3. PIN 1 IDENTIFIER FOR REVERSE PIN OUT (DIE DOWN): INK OR LASER MARK.
4. TO BE DETERMINED AT THE SEATING PLANE -C- . THE SEATING PLANE IS DEFINED AS THE PLANE OF CONTACT THAT IS MADE WHEN THE PACKAGE LEADS ARE ALLOWED TO REST FREELY ON A FLAT HORIZONTAL SURFACE.
5. DIMENSIONS D1 AND E DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION ON E IS 0.15mm PER SIDE AND ON D1 IS 0.25mm PER SIDE.
6. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF b DIMENSION AT MAX. MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD TO BE 0.07mm .
7. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
8. LEAD COPLANARITY SHALL BE WITHIN 0.10mm AS MEASURED FROM THE SEATING PLANE.
9. DIMENSION "e" IS MEASURED AT THE CENTERLINE OF THE LEADS.
10. JEDEC SPECIFICATION NO. REF: MO-142(D)DD.

51-85183 *F

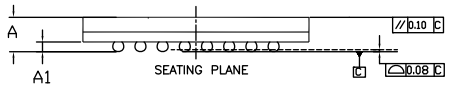
21.2 VBK048—48-Pin FBGA



TOP VIEW



BOTTOM VIEW



SIDE VIEW

SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	–	–	1.00
A1	0.18	–	–
D	8.15 BSC.		
E	6.15 BSC.		
D1	5.60 BSC.		
E1	4.00 BSC.		
MD	8		
ME	6		
n	48		
Øb	0.33	–	0.43
eD/eE	0.80 BSC.		
SD/SE	0.40 BSC.		

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994 .
2. ALL DIMENSIONS ARE IN MILLIMETERS .
3. BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP–010/020.
4. [e] REPRESENTS THE SOLDER BALL GRID PITCH .
5. SYMBOL "MD" IS THE BALL ROW MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL COLUMN MATRIX SIZE IN THE "E" DIRECTION.
   n IS THE TOTAL NUMBER OF POPULATED SOLDER BALLS FOR MATRIX SIZE MD AND ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" OR "SE" = 0.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 and "SE" = eE/2.
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

002-19063 **

22. Document History

Document History Page

Document Title: S29JL032J, 32-Mb (4M × 8-Bit/2M × 16-Bit), 3 V, Simultaneous Read/Write Flash Document Number: 002-00857				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	–	RYSU	01/27/2010	**Spansion Publication Number:** S29JL032J_00 Initial release
*A	–	RYSU	06/15/2010	**Global** Changed all references to typical Sector Erase time from 0.4 sec to 0.5 sec. Changed all references to “Secured Silicon Sector” to “Secured Silicon Region”. Corrected spelling and grammatical errors. **Product Selector Guide** Corrected Standard Voltage Range of 70 ns option from 3.0-3.6V to 2.7-3.6V. **Connection Diagrams** Added 48-ball FBGA connection diagram. **Pin Description** Changes “21 Addresses” to “21 Address Pins”. Added clarification that CE#, OE#, WE#, BYTE#, and RY/BY# are Active Low. **Ordering Information** Added FBGA ordering option. Added Low-halogen, Pb-free ordering option. Added valid combinations for FBGA. **Word/Byte Configuration** Added clarification that BYTE# must be connected to either the system VCC or ground. **Secured Silicon Region** Added clarification that D7 is the Secured Silicon Factory Indicator Bit. In Figure Secured Silicon Sector Protect Verify, corrected “Write reset command” to “Secured Silicon Region exit command”. **Command Definitions** Corrected “Writing specific addresses and data commands or sequences” to “Writing specific addresses and data sequences”. **Absolute Maximum Ratings** Corrected “A9, OE#, and RESET#” to “A9 and RESET#”. **DC Characteristics** Removed OE# from ILIT parameter description. Removed OE# = 12.5V from ILIT test conditions. Added 1 MHz to ICC6 and ICC7 test conditions. Removed Note 1 from ICC6 and ICC7. **Test Conditions** Update Figure “Test Setup” to reflect correct test setup. Added Note 1 to clarify that input rise and fall times are 0-100%. **Erase and Programming Performance** Changed Chip Erase typical time from 28 sec to 39 sec. Removed Note 5. **Physical Dimensions** Added VBK048 package outline drawing.

Document History Page (Continued)

Document Title: S29JL032J, 32-Mb (4M × 8-Bit/2M × 16-Bit), 3 V, Simultaneous Read/Write Flash Document Number: 002-00857				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
*B	–	RYSU	08/25/2010	**Global** Updated the data sheet designation from *Advanced Information* to *Preliminary.* Corrected spelling, capitalization, and grammatical errors. **Simultaneous Read/Write Operations with Zero Latency** Clarified that JL032J can be configured as either a top or bottom boot sector device, not both. **Ordering Information** Corrected typo in valid combinations table from "…, 41, 41" to "…, 41, 42". Clarified that Note 1 applies to the Packing Type column. **RESET#: Hardware Reset Pin** Changed "Refer to AC Characteristics on page 48" to "Refer to Hardware Reset (RESET#) on page 49". **Secured Silicon Region** Clarified the Secured Silicon Indicator Bit data based on factory and customer lock status. Removed forward looking statements regarding factory locking features as they are supported in this device. **Common Flash Memory Interface (CFI)** Clarified that once in the CFI query mode, the system must write the reset command to return to reading array data. **Erase Suspend/Erase Resume Commands** Added clarification that "It is not recommended to program the Secured Silicon Region after an erase suspend, as proper device functionality cannot be guaranteed.". **Erase and Programming Performance** Added Note 5 regarding minimum program and erase cycle endurance. **Pin Capacitance** Changed section title from "TSOP Pin Capacitance" to "Pin Capacitance". Updated values to reflect maximum capacitances for both TSOP and BGA. Removed typical capacitance values. Added specific pin clarifications to parameter descriptions. **Physical Dimensions** Updated the VBK048 package outline drawing.
*C	–	RYSU	04/07/2011	**Global** Updated the data sheet designation from Preliminary to Full Production (no designation on document). **Distinctive Characteristics** Corrected "Top and bottom boot sectors in the same device" to "Top and bottom boot sector configurations available". **RESET#: Hardware Reset Pin** Added warning that keeping CE# at VIL from power up through the first reset could cause erroneuous data on the first read. **Reset Command** Clarified that during an embedded program or erase, if DQ5 goes high then RY/BY# will remain low until a reset is issued. **Hardware Reset (RESET#)** Added note to the "Reset Timings" figure clarifying that CE# should only go low after RESET# has gone high.

Document History Page (Continued)

Document Title: S29JL032J, 32-Mb (4M × 8-Bit/2M × 16-Bit), 3 V, Simultaneous Read/Write Flash Document Number: 002-00857				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
*D	–	RYSU	08/24/2011	**RESET#: Hardware Reset Pin** Removed warning that keeping CE# at VIL from power up through the first reset could cause erroneuous data on the first read. **Command Definitions Table** Added Note 17 to clarify additional sector erase commands during time-out period. **Sector Erase Command Sequence** Added clarification regarding additional sector erase commands during time-out period. **Hardware Reset (RESET#)** Removed note to the “Reset Timings” figure clarifying that CE# should only go low after RESET# has gone high. **Physical Dimensions** Package drawings updated to latest version.
*E	–	RYSU	12/16/2011	**Global** Corrected all references in the text to the sector erase time-out period from 80 µs to 50 µs. **Word/Byte Configuration** Removed the statement “Please note that the BYTE# pin must be connected to either the system VCC or ground.”
*F	5034593	RYSU	12/08/2015	Updated to Cypress template.
*G	5742461	AESATMP7 / SZZX	05/19/2017	Updated *Distinctive Characteristics*: Updated Performance Characteristics: Replaced “Cycling endurance: 1 million cycles per sector typical” with “Cycling endurance: 100K cycles per sector”. Updated *Device Bus Operations*: Updated *Output Disable Mode*: Updated “S29JL032J Sector Addresses - Bottom Boot Devices (Sheet 2 of 2)”: Updated details in “Sector Address A20–A12” column corresponding to SA54 and SA55 sectors. Added *Data Integrity*. Updated Cypress Logo and Copyright.
*H	6214331	PRIT	08/23/2018	Updated *Ordering Information*: Added “A = Automotive, AEC-Q100 Grade 3 (-40°C to +85°C)” in the diagram. Added “Valid Combinations — Automotive Grade / AEC-Q100”. Updated *Physical Dimensions*: Updated *TS 048—48-Pin TSOP*: Removed spec “3664 \ f16-038.10 \ 11.6.7”. Added spec 51-85183 *F. Updated *VBK048—48-Pin FBGA*: Removed spec “g1001.2 \ f16-038.25 \ 07.13.10”. Added spec 002-19063 **. Updated to new template.
*I	6379705	BWHA	11/09/2018	Updated *Ordering Information*: Updated Valid Combinations — Automotive Grade / AEC-Q100: Updated details in “Model Number” and “Packing Type” columns in the table. Updated to new template. Completing Sunset Review.
*J	6585853	BWHA	05/31/2019	Updated to new template.

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