TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC74LCX273F, TC74LCX273FT, TC74LCX273FK

Low-Voltage Octal D-Type Flip-Flop with Clear with 5-V Tolerant Inputs and Outputs

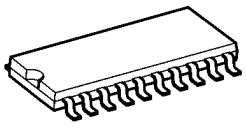
The TC74LCX273 is a high-performance CMOS octal D-type flip-flop. Designed for use in 3.3-V systems, it achieves high-speed operation while maintaining the CMOS low-power dissipation.

The device is designed for low-voltage (3.3 V) V_{CC} applications, but it could be used to interface to 5-V supply environment for both inputs and outputs.

This 8 bit D-type flip-flop is controlled by a clock input (CK) and a clear input ($\overline{CLR}$). When the $\overline{CLR}$ input is low, the eight outputs are at a low logic level.

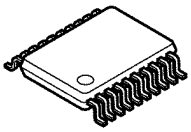
All inputs are equipped with protection circuits against static discharge.

TC74LCX273F



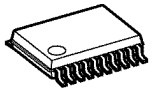
SOP20-P-300-1.27A

TC74LCX273FT



TSSOP20-P-0044-0.65A

TC74LCX273FK



VSSOP20-P-0030-0.50

Weight

SOP20-P-300-1.27A : 0.22 g (typ.)
TSSOP20-P-0044-0.65A : 0.08 g (typ.)
VSSOP20-P-0030-0.50 : 0.03 g (typ.)

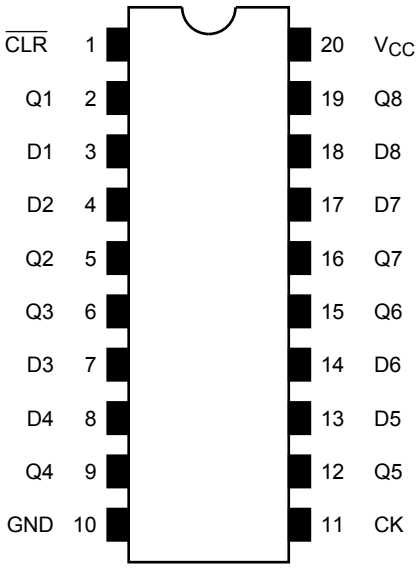
Features

- Low-voltage operation: V_{CC} = 1.65 to 3.6 V
- High-speed operation: t_{pd} = 8.5 ns (max) (V_{CC} = 3.0 to 3.6 V)
- Output current: $|I_{OH}|/I_{OL}$ = 24 mA (min) (V_{CC} = 3.0 V)
- Latch-up performance: $>\pm 500$ mA
- Available in JEITA SOP, TSSOP and VSSOP (US)
- Power-down protection is provided on all inputs and outputs
- Pin and function compatible with the 74 series (74AC/VHC/HC/F/ALS/LS etc.) 273 type

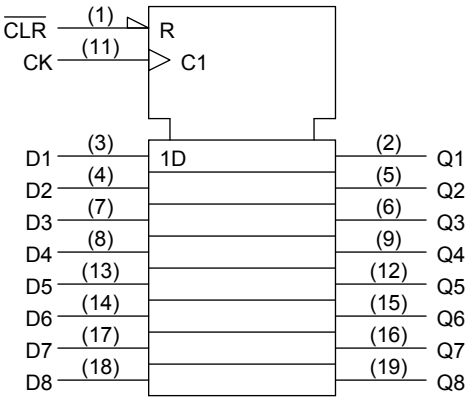
Note: The Electrical Characteristics of V_{CC}=1.8±0.15V is only applicable for products which manufactured from January 2009 onward.

Start of commercial production
2000-02

Pin Assignment (top view)



IEC Logic Symbol

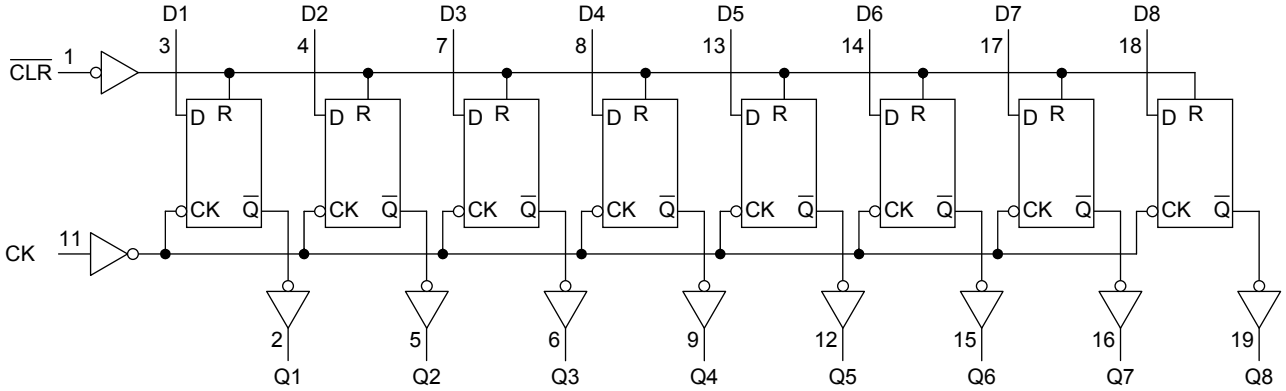


Truth Table

Inputs			Outputs	Function
$\overline{CLR}$	D	CK	Q	
L	X	X	L	Clear
H	L	↑	L	—
H	H	↑	H	—
H	X	↓	Qn	No change

X: Don’t care

System Diagram



Absolute Maximum Ratings (Note 1)

Characteristics	Symbol	Rating	Unit
Power supply voltage	V_{CC}	−0.5 to 7.0	V
DC input voltage	V_{IN}	−0.5 to 7.0	V
DC output voltage	V_{OUT}	−0.5 to 7.0 (Note 2)	V
		−0.5 to V_{CC} + 0.5 (Note 3)	
Input diode current	I_{IK}	−50	mA
Output diode current	I_{OK}	±50 (Note 4)	mA
DC output current	I_{OUT}	±50	mA
Power dissipation	P_D	180	mW
DC V_{CC}/ground current	I_{CC}/I_{GND}	±100	mA
Storage temperature	T_{stg}	−65 to 150	°C

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.
Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 2: V_{CC} = 0 V

Note 3: High or low state. I_{OUT} absolute maximum rating must be observed.

Note 4: V_{OUT} < GND, V_{OUT} > V_{CC}

Operating Ranges (Note 1)

Characteristics	Symbol	Rating	Unit
Power supply voltage	V_{CC}	1.65 to 3.6	V
		1.5 to 3.6 (Note 2)	
Input voltage	V_{IN}	0 to 5.5	V
Output voltage	V_{OUT}	0 to 5.5 (Note 3)	V
		0 to V_{CC} (Note 4)	
Output current	I_{OH}/I_{OL}	±24 (Note 5)	mA
		±12 (Note 6)	
Operating temperature	T_{opr}	−40 to 85	°C
Input rise and fall time	dt/dv	0 to 10 (Note 7)	ns/V

Note 1: The operating ranges must be maintained to ensure the normal operation of the device.
Unused inputs must be tied to either V_{CC} or GND.

Note 2: Data retention only

Note 3: V_{CC} = 0 V

Note 4: High or low state

Note 5: V_{CC} = 3.0 to 3.6 V

Note 6: V_{CC} = 2.7 to 3.0 V

Note 7: V_{IN} = 0.8 to 2.0 V, V_{CC} = 3.0 V

Electrical Characteristics

DC Characteristics (Ta = −40 to 85°C)

Characteristics		Symbol	Test Condition		V_{CC} (V)	Min	Max	Unit
Input voltage	H-level	V_{IH}			1.65 to 2.3	V_{CC} × 0.9	—	V
					2.3 to 2.7	1.7	—	
					2.7 to 3.6	2.0	—	
	L-level	V_{IL}			1.65 to 2.3	—	V_{CC} × 0.1	
					2.3 to 2.7	—	0.7	
					2.7 to 3.6	—	0.8	
Output voltage	H-level	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −100 μA	1.65 to 3.6	V_{CC} − 0.2	—	V
				I_{OH} = −4 mA	1.65	1.05	—	
				I_{OH} = −8 mA	2.3	1.7	—	
				I_{OH} = −12 mA	2.7	2.2	—	
				I_{OH} = −18 mA	3.0	2.4	—	
				I_{OH} = −24 mA	3.0	2.2	—	
	L-level	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 100 μA	1.65 to 3.6	—	0.2	
				I_{OL} = 4 mA	1.65	—	0.45	
				I_{OL} = 8 mA	2.3	—	0.7	
				I_{OL} = 12 mA	2.7	—	0.4	
				I_{OL} = 16 mA	3.0	—	0.4	
				I_{OL} = 24 mA	3.0	—	0.55	
Input leakage current		I_{IN}	V_{IN} = 0 to 5.5 V		1.65 to 3.6	—	±5.0	μA
Power-off leakage current		I_{OFF}	V_{IN}/V_{OUT} = 5.5 V		0	—	10.0	μA
Quiescent supply current		I_{CC}	V_{IN} = V_{CC} or GND		1.65 to 3.6	—	10.0	μA
			V_{IN} = 3.6 to 5.5 V		1.65 to 3.6	—	±10.0	
Increase in I_{CC} per input		ΔI_{CC}	V_{IN} = V_{CC} − 0.6 V		2.7 to 3.6	—	500	

AC Characteristics (Ta = –40 to 85°C)

Characteristics	Symbol	Test Condition	V_{CC} (V)	Min	Max	Unit
Maximum clock frequency	f_{MAX}	(Figure 1, Figure 2)	1.8±0.15	50	—	MHz
			2.5±0.2	100	—	
			2.7	150	—	
			3.3 ± 0.3	150	—	
Propagation delay time (CK-Q)	t_{PLH} t_{PHL}	(Figure 1, Figure 2)	1.8±0.15	—	30.0	ns
			2.5±0.2	—	10.5	
			2.7	—	9.5	
			3.3 ± 0.3	1.5	8.5	
Propagation delay time ($\overline{CLR}$ -Q)	t_{PHL}	(Figure 1, Figure 3)	1.8±0.15	—	30.0	ns
			2.5±0.2	—	10.5	
			2.7	—	9.5	
			3.3 ± 0.3	1.5	8.5	
Minimum pulse width (CK)	$t_{w\ (H)}$ $t_{w\ (L)}$	(Figure 1, Figure 2)	1.8±0.15	10.0	—	ns
			2.5±0.2	5.0	—	
			2.7	3.3	—	
			3.3 ± 0.3	3.3	—	
Minimum pulse width ($\overline{CLR}$)	$t_{w\ (L)}$	(Figure 3)	1.8±0.15	10.0	—	ns
			2.5±0.2	5.0	—	
			2.7	3.3	—	
			3.3 ± 0.3	3.3	—	
Minimum setup time	t_s	(Figure 1, Figure 2)	1.8±0.15	10.0	—	ns
			2.5±0.2	5.0	—	
			2.7	2.5	—	
			3.3 ± 0.3	2.5	—	
Minimum hold time	t_h	(Figure 1, Figure 2)	1.8±0.15	1.5	—	ns
			2.5±0.2	1.5	—	
			2.7	1.5	—	
			3.3 ± 0.3	1.5	—	
Minimum removal time	t_{rem}	(Figure 4)	1.8±0.15	8.0	—	ns
			2.5±0.2	4.0	—	
			2.7	2.5	—	
			3.3 ± 0.3	2.0	—	
Output to output skew	t_{osLH} t_{osHL}	(Note)	2.7	—	—	ns
			3.3 ± 0.3	—	1.0	

Note: Parameter guaranteed by design.
($t_{osLH} = |t_{pLHm} - t_{pLHn}|$, $t_{osHL} = |t_{pHLm} - t_{pHLn}|$)

Dynamic Switching Characteristics

(Ta = 25°C, input: $t_r = t_f = 2.5$ ns, $C_L = 50$ pF, $R_L = 500\ \Omega$)

Characteristics	Symbol	Test Condition	V_{CC} (V)	Typ.	Unit
Quiet output maximum dynamic V_{OL}	V_{OLP}	V_{IH} = 3.3 V, V_{IL} = 0 V	3.3	0.8	V
Quiet output minimum dynamic V_{OL}	$\lvert V_{OLV} \rvert$	V_{IH} = 3.3 V, V_{IL} = 0 V	3.3	0.8	V

Capacitive Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Condition	V_{CC} (V)	Typ.	Unit
Input capacitance	C_{IN}	—	3.3	7	pF
Output capacitance	C_{OUT}	—	0	8	pF
Power dissipation capacitance	C_{PD}	f_{IN} = 10 MHz (Note)	3.3	25	pF

Note: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption.
Average operating current can be obtained by the equation:
$I_{CC\ (opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8$ (per bit)

AC Test Circuit

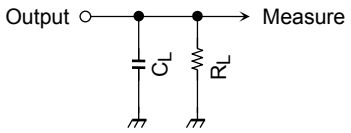


Figure 1

AC Waveform

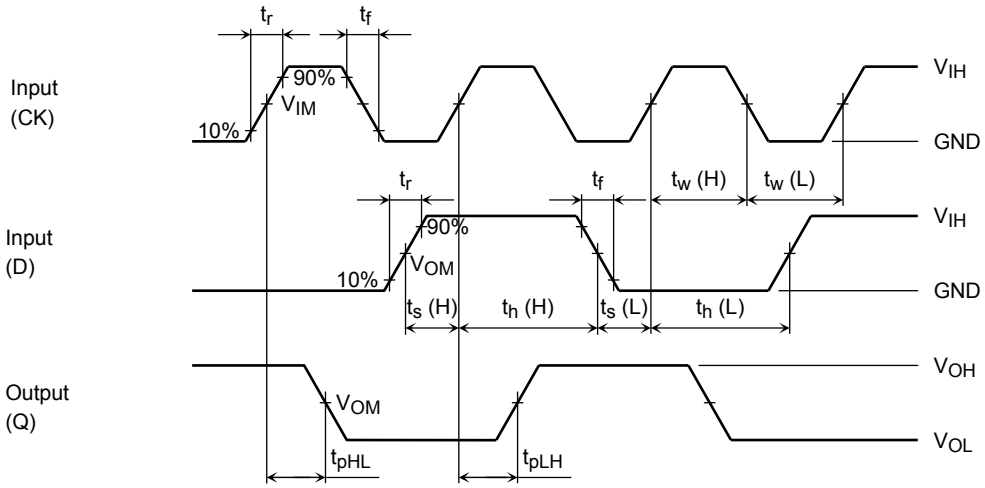


Figure 2 t_{pLH}, t_{pHL}, t_w, t_s, t_h

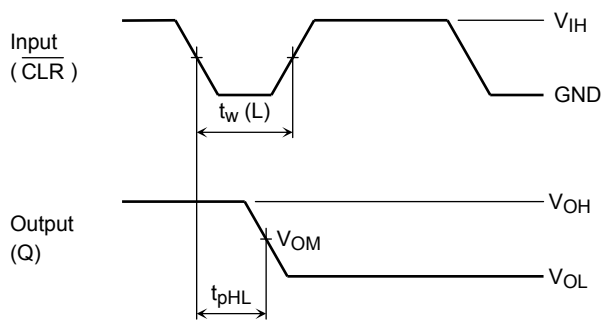


Figure 3 t_{pHL}

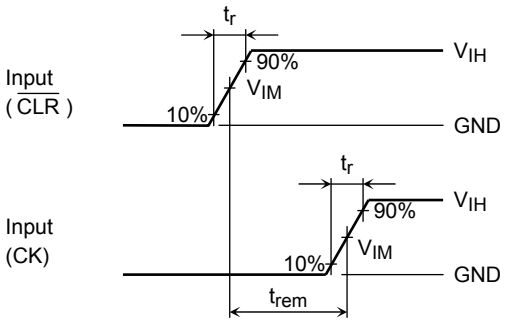
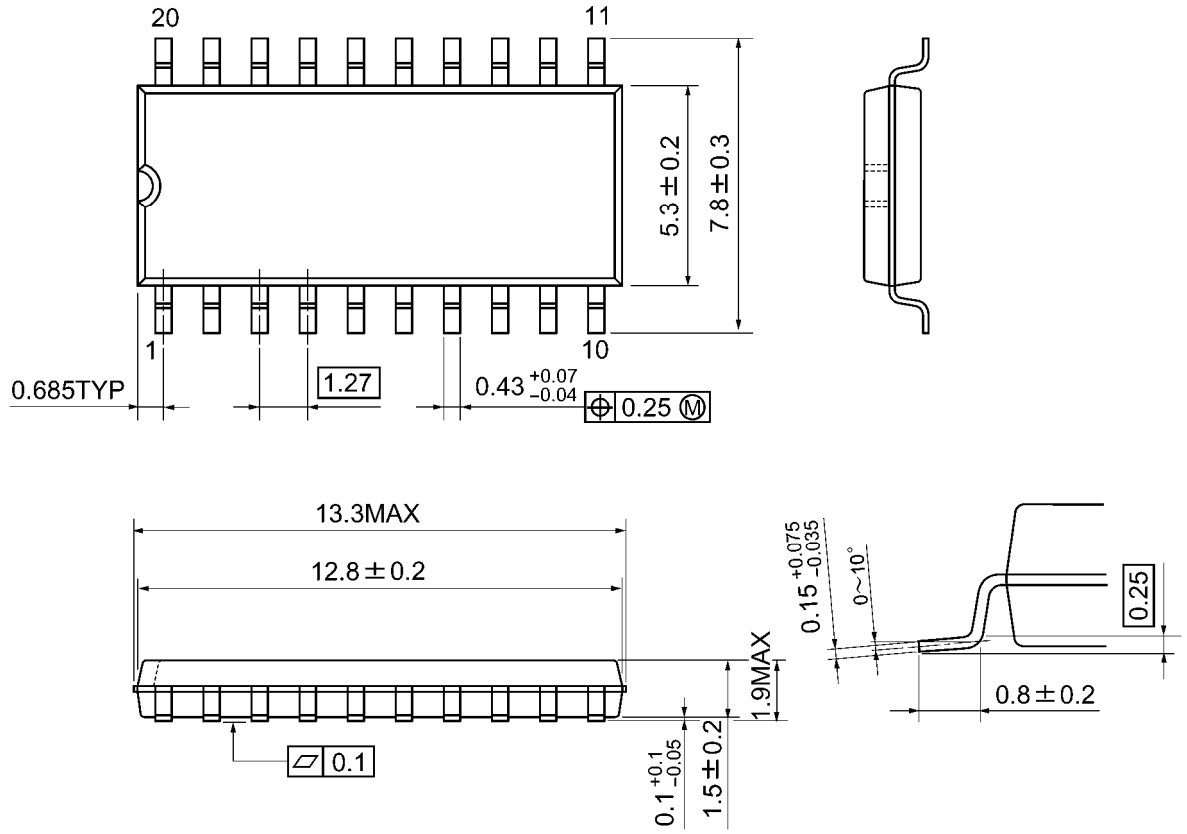


Figure 4 t_{rem}

	Symbol	V_{CC}		
		3.3 ± 0.3 V 2.7V	2.5 ± 0.2 V	1.8 ± 0.15 V
Input	V_{IH}	2.7V	V_{CC}	V_{CC}
	V_{IM}	1.5V	$V_{CC}/2$	$V_{CC}/2$
	t_r, t_f	2.5ns	2.0ns	2.0ns
Output	V_{OM}	1.5V	$V_{OH}/2$	$V_{OH}/2$
Load	C_L	50pF	30pF	30pF
	R_L	500Ω	500Ω	1kΩ

Package Dimensions

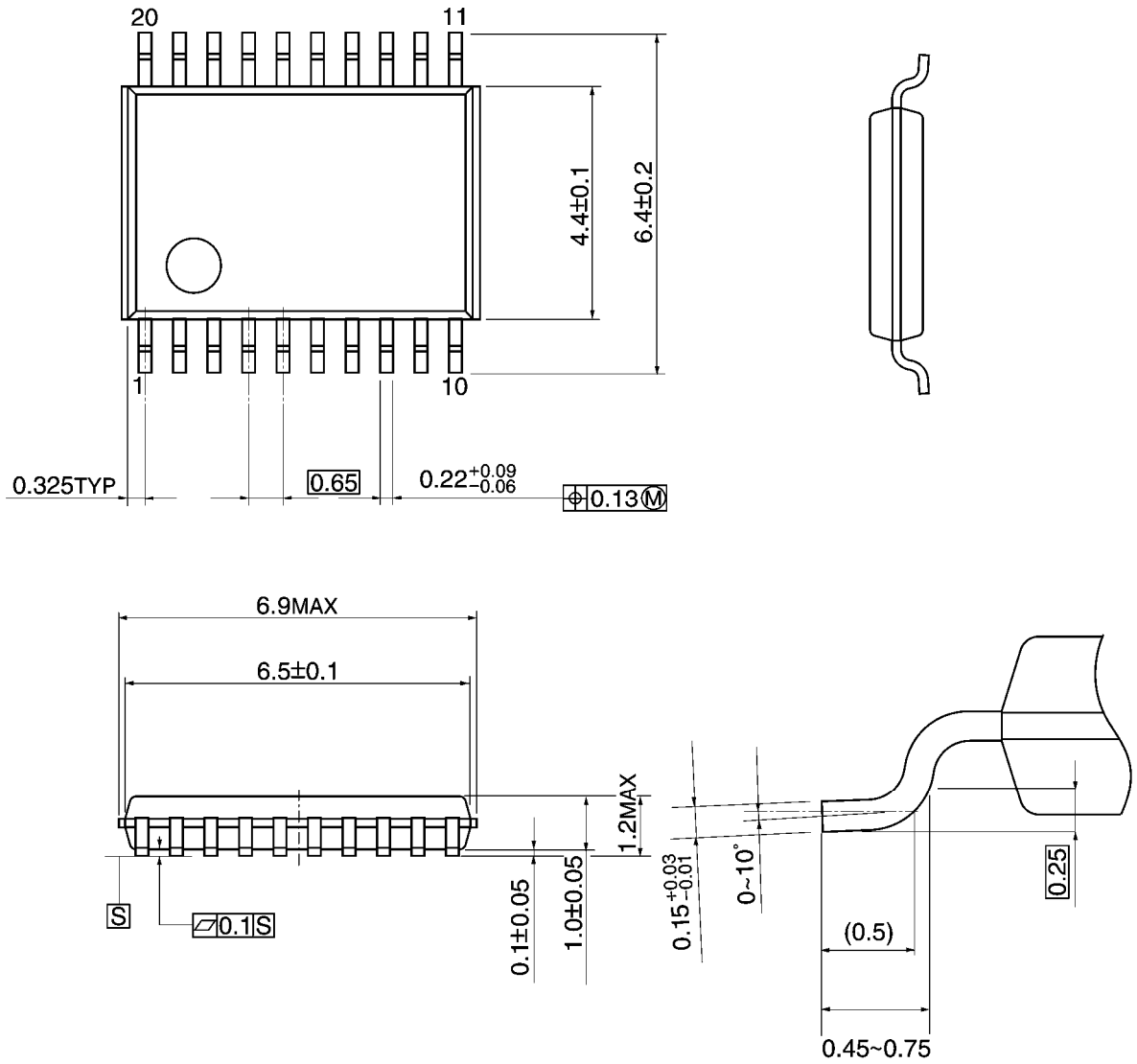
SOP20-P-300-1.27A Unit: mm



Weight: 0.22 g (typ.)

Package Dimensions

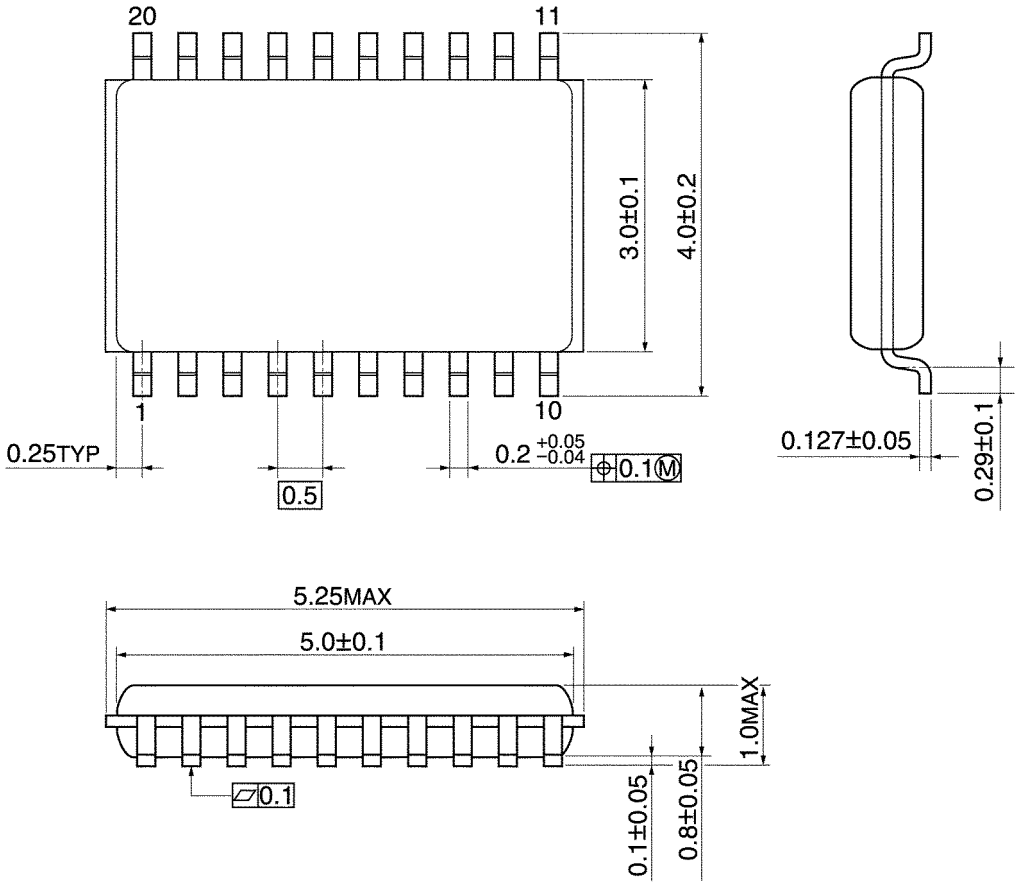
TSSOP20-P-0044-0.65A Unit: mm



Weight: 0.08 g (typ.)

Package Dimensions

VSSOP20-P-0030-0.50 Unit: mm



Weight: 0.03 g (typ.)

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