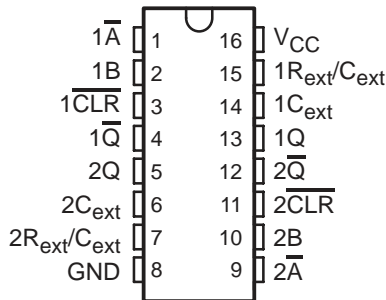


SN54LV221A, SN74LV221A DUAL MONOSTABLE MULTIVIBRATORS WITH SCHMITT-TRIGGER INPUTS

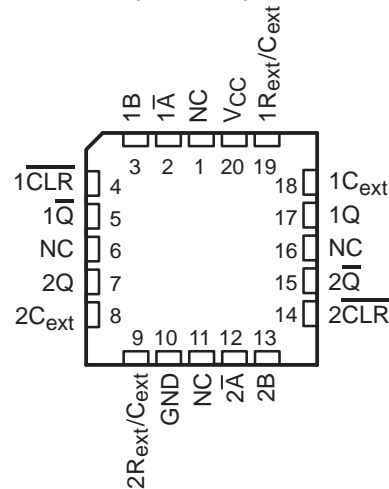
SCLS450G – DECEMBER 1999 – REVISED APRIL 2005

- 2-V to 5.5-V V_{CC} Operation
- Max t_{pd} of 11 ns at 5 V
- Support Mixed-Mode Voltage Operation on All Ports
- Schmitt-Trigger Circuitry on \overline{A} , B, and \overline{CLR} Inputs for Slow Input Transition Rates
- Overriding Clear Terminates Output Pulse
- Glitch-Free Power-Up Reset on Outputs
- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

SN54LV221A . . . J OR W PACKAGE
SN74LV221A . . . D, DB, DGV, NS, OR PW PACKAGE
(TOP VIEW)



SN54LV221A . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description/ordering information

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SOIC – D	Tube of 40	SN74LV221AD	LV221A
		Reel of 2500	SN74LV221ADR	
	SOP – NS	Reel of 2000	SN74LV221ANSR	74LV221A
	SSOP – DB	Reel of 2000	SN74LV221ADBR	LV221A
	TSSOP – PW	Tube of 90	SN74LV221APW	LV221A
		Reel of 2000	SN74LV221APWR	
Reel of 250		SN74LV221APWT		
TVSOP – DGV	Reel of 2000	SN74LV221ADGVR	LV221A	
–55°C to 125°C	CDIP – J	Tube of 25	SNJ54LV221AJ	SNJ54LV221AJ
	CFP – W	Tube of 150	SNJ54LV221AW	SNJ54LV221AW
	LCCC – FK	Tube of 55	SNJ54LV221AFK	SNJ54LV221AFK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

UNLESS OTHERWISE NOTED this document contains PRODUCTION DATA information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2005, Texas Instruments Incorporated

SN54LV221A, SN74LV221A DUAL MONOSTABLE MULTIVIBRATORS WITH SCHMITT-TRIGGER INPUTS

SCLS450G – DECEMBER 1999 – REVISED APRIL 2005

description/ordering information (continued)

The 'LV221A devices are dual multivibrators designed for 2-V to 5.5-V V_{CC} operation. Each multivibrator has a negative-transition-triggered (\bar{A}) input and a positive-transition-triggered (B) input, either of which can be used as an inhibit input.

These edge-triggered multivibrators feature output pulse-duration control by three methods. In the first method, the \bar{A} input is low and the B input goes high. In the second method, the B input is high and the \bar{A} input goes low. In the third method, the \bar{A} input is low, the B input is high, and the clear (\bar{CLR}) input goes high.

The output pulse duration is programmable by selecting external resistance and capacitance values. The external timing capacitor must be connected between C_{ext} and R_{ext}/C_{ext} (positive) and an external resistor connected between R_{ext}/C_{ext} and V_{CC} . To obtain variable pulse durations, connect an external variable resistor between R_{ext}/C_{ext} and V_{CC} . The output pulse duration also can be reduced by taking \bar{CLR} low.

Pulse triggering occurs at a particular voltage level and is not related directly to the transition time of the input pulse. The \bar{A} , B, and \bar{CLR} inputs have Schmitt triggers with sufficient hysteresis to handle slow input transition rates with jitter-free triggering at the outputs.

Once triggered, the outputs are independent of further transitions of the \bar{A} and B inputs and are a function of the timing components, or the output pulses can be terminated by the overriding clear. Input pulses can be of any duration relative to the output pulse. Output pulse duration can be varied by choosing the appropriate timing components. Output rise and fall times are TTL compatible and independent of pulse duration. Typical triggering and clearing sequences are illustrated in the input/output timing diagram.

The variance in output pulse duration from device to device typically is less than $\pm 0.5\%$ for given external timing components. An example of this distribution for the 'LV221A is shown in Figure 8. Variations in output pulse duration versus supply voltage and temperature are shown in Figure 5.

During power up, Q outputs are in the low state, and \bar{Q} outputs are in the high state. The outputs are glitch free, without applying a reset pulse.

These devices are fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down.

Pin assignments are identical to those of the 'AHC123A and 'AHCT123A devices, so the 'LV221A can be substituted for those devices not using the retrigger feature.

For additional application information on multivibrators, see the application report *Designing With The SN74AHC123A and SN74AHCT123A*, literature number SCLA014.

SN54LV221A, SN74LV221A DUAL MONOSTABLE MULTIVIBRATORS WITH SCHMITT-TRIGGER INPUTS

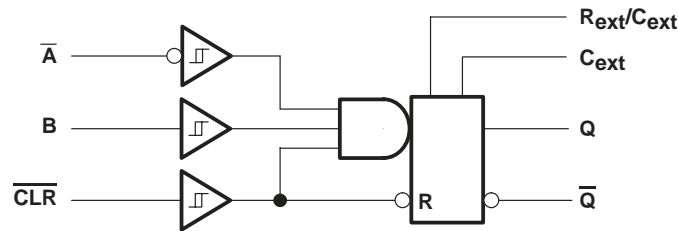
SCLS450G – DECEMBER 1999 – REVISED APRIL 2005

FUNCTION TABLE
(each multivibrator)

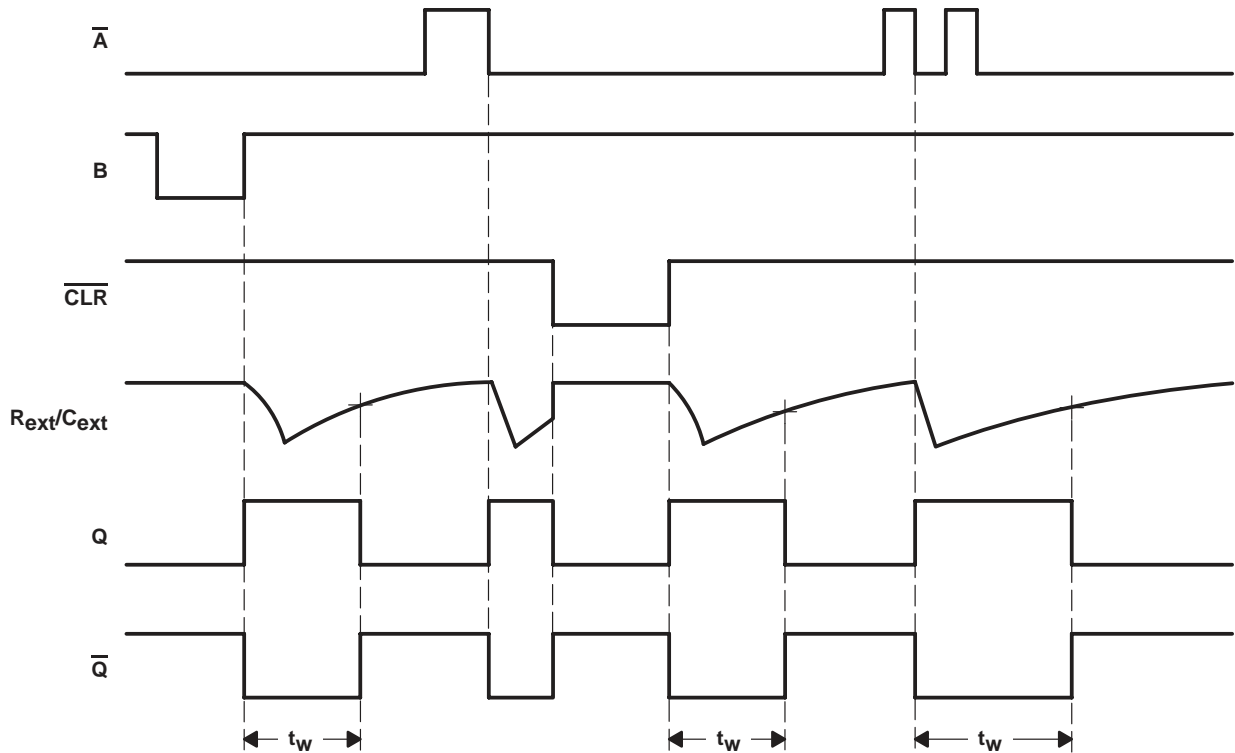
INPUTS			OUTPUTS		FUNCTION
$\overline{\text{CLR}}$	$\overline{\text{A}}$	B	Q	$\overline{\text{Q}}$	
L	X	X	L	H	Reset
H	H	X	L	H	Inhibit
H	X	L	L	H	Inhibit
H	L	↑	⌋	⌋	Outputs enabled
H	↓	H	⌋	⌋	Outputs enabled
↑†	L	H	⌋	⌋	Outputs enabled

† This condition is true only if the output of the latch formed by the NAND gate has been conditioned to the logic 1 state prior to $\overline{\text{CLR}}$ going high. This latch is conditioned by taking either $\overline{\text{A}}$ high or B low while $\overline{\text{CLR}}$ is inactive (high).

logic diagram, each multivibrator (positive logic)



input/output timing diagram



SN54LV221A, SN74LV221A
DUAL MONOSTABLE MULTIVIBRATORS
WITH SCHMITT-TRIGGER INPUTS

SCLS450G – DECEMBER 1999 – REVISED APRIL 2005

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input voltage range, V_I (see Note 1)	-0.5 V to 7 V
Output voltage range in high or low state, V_O (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range in power-off state, V_O (see Note 1)	-0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$)	-20 mA
Output clamp current, I_{OK} ($V_O < 0$)	-50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 25 mA
Continuous current through V_{CC} or GND	± 50 mA
Package thermal impedance, θ_{JA} (see Note 3): D package	73°C/W
DB package	82°C/W
DGV package	120°C/W
NS package	64°C/W
PW package	108°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
 2. This value is limited to 5.5 V maximum.
 3. The package thermal impedance is calculated in accordance with JESD 51-7.



SN54LV221A, SN74LV221A DUAL MONOSTABLE MULTIVIBRATORS WITH SCHMITT-TRIGGER INPUTS

SCLS450G – DECEMBER 1999 – REVISED APRIL 2005

recommended operating conditions (see Note 4)

		SN54LV221A		SN74LV221A		UNIT
		MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	2	5.5	2	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 2 V	1.5	1.5		V
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.7	V _{CC} × 0.7		
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.7	V _{CC} × 0.7		
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.7	V _{CC} × 0.7		
V _{IL}	Low-level input voltage	V _{CC} = 2 V	0.5	0.5		V
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.3	V _{CC} × 0.3		
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.3	V _{CC} × 0.3		
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.3	V _{CC} × 0.3		
V _I	Input voltage	0	5.5	0	5.5	V
V _O	Output voltage	0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 2 V		-50	-50	μA
		V _{CC} = 2.3 V to 2.7 V		-2	-2	mA
		V _{CC} = 3 V to 3.6 V		-6	-6	
		V _{CC} = 4.5 V to 5.5 V		-12	-12	
I _{OL}	Low-level output current	V _{CC} = 2 V		50	50	μA
		V _{CC} = 2.3 V to 2.7 V		2	2	mA
		V _{CC} = 3 V to 3.6 V		6	6	
		V _{CC} = 4.5 V to 5.5 V		12	12	
R _{ext}	External timing resistance	V _{CC} = 2 V	5k	5k		Ω
		V _{CC} ≥ 3 V	1k	1k		
C _{ext}	External timing capacitance	No restriction		No restriction		pF
Δt/ΔV _{CC}	Power-up ramp rate	1		1		ms/V
T _A	Operating free-air temperature	-55	125	-40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN54LV221A, SN74LV221A DUAL MONOSTABLE MULTIVIBRATORS WITH SCHMITT-TRIGGER INPUTS

SCLS450G – DECEMBER 1999 – REVISED APRIL 2005

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	SN54LV221A			SN74LV221A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V _{OH}	I _{OH} = -50 μA	2 V to 5.5 V	V _{CC} -0.1			V _{CC} -0.1			V
	I _{OH} = -2 mA	2.3 V	2			2			
	I _{OH} = -6 mA	3 V	2.48			2.48			
	I _{OH} = -12 mA	4.5 V	3.8			3.8			
V _{OL}	I _{OL} = 50 μA	2 V to 5.5 V	0.1			0.1			V
	I _{OL} = 2 mA	2.3 V	0.4			0.4			
	I _{OL} = 6 mA	3 V	0.44			0.44			
	I _{OL} = 12 mA	4.5 V	0.55			0.55			
I _I	R _{ext} /C _{ext} †	V _I = 5.5 V or GND	2 V to 5.5 V			±2.5			μA
	\bar{A} , B, and \overline{CLR}	V _I = 5.5 V or GND	0			±1			
I _{CC}	Quiescent	V _I = V _{CC} or GND, I _O = 0	5.5 V			20			μA
I _{CC}	Active state (per circuit)	V _I = V _{CC} or GND, R _{ext} /C _{ext} = 0.5 V _{CC}	2.3 V			220			μA
			3 V			280			
			4.5 V			650			
			5.5 V			975			
I _{off}		V _I or V _O = 0 to 5.5 V	0			5			μA
C _i		V _I = V _{CC} or GND	3.3 V			1.9			pF
			5 V			1.9			

† This test is performed with the terminal in the off-state condition.

timing requirements over recommended operating free-air temperature range, V_{CC} = 2.5 V ± 0.2 V (unless otherwise noted) (see Figure 1)

		T _A = 25°C		SN54LV221A		SN74LV221A		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t _w	Pulse duration	\overline{CLR}		6	6.5	6.5	6.5	ns
		\bar{A} or B trigger		6	6.5	6.5	6.5	

timing requirements over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

		T _A = 25°C		SN54LV221A		SN74LV221A		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t _w	Pulse duration	\overline{CLR}		5	5	5	5	ns
		\bar{A} or B trigger		5	5	5	5	

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

		T _A = 25°C		SN54LV221A		SN74LV221A		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t _w	Pulse duration	\overline{CLR}		5	5	5	5	ns
		\bar{A} or B trigger		5	5	5	5	

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



SN54LV221A, SN74LV221A DUAL MONOSTABLE MULTIVIBRATORS WITH SCHMITT-TRIGGER INPUTS

SCLS450G – DECEMBER 1999 – REVISED APRIL 2005

switching characteristics over recommended operating free-air temperature range, $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	$T_A = 25^\circ\text{C}$			SN54LV221A		SN74LV221A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	\bar{A} or B	Q or \bar{Q}	$C_L = 15\text{ pF}$	14.6*	31.4*	1*	37*	1	37	ns	
	$\overline{\text{CLR}}$	Q or \bar{Q}		13.2*	25*	1*	29.5*	1	29.5		
	$\overline{\text{CLR}}$ trigger	Q or \bar{Q}		15.2*	33.4*	1*	39*	1	39		
t_{pd}	\bar{A} or B	Q or \bar{Q}	$C_L = 50\text{ pF}$	16.7	36	1	42	1	42	ns	
	$\overline{\text{CLR}}$	Q or \bar{Q}		15	32.8	1	34.5	1	34.5		
	$\overline{\text{CLR}}$ trigger	Q or \bar{Q}		17.4	38	1	44	1	44		
t_w^\dagger		Q or \bar{Q}	$C_L = 50\text{ pF}$, $C_{ext} = 28\text{ pF}$, $R_{ext} = 2\text{ k}\Omega$	203	260		320		320	ns	
			$C_L = 50\text{ pF}$, $C_{ext} = 0.01\text{ }\mu\text{F}$, $R_{ext} = 10\text{ k}\Omega$	90	100	110	90	110	90	110	μs
			$C_L = 50\text{ pF}$, $C_{ext} = 0.1\text{ }\mu\text{F}$, $R_{ext} = 10\text{ k}\Omega$	0.9	1	1.1	0.9	1.1	0.9	1.1	ms
Δt_w^\ddagger			$C_L = 50\text{ pF}$	± 1						%	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

$\dagger t_w$ = Pulse duration at Q and \bar{Q} outputs

$\ddagger \Delta t_w$ = Output pulse-duration variation (Q and \bar{Q}) between circuits in same package

switching characteristics over recommended operating free-air temperature range, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	$T_A = 25^\circ\text{C}$			SN54LV221A		SN74LV221A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	\bar{A} or B	Q or \bar{Q}	$C_L = 15\text{ pF}$	10.2*	20.6*	1*	24*	1	24	ns	
	$\overline{\text{CLR}}$	Q or \bar{Q}		9.3*	15.8*	1*	18.5*	1	18.5		
	$\overline{\text{CLR}}$ trigger	Q or \bar{Q}		10.6*	22.4*	1*	26*	1	26		
t_{pd}	\bar{A} or B	Q or \bar{Q}	$C_L = 50\text{ pF}$	11.8	24.1	1	27.5	1	27.5	ns	
	$\overline{\text{CLR}}$	Q or \bar{Q}		10.6	19.3	1	22	1	22		
	$\overline{\text{CLR}}$ trigger	Q or \bar{Q}		12.3	25.9	1	29.5	1	29.5		
t_w^\dagger		Q or \bar{Q}	$C_L = 50\text{ pF}$, $C_{ext} = 28\text{ pF}$, $R_{ext} = 2\text{ k}\Omega$	186	240		300		300	ns	
			$C_L = 50\text{ pF}$, $C_{ext} = 0.01\text{ }\mu\text{F}$, $R_{ext} = 10\text{ k}\Omega$	90	100	110	90	110	90	110	μs
			$C_L = 50\text{ pF}$, $C_{ext} = 0.1\text{ }\mu\text{F}$, $R_{ext} = 10\text{ k}\Omega$	0.9	1	1.1	0.9	1.1	0.9	1.1	ms
Δt_w^\ddagger			$C_L = 50\text{ pF}$	± 1						%	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

$\dagger t_w$ = Pulse duration at Q and \bar{Q} outputs

$\ddagger \Delta t_w$ = Output pulse-duration variation (Q and \bar{Q}) between circuits in same package

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

SN54LV221A, SN74LV221A DUAL MONOSTABLE MULTIVIBRATORS WITH SCHMITT-TRIGGER INPUTS

SCLS450G – DECEMBER 1999 – REVISED APRIL 2005

switching characteristics over recommended operating free-air temperature range, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	$T_A = 25^\circ\text{C}$			SN54LV221A		SN74LV221A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	\overline{A} or B	Q or \overline{Q}	$C_L = 15\text{ pF}$	7.1*	12*	1*	14*	1	14	ns	
	\overline{CLR}	Q or \overline{Q}		6.5*	9.4*	1*	11*	1	11		
	\overline{CLR} trigger	Q or \overline{Q}		7.3*	12.9*	1*	15*	1	15		
t_{pd}	\overline{A} or B	Q or \overline{Q}	$C_L = 50\text{ pF}$	8.2	14	1	16	1	16	ns	
	\overline{CLR}	Q or \overline{Q}		7.4	11.4	1	13	1	13		
	\overline{CLR} trigger	Q or \overline{Q}		8.6	14.9	1	17	1	17		
t_w^\dagger		Q or \overline{Q}	$C_L = 50\text{ pF}$, $C_{ext} = 28\text{ pF}$, $R_{ext} = 2\text{ k}\Omega$	171	200		240		240	ns	
			$C_L = 50\text{ pF}$, $C_{ext} = 0.01\text{ }\mu\text{F}$, $R_{ext} = 10\text{ k}\Omega$	90	100	110	90	110	90	110	μs
			$C_L = 50\text{ pF}$, $C_{ext} = 0.1\text{ }\mu\text{F}$, $R_{ext} = 10\text{ k}\Omega$	0.9	1	1.1	0.9	1.1	0.9	1.1	ms
Δt_w^\ddagger			$C_L = 50\text{ pF}$	± 1						%	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† t_w = Pulse duration at Q and \overline{Q} outputs

‡ Δt_w = Output pulse-duration variation (Q and \overline{Q}) between circuits in same package

operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd} Power dissipation capacitance	$C_L = 50\text{ pF}$, $f = 10\text{ MHz}$	3.3 V	50	pF
		5 V	51	

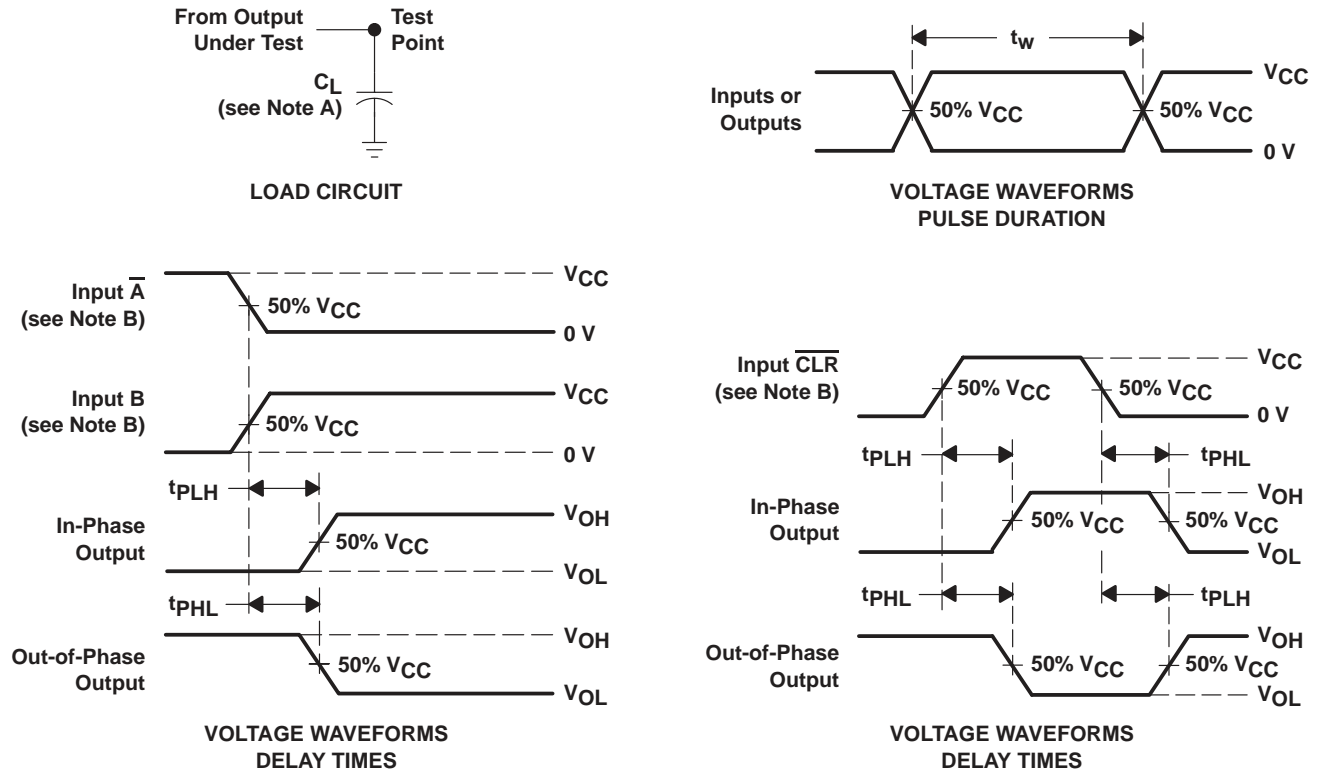
PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



SN54LV221A, SN74LV221A DUAL MONOSTABLE MULTIVIBRATORS WITH SCHMITT-TRIGGER INPUTS

SCLS450G – DECEMBER 1999 – REVISED APRIL 2005

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 B. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r = 3 \text{ ns}$, $t_f = 3 \text{ ns}$.
 C. The outputs are measured one at a time, with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

SN54LV221A, SN74LV221A DUAL MONOSTABLE MULTIVIBRATORS WITH SCHMITT-TRIGGER INPUTS

SCLS450G – DECEMBER 1999 – REVISED APRIL 2005

APPLICATION INFORMATION

caution in use

To prevent malfunctions due to noise, connect a high-frequency capacitor between V_{CC} and GND, and keep the wiring between the external components and C_{ext} and R_{ext}/C_{ext} terminals as short as possible.

power-down considerations

Large values of C_{ext} can cause problems when powering down the 'LV221A because of the amount of energy stored in the capacitor. When a system containing this device is powered down, the capacitor can discharge from V_{CC} through the protection diodes at pin 2 or pin 14. Current through the input protection diodes must be limited to 30 mA; therefore, the turn-off time of the V_{CC} power supply must not be faster than $t = V_{CC} \times C_{ext}/30 \text{ mA}$. For example, if $V_{CC} = 5 \text{ V}$ and $C_{ext} = 15 \text{ pF}$, the V_{CC} supply must turn off no faster than $t = (5 \text{ V}) \times (15 \text{ pF})/30 \text{ mA} = 2.5 \text{ ns}$. Usually, this is not a problem because power supplies are heavily filtered and cannot discharge at this rate. When a more rapid decrease of V_{CC} to zero occurs, the 'LV221A can sustain damage. To avoid this possibility, use external clamping diodes.

output pulse duration

The output pulse duration, t_w , is determined primarily by the values of the external capacitance (C_T) and timing resistance (R_T). The timing components are connected as shown in Figure 2.

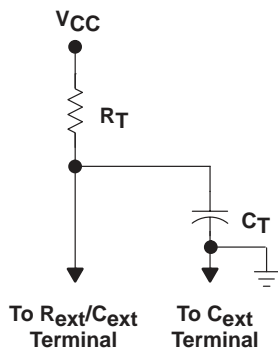


Figure 2. Timing-Component Connections

The pulse duration is given by:

$$t_w = K \times R_T \times C_T \quad (1)$$

if C_T is $\geq 1000 \text{ pF}$, $K = 1.0$

or

if C_T is $< 1000 \text{ pF}$, K can be determined from Figure 7

where:

- t_w = pulse duration in ns
- R_T = external timing resistance in $k\Omega$
- C_T = external capacitance in pF
- K = multiplier factor

Equation 1 and Figure 3 or 4 can be used to determine values for pulse duration, external resistance, and external capacitance.

APPLICATION INFORMATION†

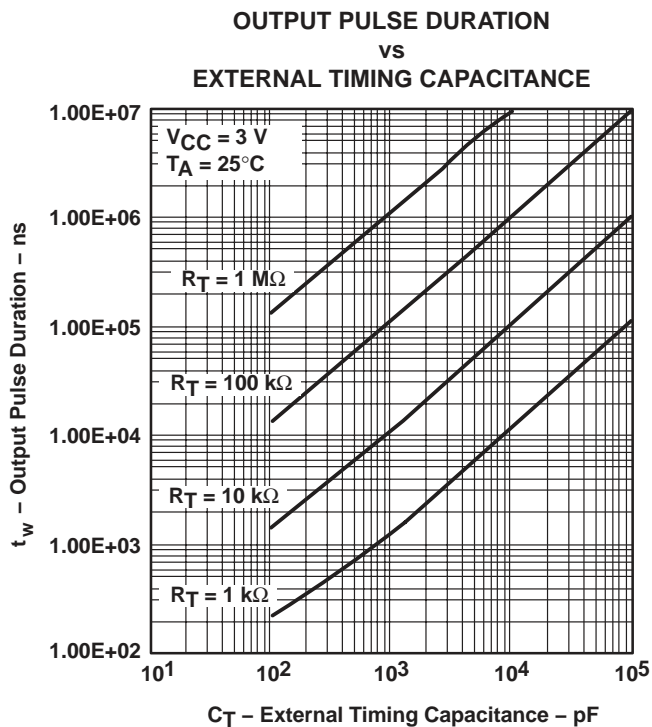


Figure 3

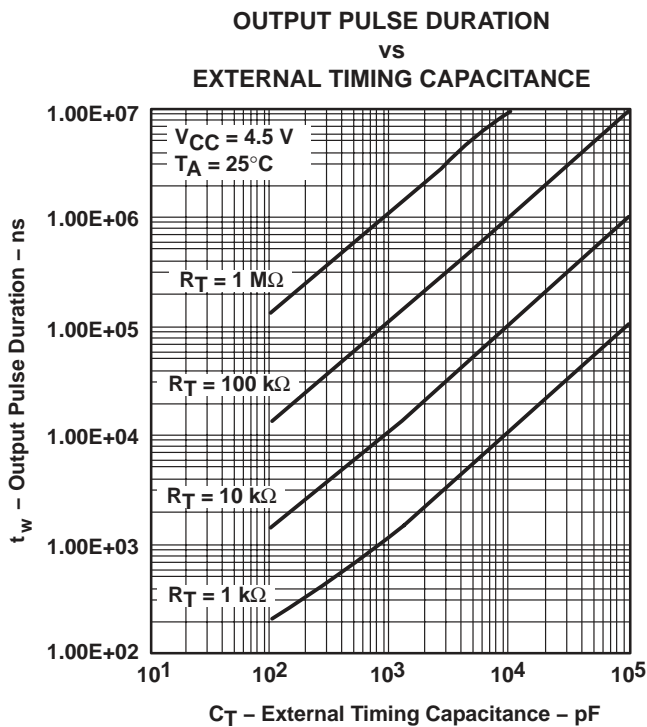


Figure 4

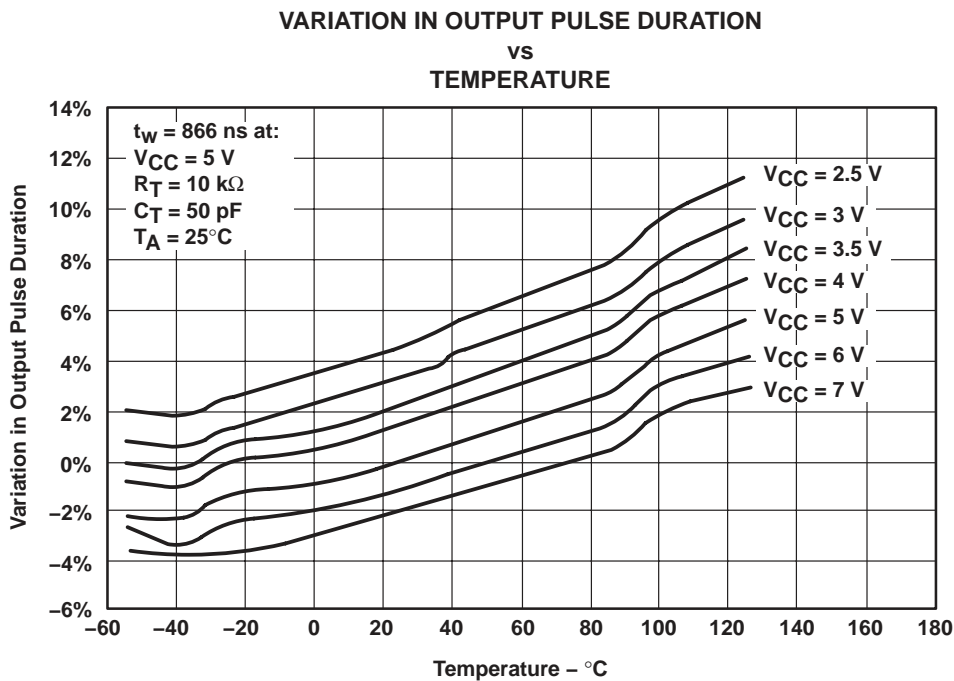


Figure 5

† Operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied.

SN54LV221A, SN74LV221A DUAL MONOSTABLE MULTIVIBRATORS WITH SCHMITT-TRIGGER INPUTS

SCLS450G – DECEMBER 1999 – REVISED APRIL 2005

APPLICATION INFORMATION†

EXTERNAL CAPACITANCE
vs
MULTIPLIER FACTOR

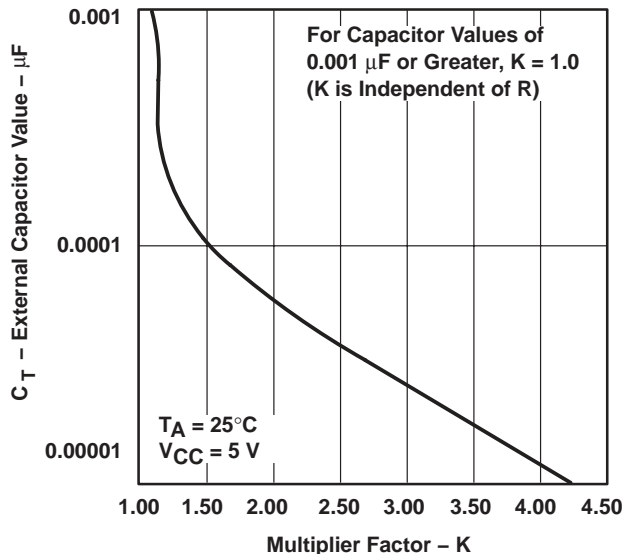


Figure 6

OUTPUT PULSE DURATION
vs
SUPPLY VOLTAGE

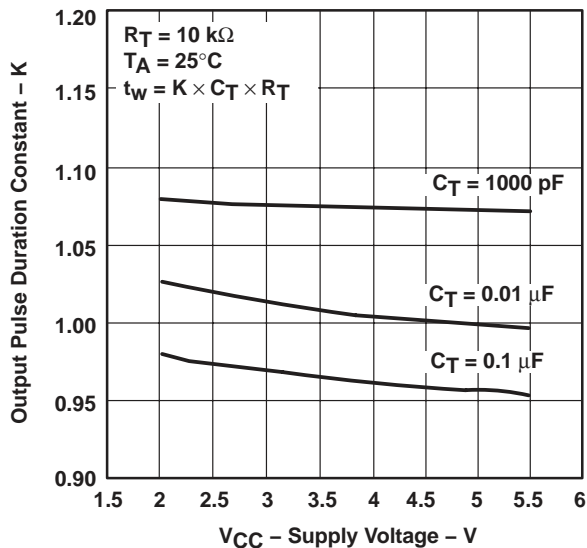


Figure 7

DISTRIBUTION OF UNITS
vs
OUTPUT PULSE DURATION

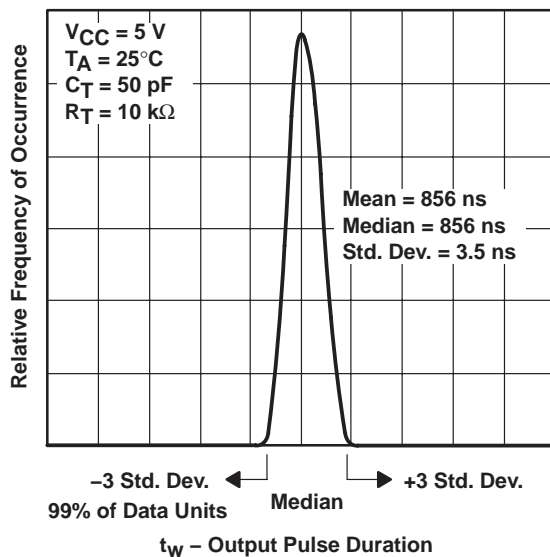


Figure 8

† Operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LV221ADGVR	ACTIVE	TVSOP	DGV	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV221A	Samples
SN74LV221ADR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV221A	Samples
SN74LV221ANSR	ACTIVE	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	74LV221A	Samples
SN74LV221APWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV221A	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74LV221A :

- Automotive : [SN74LV221A-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV221ADGVR	TVSOP	DGV	16	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74LV221ADR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74LV221ANSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74LV221APWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV221ADGVR	TVSOP	DGV	16	2000	356.0	356.0	35.0
SN74LV221ADR	SOIC	D	16	2500	340.5	336.1	32.0
SN74LV221ANSR	SO	NS	16	2000	356.0	356.0	35.0
SN74LV221APWR	TSSOP	PW	16	2000	356.0	356.0	35.0

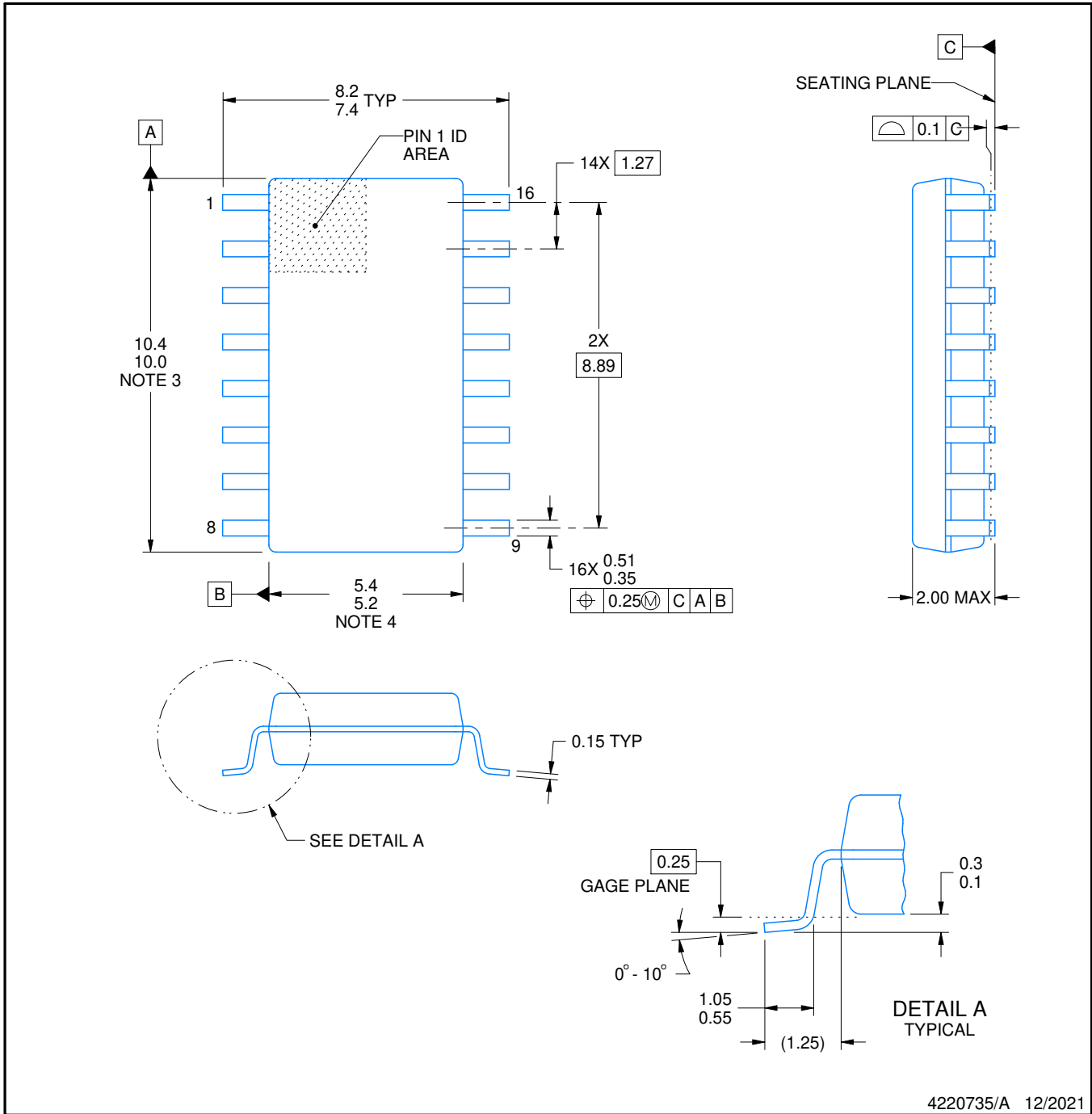


PACKAGE OUTLINE

NS0016A

SOP - 2.00 mm max height

SOP



4220735/A 12/2021

NOTES:

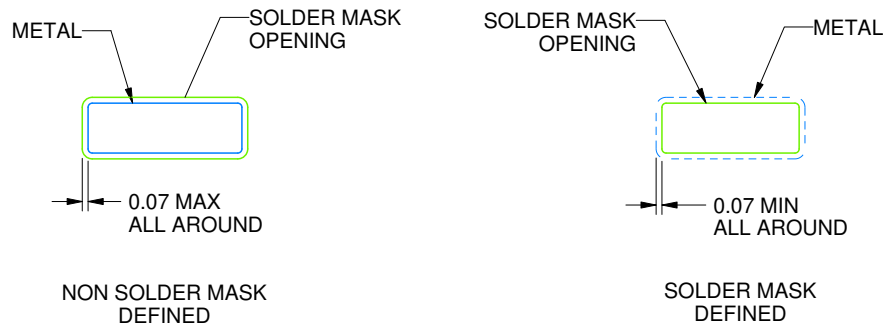
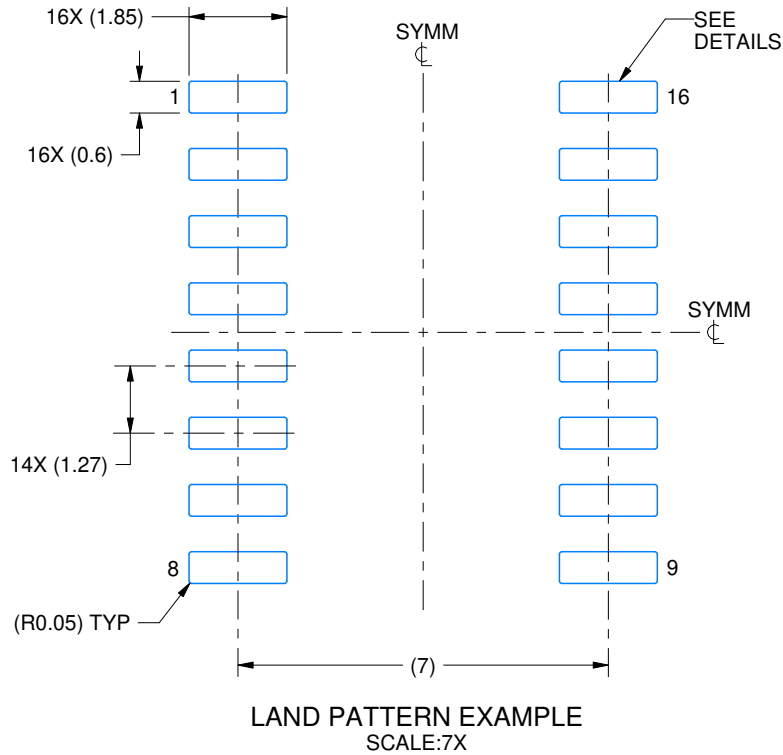
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

EXAMPLE BOARD LAYOUT

NS0016A

SOP - 2.00 mm max height

SOP



4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

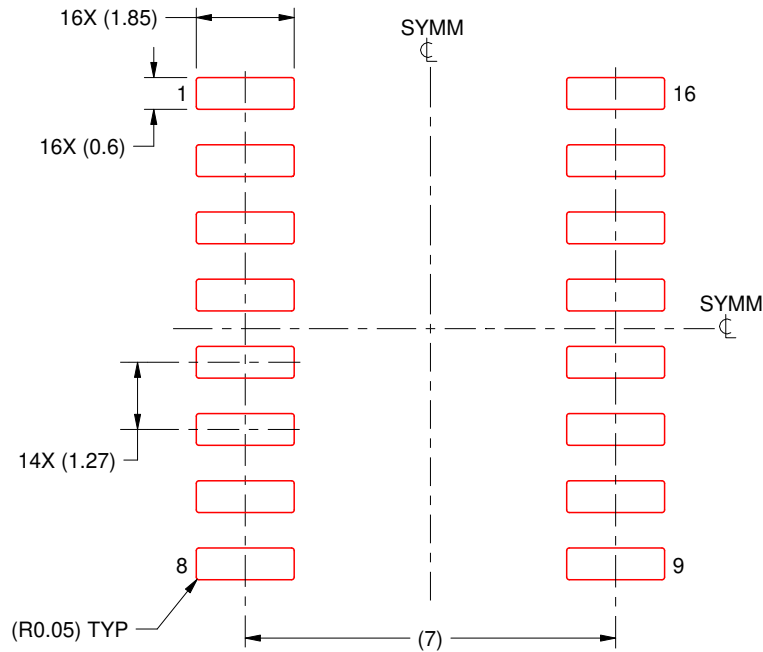
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

NS0016A

SOP - 2.00 mm max height

SOP



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

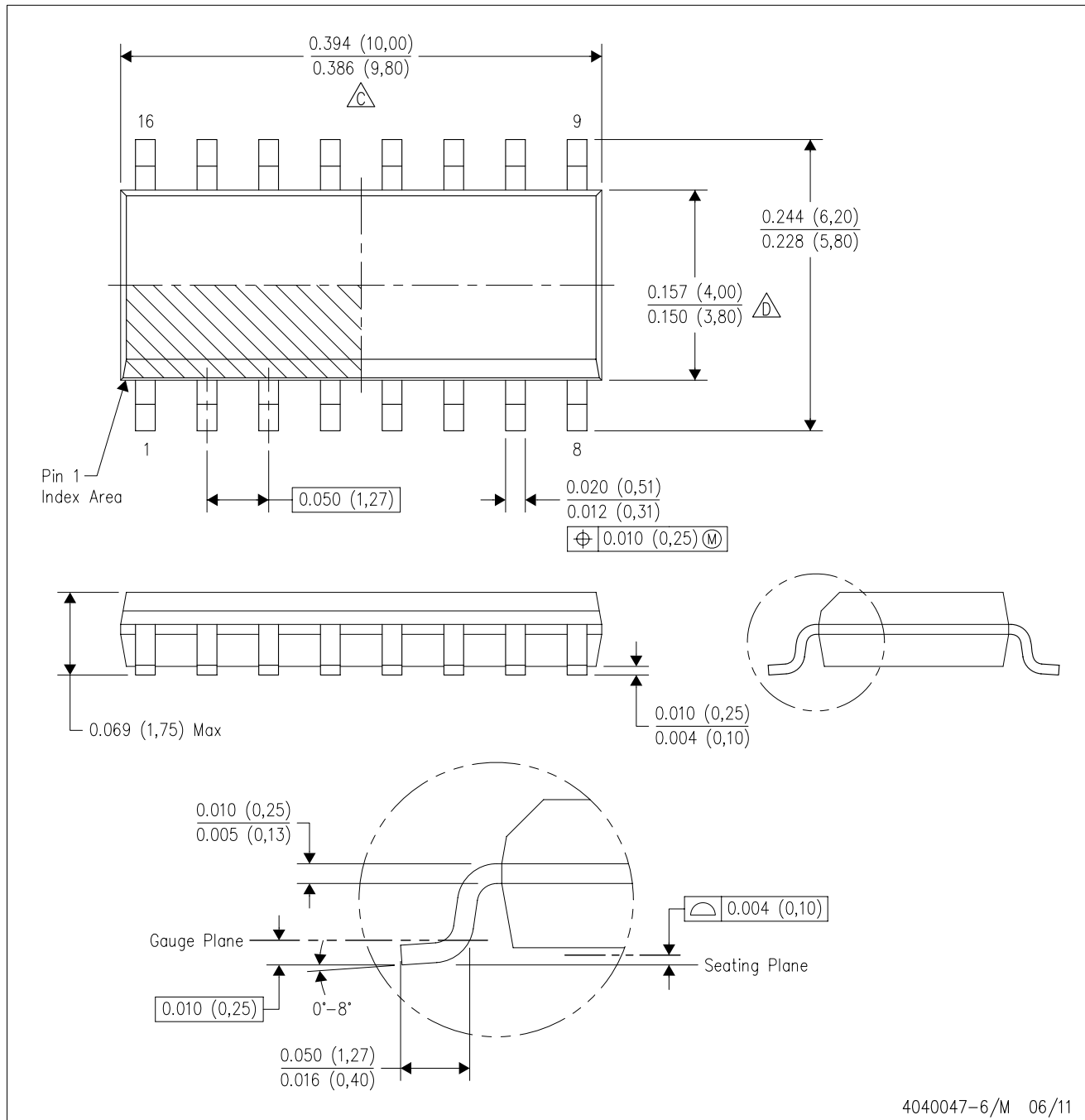
4220735/A 12/2021

NOTES: (continued)

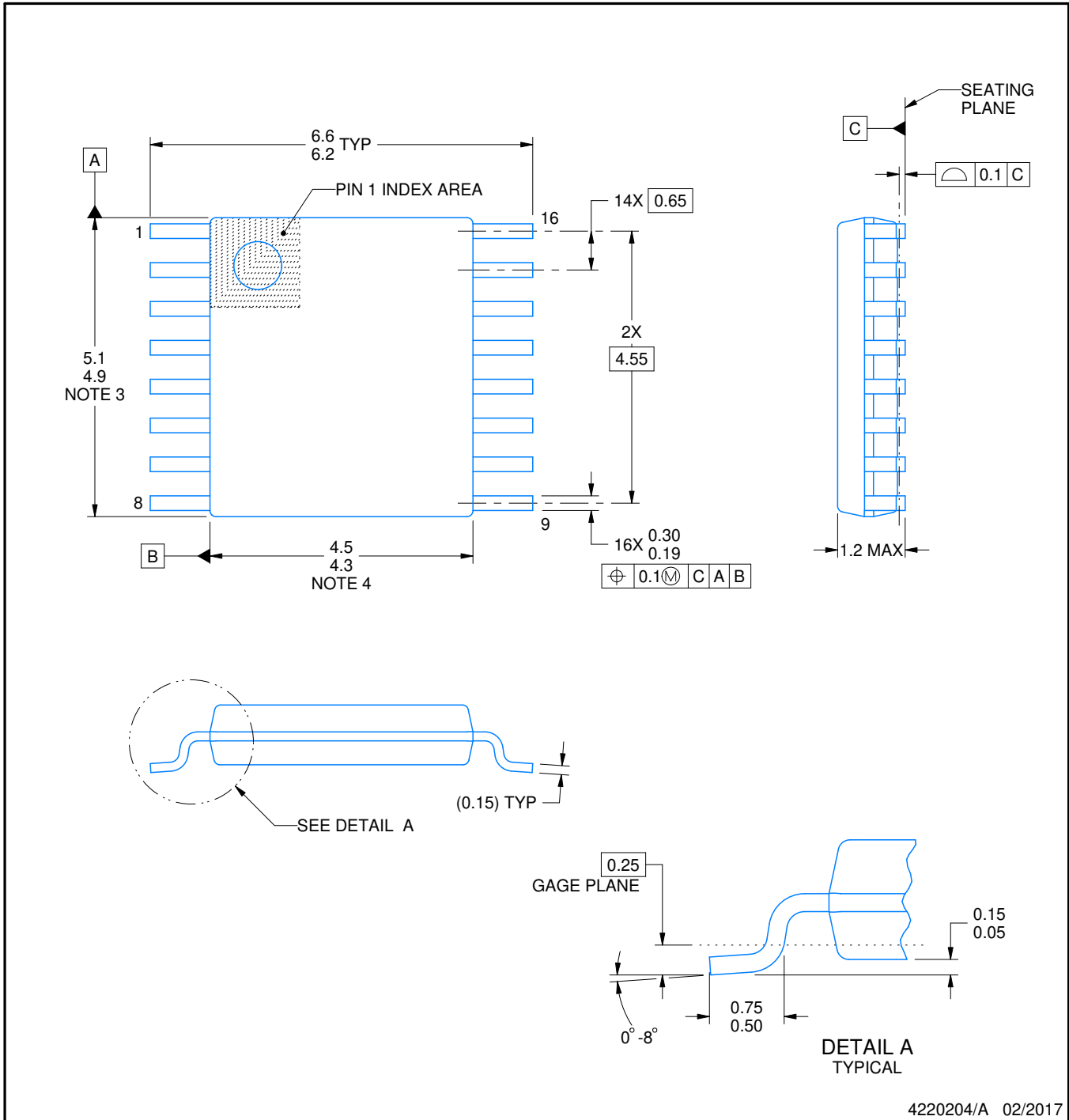
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.



4220204/A 02/2017

NOTES:

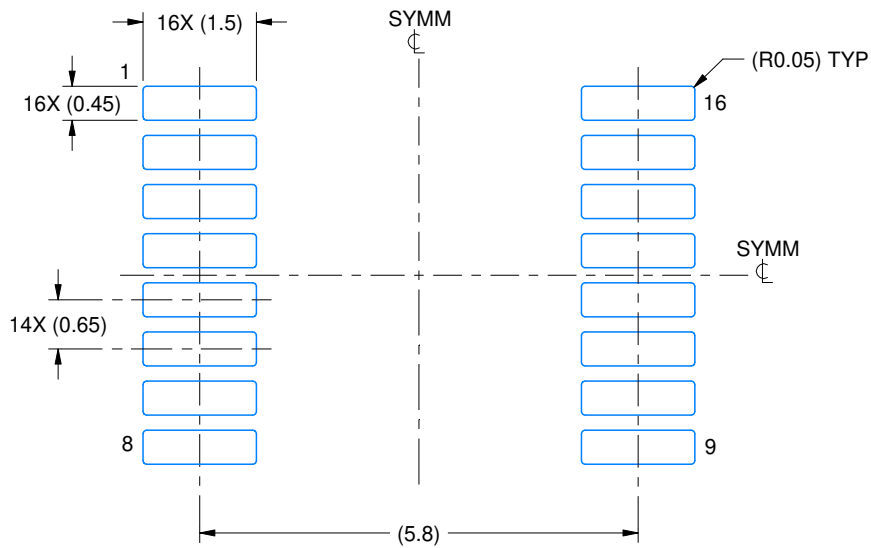
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

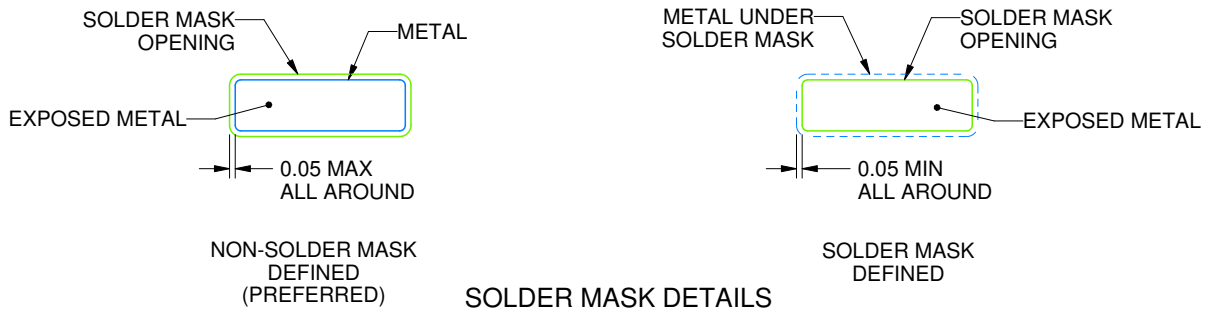
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

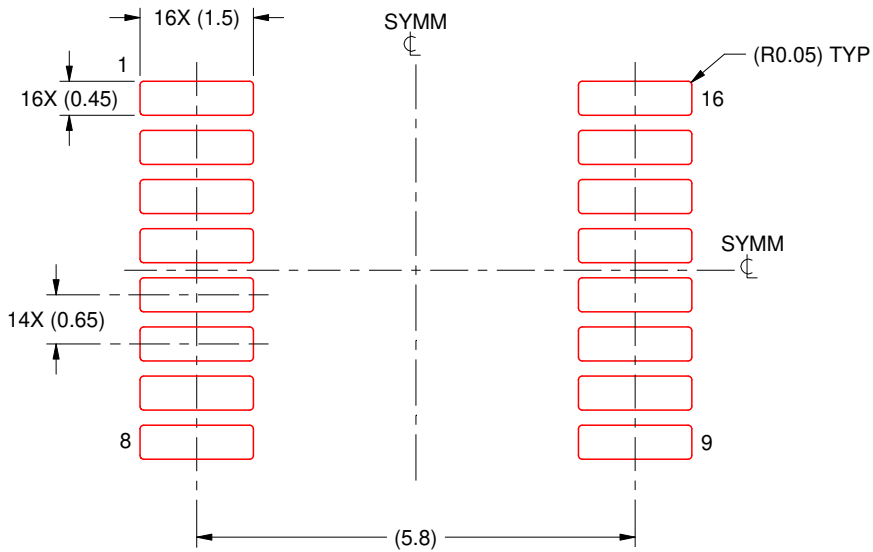
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

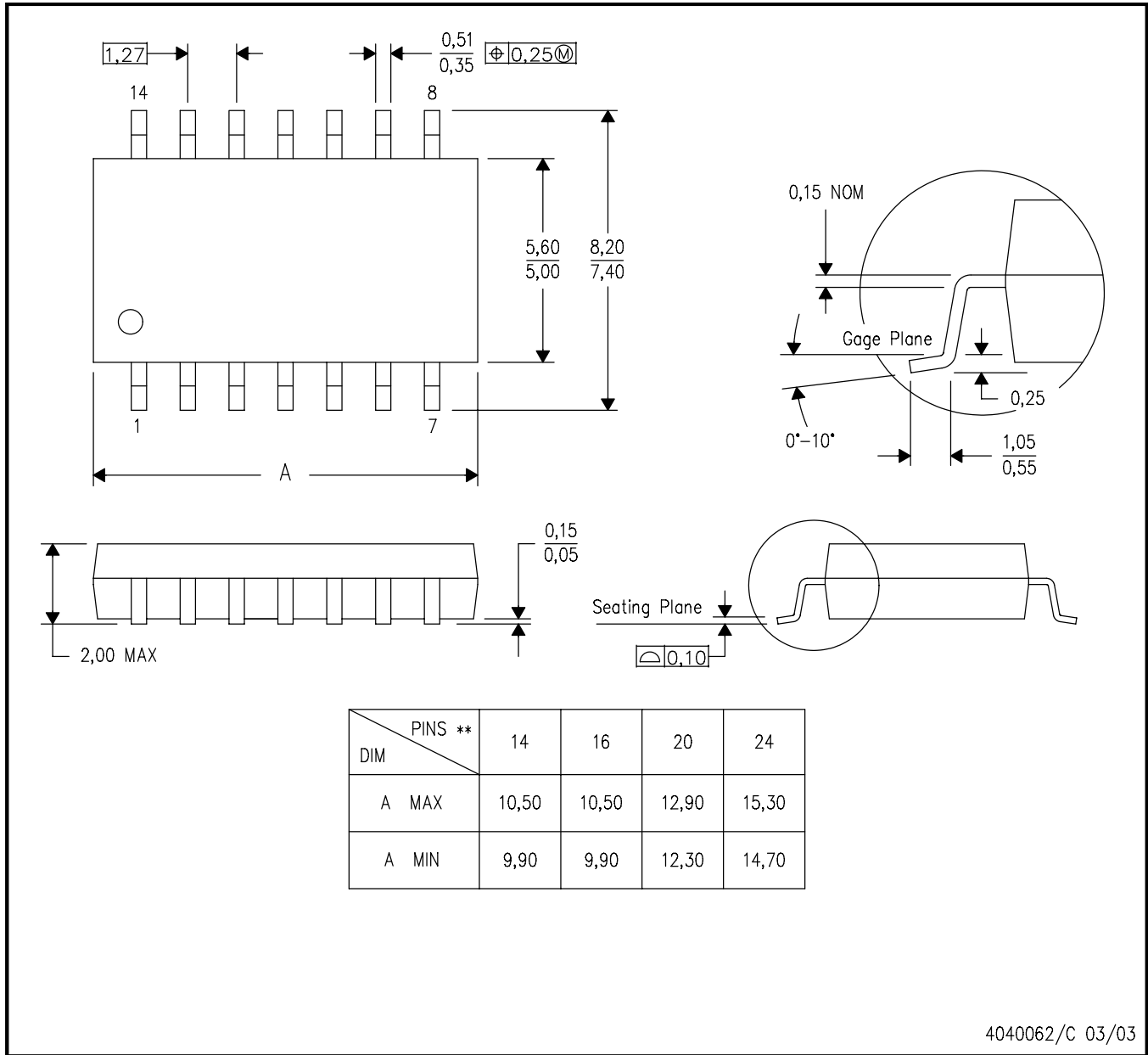
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN

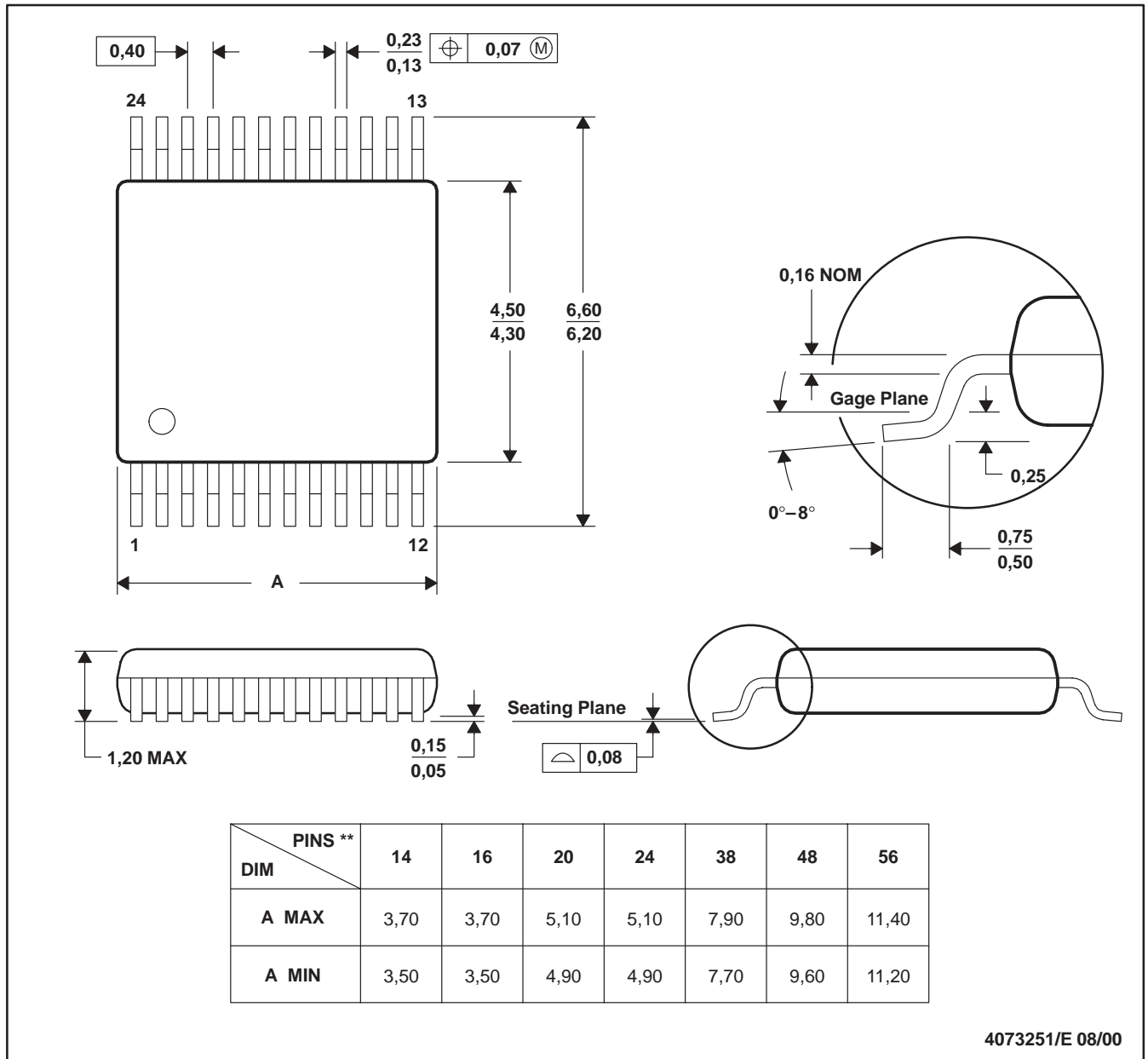


- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2023, Texas Instruments Incorporated