Using the TPS53311EVM-561, a 3-A Eco-mode™ Integrated Switcher With Master-Slave

The TPS53311EVM-561 evaluation module (EVM) is a high-efficiency evaluation platform with two TPS53311 3-A integrated FET step-down converters working in a Master-Slave synchronization scheme. The two outputs are 1.5 V/3 A (master) and 1.2 V/3 A (slave) from a 3.3-V or 5-V input bus. The EVM uses the TPS53311 synchronous buck controller with integrated switcher.

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1 Description

The TPS53311EVM-561 is designed to use a regulated 3.3-V or 5-V bus to produce outputs at up to 3 A of load current. The output is 1.5-V master and 1.2-V slave. The TPS53311EVM-561 is designed to demonstrate the TPS53311 in a typical low-voltage application while providing a number of test points to evaluate the performance of the TPS53311.

1.1 Typical Applications

- Servers and notebook/netbook computers
- Multifunction printers (MFP)
- Embedded PCs, POS terminals
- Switches, routers
- Low-voltage, point-of-load converters
- Any ENERGY STAR/ 80 PLUS™ low-voltage rail

1.2 Features

The TPS53311EVM-561 features:

- 1.5-V master and 1.2-V slave outputs
- 3-Adc, steady-state current
- 1.1-MHz switching frequency
- J1: Selectable 3.3-V or 5-V input voltage
- J2, J7: Selectable FCCM, DE, or HEF mode
- J5: Selectable master and slave interleaved operation
- J4 and J9 for master and slave enable function
- Loop gain measurement
- Convenient test points for probing critical waveforms
- Four-layer PCB with 2-oz copper on the outside layer

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2 Electrical Performance Specifications

Table 1. TPS53311EVM-561 Electrical Performance Specifications[(1)]

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS					
VIN Input Voltage range*	Vin	2.9	3.3/5	6	V
Maximum input current	Vin = 3.3 V,1.5 V/3 A, 1.2 V/3 A, FCCM			2.82	A
No load input current	Vin=3.3 V, 1.5 V/0 A, 1.2 V/0 A, FCCM			40	mA
OUTPUT CHARACTERISTICS					
Master Output voltage Vo_MST		1.485	1.5	1.515	V
Slave Output voltage Vo_SLV		1.188	1.2	1.212	V
Output voltage regulation	Line regulation		0.1%		
	Load regulation		1.0%		
Output voltage ripple	Vin=3.3 V, 1.5 V/0 A-3 A, 1.2 V/0 A-3 A			20	mVpp
Output load current		0		3	A
Output over current			4.5		A
SYSTEMS CHARACTERISTICS					
Switching frequency	Fixed		1.1		MHz
1.5-V full load efficiency	Vin = 3.3 V, 1.5 V/3 A		88.82%		
1.5-V full load efficiency	Vin = 5 V, 1.5 V/3 A		89.50%		
1.2-V full load efficiency	Vin = 3.3 V, 1.2 V/3 A		86.50%		
1.2-V full load efficiency	Vin = 5 V, 1.2 V/3 A		87.32%		
Operating temperature			25		ºC

(1) Jumpers set to default locations; see Section 5 of this user's guide.

3 Schematic

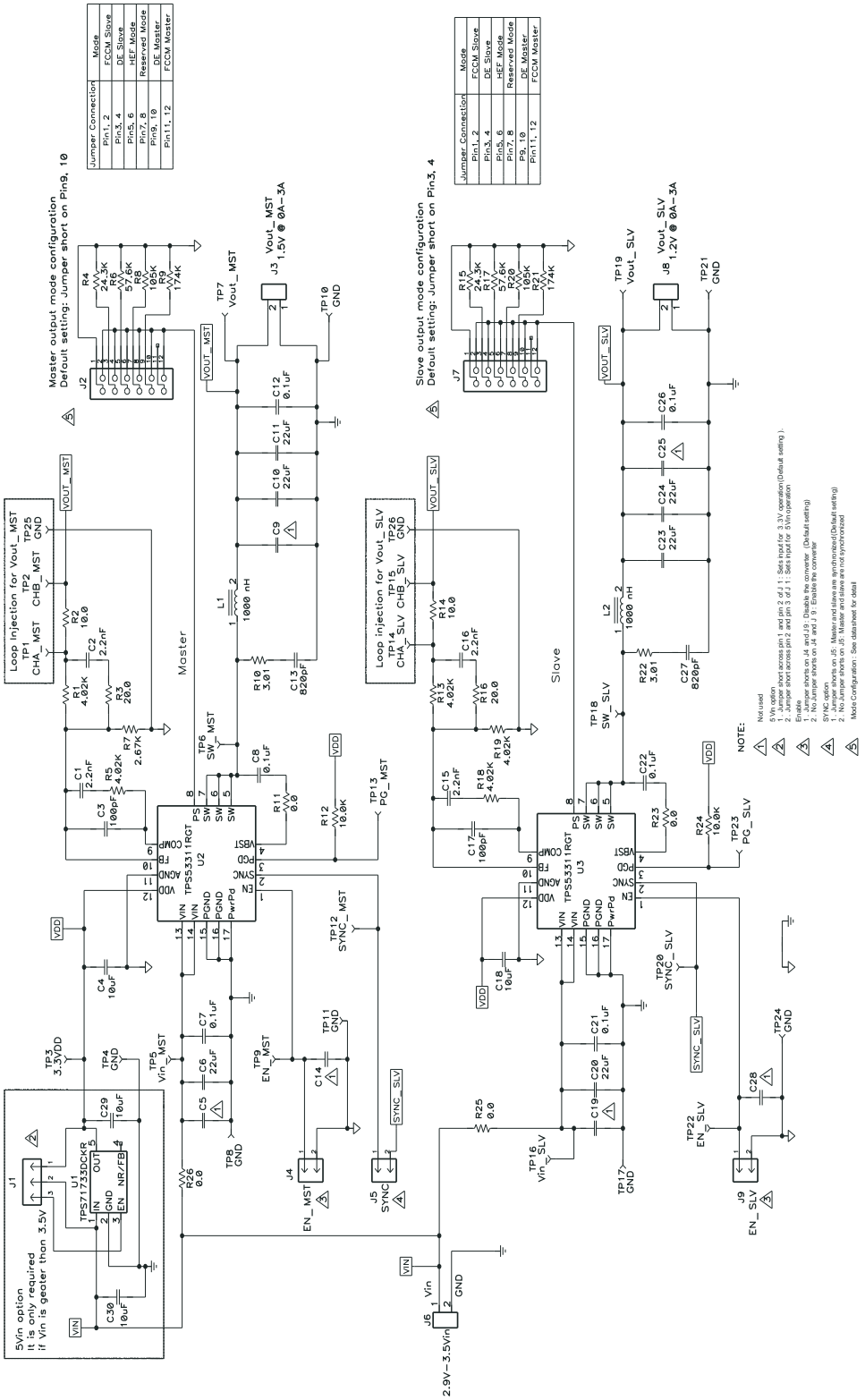


Figure 1. TPS53311EVM-561 Schematic

4 Test Setup

4.1 Test Equipment

Voltage Source VIN: The input voltage source VIN must be a 0-V to 6-V variable dc source capable of supplying 3 Adc. Connect Vin to J6 as shown in Figure 3.

Multimeters: V1: Vin at TP5 (Vin_MST) and TP8 (GND) V2: 1.5 Vout at TP7 (Vout_MST) and TP10 (GND) V3: 1.2 Vout at TP19 (Vout_SLV) and TP21 (GND) A1: Vin input current

Output Load:
Load1: The output load1 must be an electronic constant resistance mode load capable of 0 Adc to 5 Adc at 1.5 V.
Load2: The output load2 must be an electronic constant resistance mode load capable of 0 Adc to 5 Adc at 1.2 V.

Oscilloscope: A digital or analog oscilloscope can be used to measure the output ripple. The oscilloscope must be set for 1-MΩ impedance, 20-MHz bandwidth, ac coupling, 1-µs/division horizontal resolution, 20-mV/division vertical resolution. Test points TP7 and TP10 can be used to measure 1.5-V master output ripple voltage. TP19 and TP21 can be used to measure 1.2-V slave output ripple voltage. Place the oscilloscope probe tip through TP7 (TP19) and hold the ground barrel TP10 (TP21) as shown in Figure 2.

Do not use a leaded ground connection as this may induce additional noise due to the large ground loop.

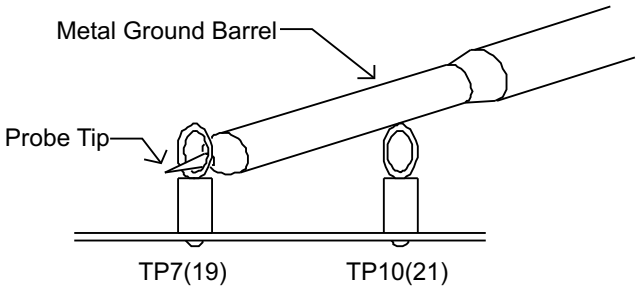


Figure 2. Tip and Barrel Measurement for Vout Ripple

Recommended Wire Gauge:

1. Vin to J6: The recommended wire size is AWG 16 per input connection, with the total length of wire less than 4 feet (2-foot input, 2-foot return).
2. J3 to LOAD1 the minimum recommended wire size is AWG 16, with the total length of wire less than 4 feet (2-foot input, 2-foot return)
3. J8 to LOAD2 the minimum recommended wire size is AWG 16, with the total length of wire less than 4 feet (2-foot input, 2-foot return)

4.2 Recommended Test Setup

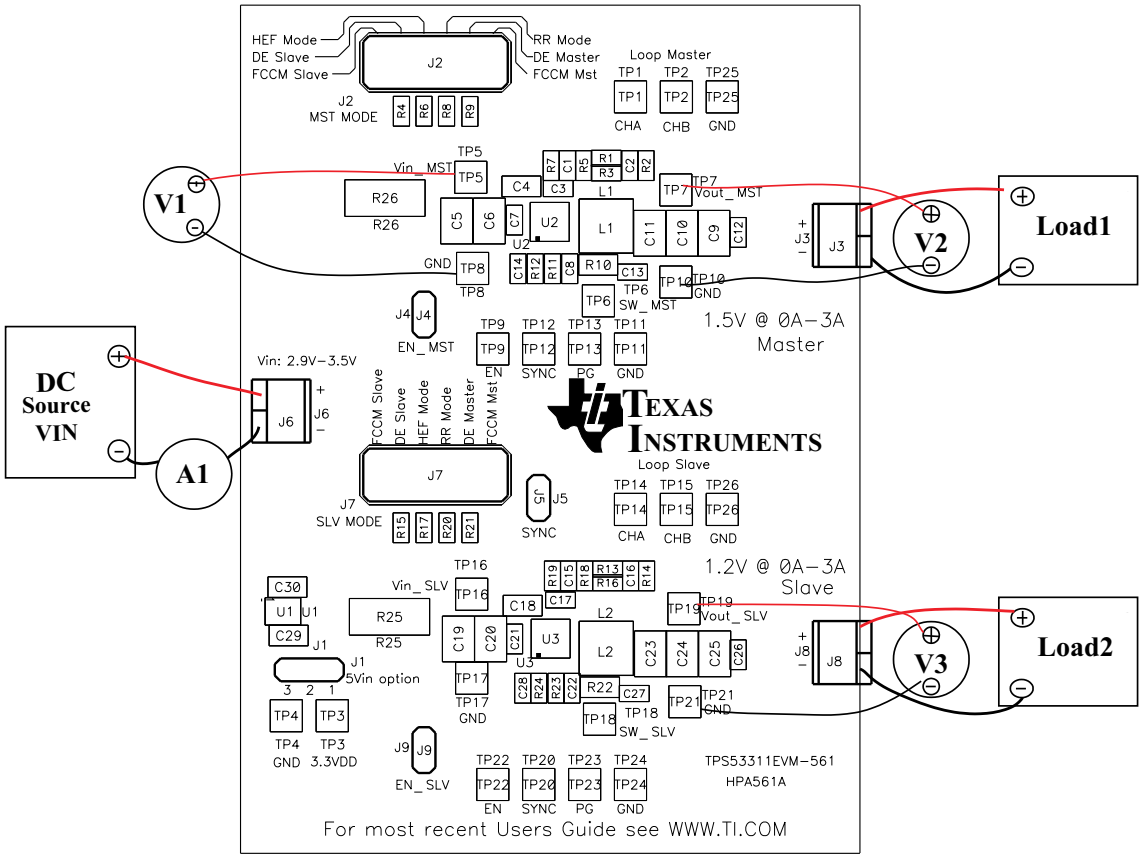


Figure 3. TPS53311EVM-561 Recommended Test Setup

Figure 3 is the recommended test setup to evaluate the TPS53311EVM-561. Working at an ESD workstation, ensure that any wrist straps, bootstraps, or mats are connected referencing the user to earth ground before handling the EVM.

Input Connections:

1. Prior to connecting the dc input source VIN, it is advisable to limit the source current from VIN to 5 A maximum. Ensure that VIN is initially set to 0 V and connected as shown in Figure 3.
2. Connect a voltmeter V1 at TP5 (Vin_MST) and TP8 (GND) to measure input voltage.
3. Connect a current meter A1 between VIN DC source and J6.

Output Connections:

1. Connect Load1 to J3, and set Load to constant resistance mode to sink 0 Adc before Vin is applied.
2. Connect a voltmeter V2 at TP7(Vout_MST) and TP10(GND) to measure the 1.5-V output voltage.
3. Connect Load2 to J8 and set Load to constant resistance mode to sink 0 Adc before Vin is applied.
4. Connect a voltmeter V3 at TP19 (Vout_SLV) and TP21 (GND) to measure the 1.2-V output voltage.

5 Configuration

All jumper selections must be made prior to applying power to the EVM. Users can configure this EVM per the following configurations.

5.1 5-Vin Option (J1: 5-Vin Option)

The 5-V input option can be set by J1.

Default setting: 3.3 Vin.

Table 2. 5-Vin Option

Jumper set to	Input Voltage
1-2 pin shorted	**3.3 Vin**
2-3 pin shorted	5 Vin

5.2 Master Mode Selection (J2: MST Mode)

The Master mode selection can be set by J2.

Default setting: FCCM_Mst

Table 3. Master Mode Selection

Jumper set to	Mode
Left (1-2 pin shorted)	FCCM Slave
Second (3-4 pin shorted)	DE Slave
Third (5-6 pin shorted)	HEF
Fourth (7-8 pin shorted)	Reserved
Fifth (9-10 pin shorted)	DE Master
Right (11-12 pin shorted)	**FCCM Master**

5.3 Slave Mode Selection (J7: SLV Mode)

The Slave mode selection can be set by J7.

Default setting: FCCM_Slave

Table 4. Slave Mode Selection

Jumper set to	Mode
Left (1-2 pin shorted)	**FCCM Slave**
Second(3-4 pin shorted)	DE Slave
Third (5-6 pin shorted)	HEF
Fourth (7-8 pin shorted)	Reserved
Fifth (9-10 pin shorted)	DE Master
Right (11-12 pin shorted)	FCCM Master

5.4 Synchronization (J5: SYNC)

Synchronization for input interleaving can be set by J5.

Default setting: Jumper on J5, Master and Slave 180° Interleaved

Table 5. Synchronization Selection

Jumper set to	Master and Slave Synchronization
Jumper shorts on J5	**Yes**
No jumper on J5	No

5.5 Master Enable (J4: EN_MST)

The Master Enable can be set by J4.

Default setting: Jumper on J4,

Table 6. Master Enable Selection

Jumper set to	Enable/Disable Controller
Jumper shorts on J4	**Disable 1.5-V Master output**
No Jumper on J4	Enable 1.5-V Master output

5.6 Slave Enable (J9: EN_SLV)

The Slave Enable can be set by J9.

Default setting: Jumper on J9,

Table 7. Slave Enable Selection

Jumper set to	Enable/Disable Controller
Jumper shorts on J9	**Disable 1.2-V Master output**
No Jumper on J9	Enable 1.2-V Master output

6 Test Procedure

6.1 Line/Load Regulation and Efficiency Measurement Procedure

1. Ensure that the Load1 and Load2 are set to constant resistance mode and sink 0 A.
2. Ensure that all jumper configuration settings are per Section 5.
3. Ensure that jumpers short on J4, J9 before Vin is applied.
4. Increase Vin from 0 V to 3.3 V, using V1 to measure input voltage.
5. Remove jumper from J4 to enable the master controller.
6. Vary Load1 from 0 A to 3 A; 1.5-V master output must remain in load regulation.
7. Vary Vin from 2.9 V to 3.5 V; 1.5-V master output must remain in line regulation.
8. Remove jumper from J9 to enable the slave controller.
9. Vary Load2 from 0 A to 3 A; 1.2-V slave output must remain in load regulation.
10. Vary Vin from 2.9 V to 3.5 V; 1.2-V slave output must remain in line regulation.
11. Measure the waveforms of SW_MST(TP6) and SW_SLV(TP18) to see master-slave 180° interleaved.
12. Put jumpers on J4 and J9 to disable master and slave controller.
13. Decrease Load1 and Load2 to 0 A.
14. Decrease Vin to 0 V.

6.2 Loop Gain/Phase Measurement

1. Set up EVM as described in Section 6.1 and Figure 3. Measure 1.5-V bode plot.
2. Connect the isolation transformer to CHA_MST and CHB_MST.
3. Connect input signal CHA to TP1 (CHA_MST) and connect output signal CHB to TP2 (CHB_MST).
4. Connect the GND lead of CHA and CHB to TP25 (GND).
5. Inject approximately 50-mV or less signal through the isolate transformer.
6. Sweep the frequency from 500 Hz to 1 MHz with 10-Hz or lower post filter. The control loop gain and phase margin can be measured.
7. Disconnect isolate transformer from the bode plot setup before making other measurements. (Signal injection into feedback may interfere with accuracy of other measurements.)
8. The loop measurement for 1.2-V slave output is the same as with a 1.5-V master output.

6.3 List of Test Points

Table 8. Functions of Each Test Points

Test Points	Name	Description
TP1[(1)]	CHA_MST	Input A for 1.5-V loop injection
TP2	CHB_MST	Input B for 1.5-V loop injection
TP3	3.3VDD	3.3 VDD
TP4	GND	Ground
TP5	Vin_MST	Input voltage for 1.5-V master
TP6	SW_MST	Switching node for 1.5-V master
TP7	Vout_MST	1.5-V output
TP8	GND	Ground
TP9	EN_MST	Enable for 1.5-V master
TP10	GND	Ground
TP11	GND	Ground
TP12	SYNC_MST	SYNC signal for 1.5-V master
TP13	PG_MST	Power Good for 1.5-V master
TP14	CHA_SLV	Input A for 1.2-V loop injection
TP15	CHB_SLV	Input B for 1.2-V loop injection
TP16	Vin_SLV	Input voltage for 1.2-V slave
TP17	GND	Ground
TP18	SW_SLV	Switching node for 1.2-V slave
TP19	Vout_SLV	1.2-V output
TP20	SYNC_SLV	SYNC signal for 1.2-V slave
TP21	GND	Ground
TP22	EN_SLV	Enable for 1.2-V slave
TP23	PG_SLV	Power Good for 1.2-V slave
TP24	GND	Ground
TP25	GND	Ground
TP26	GND	Ground

(1) For test point locations, see Figure 3

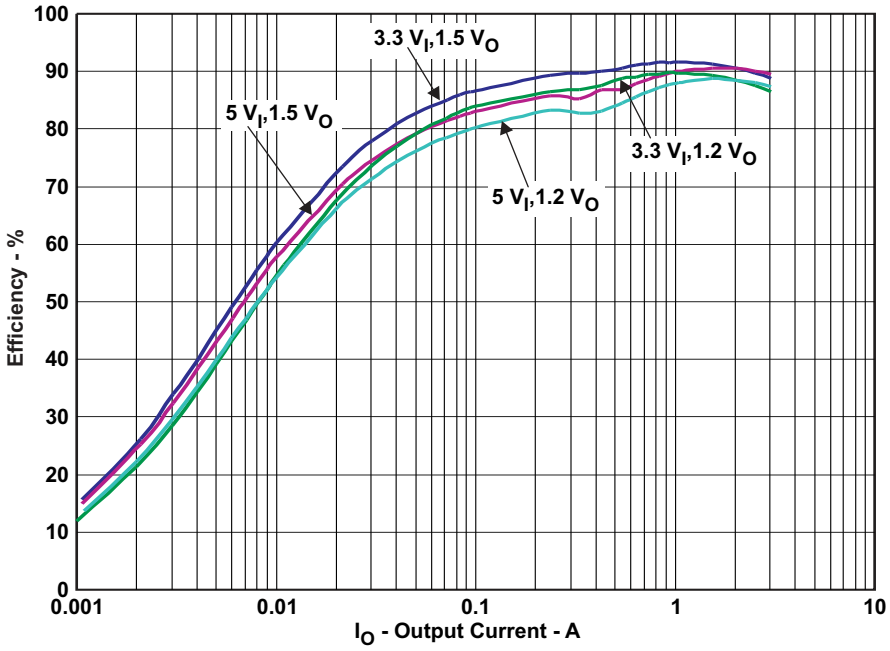
6.4 Equipment Shutdown

1. Shut down Load.
2. Shut down Vin.
3. Shut down Oscilloscope.

7 Performance Data and Typical Characteristic Curves

Figure 4 through Figure 16 present typical performance curves for TPS53311EVM-561. Jumpers set to default locations; see section 5 of this user's guide.

7.1 Efficiency



NOTE: R-C snubber to reduce switching node ringing has effect on dc-dc converter efficiency.

Figure 4. TPS53311EVM-561 Efficiency

7.2 Load Regulation

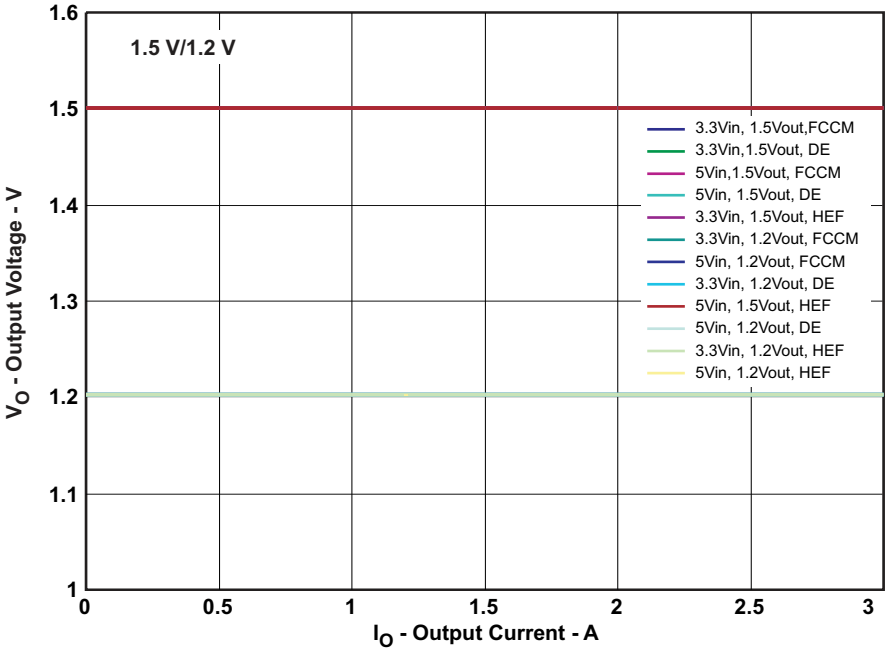


Figure 5. TPS53311EVM-561 Load Regulation

7.3 Line Regulation

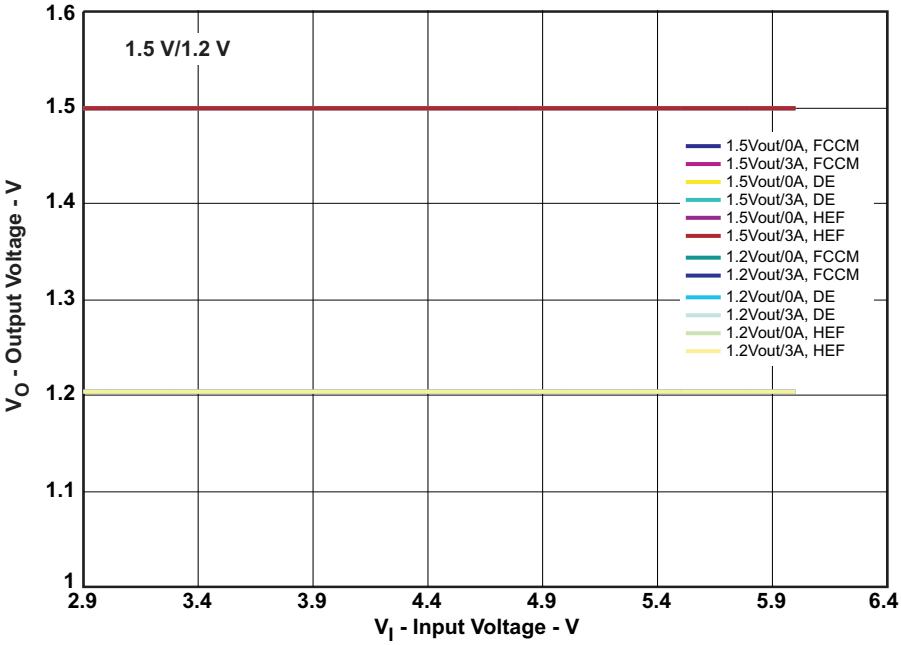


Figure 6. TPS53311EVM-561 Line Regulation

7.4 1.5-V Output Ripple

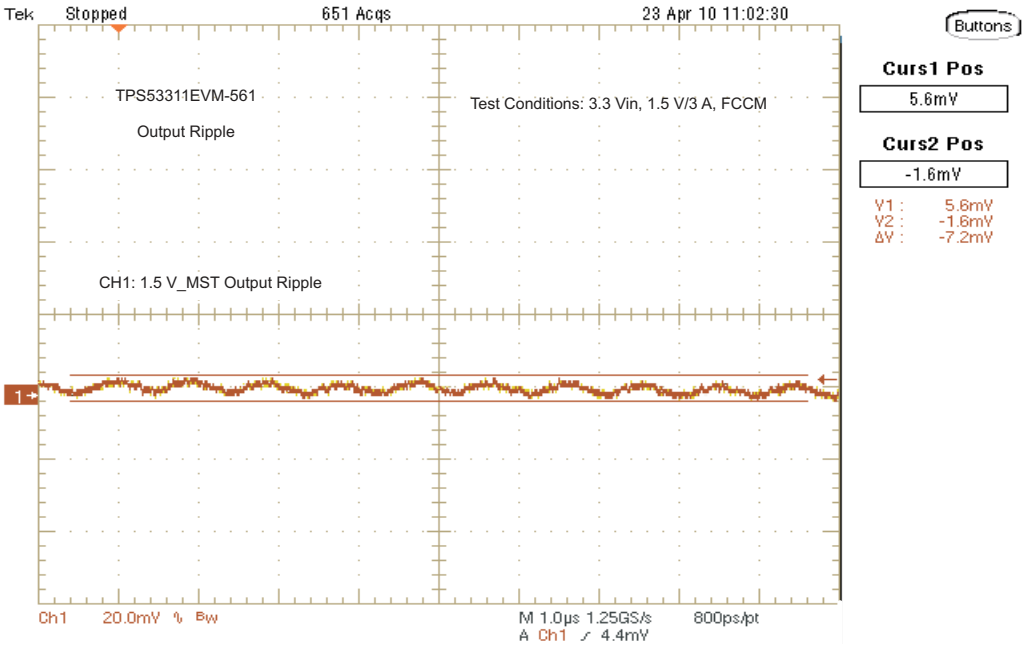


Figure 7. TPS53311EVM-561 Output Ripple,3.3 Vin, 1.5 V/3 A

7.5 1.5-V Switching Node at Full Load

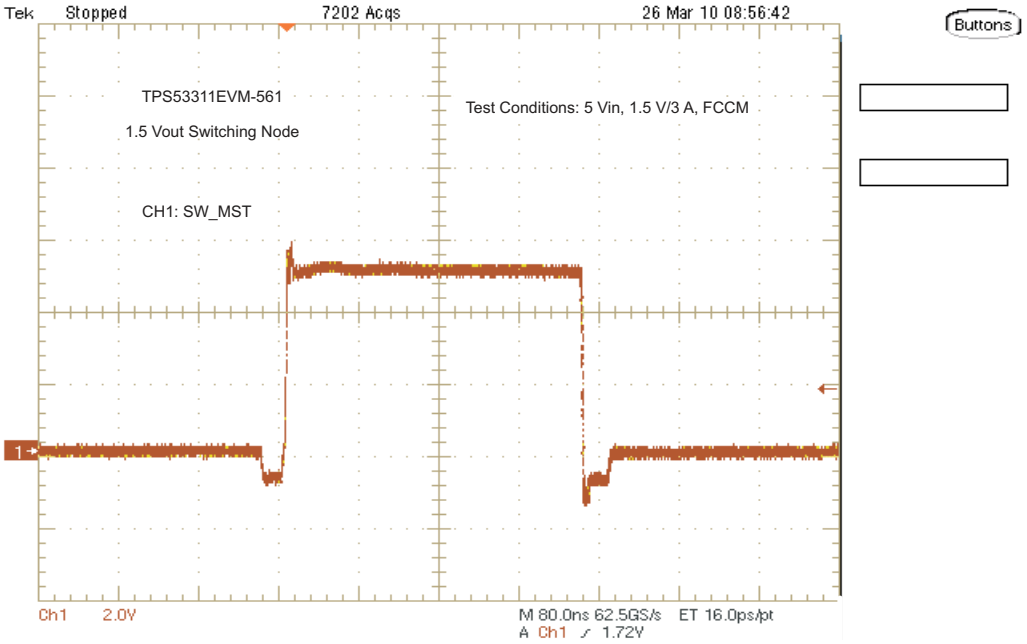


Figure 8. TPS53311EVM-561 Switching Node at Full Load, 5 Vin, 1.5 V/3 A

7.6 1.5-V Switching Node at No Load

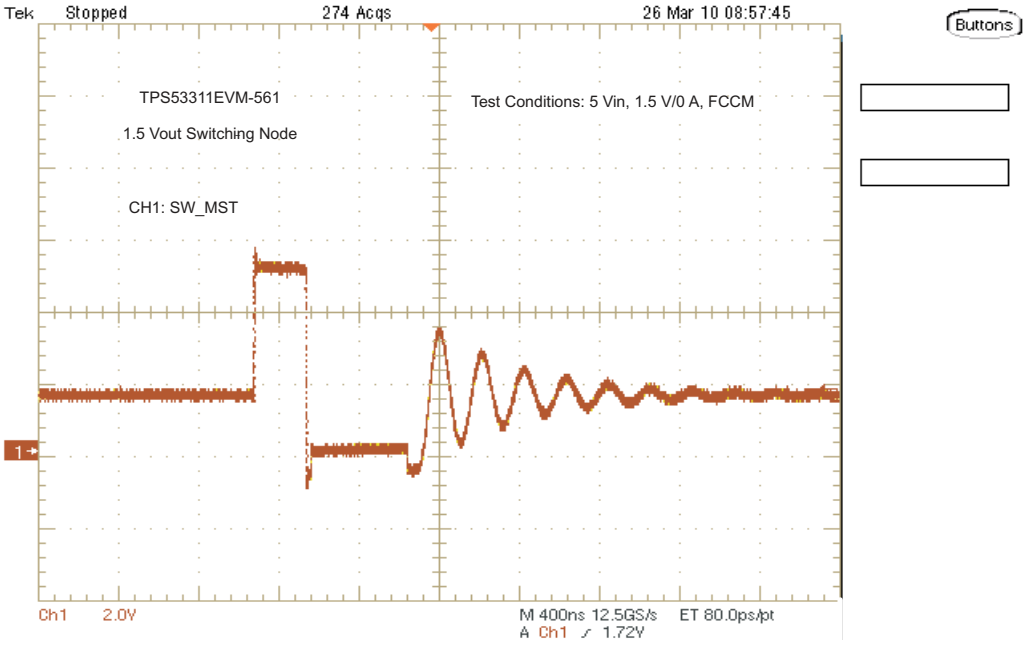


Figure 9. TPS53311EVM-561 Switching Node at No Load, 5 Vin, 1.5 V/0 A DE Mode

7.7 Master-Slave 180° Synchronization

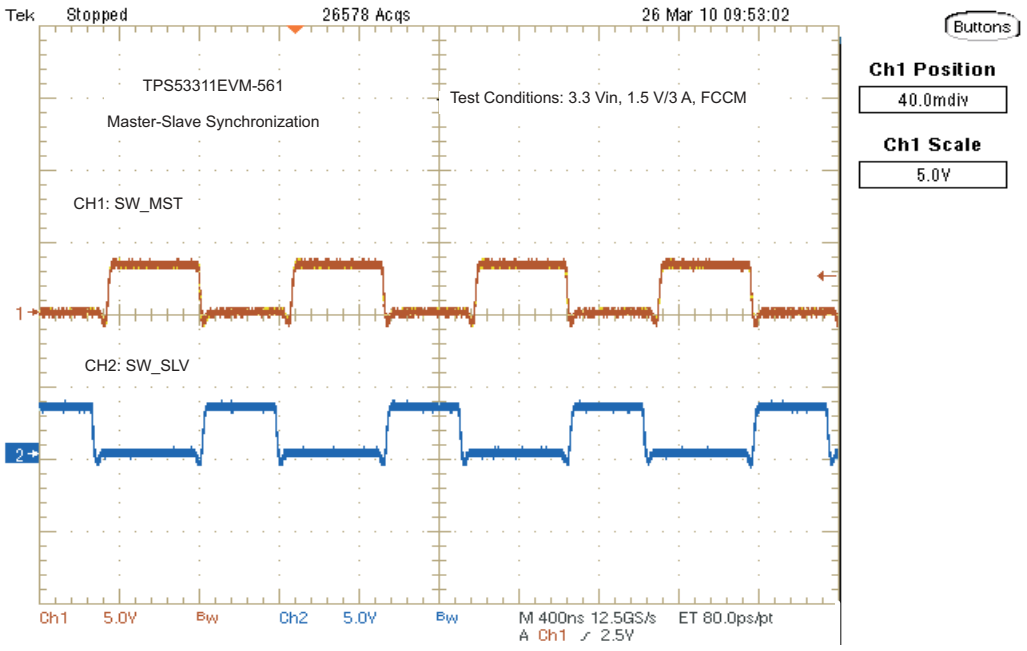


Figure 10. TPS53311EVM-561 Synchronization
3.3 Vin, 1.5 V/3 A, 1.2 V/3 A 180° Synchronization

7.8 1.5-V Master Turnoff During Master-Slave Synchronization

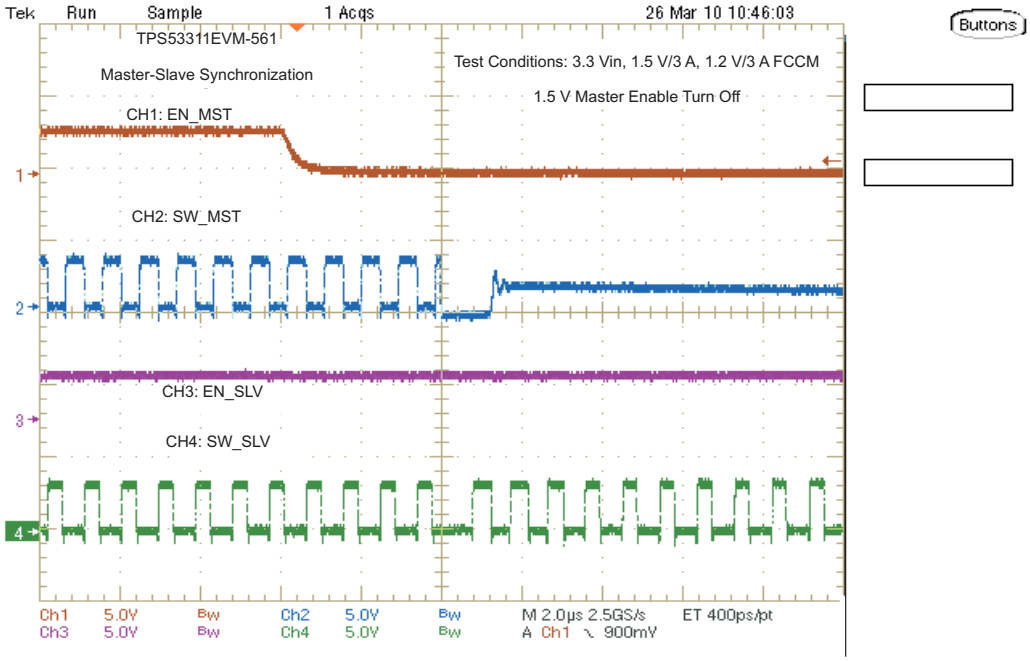


Figure 11. TPS53311EVM-561 Synchronization
(3.3 Vin, 1.5 V/3 A, 1.2 V/3 A 180° Synchronization, Then Turn Off Master)

7.9 1.5-V Output Transient

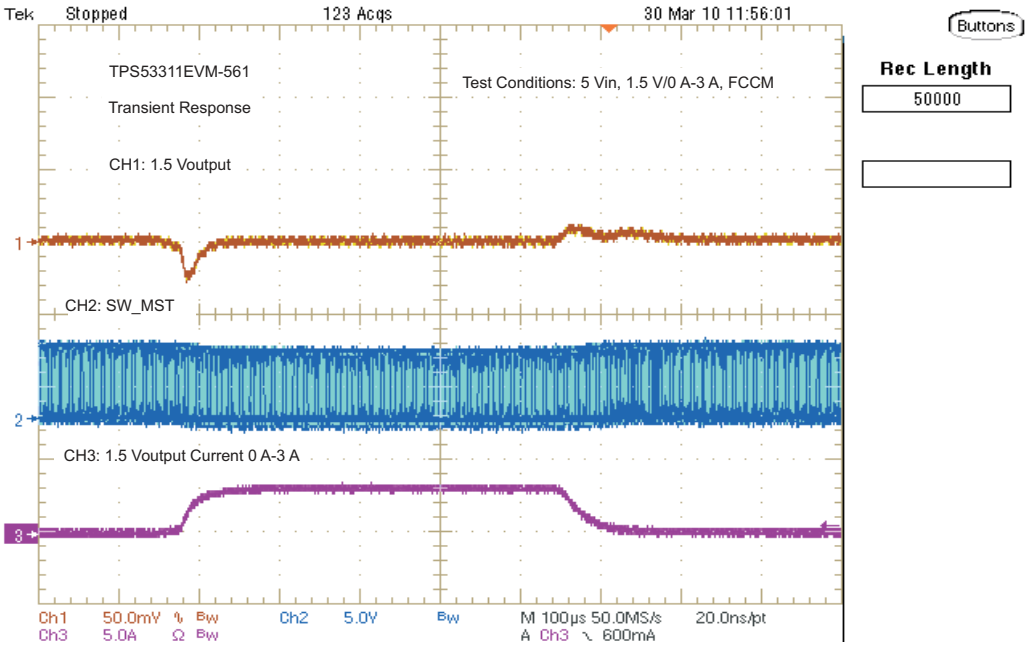


Figure 12. TPS53311EVM-561, 1.5-V Output Transient, 5 Vin, 1.5/0 A to 3 A

7.10 1.5-V Turnon Waveform

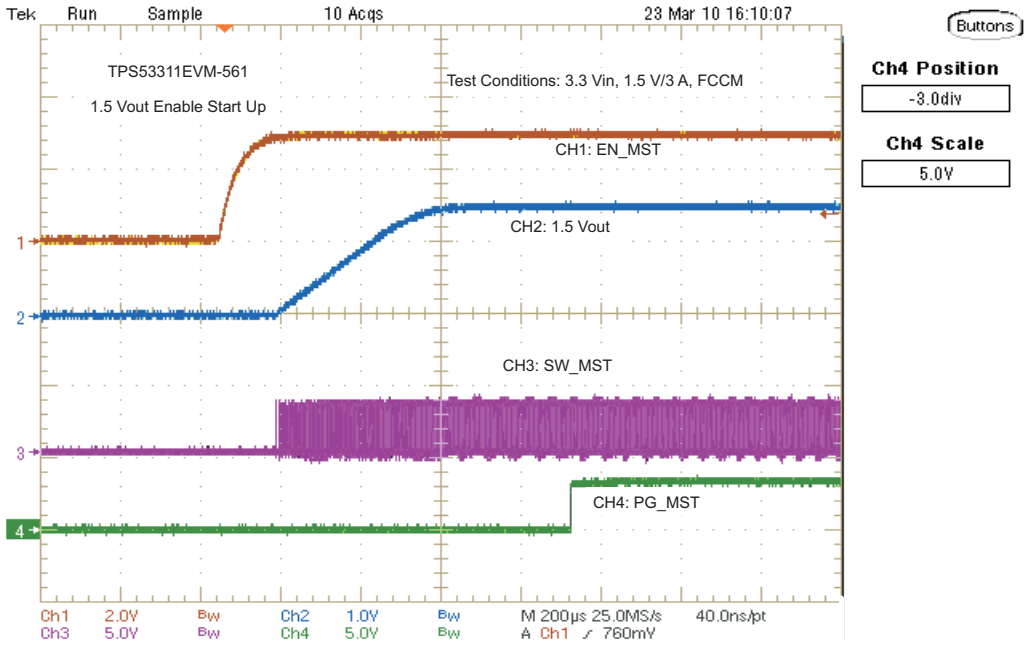


Figure 13. TPS53311EVM-561 Enable Turns On Waveform, 3.3 Vin, 1.5 V/3 A

7.11 1.5-V Turnoff Waveform

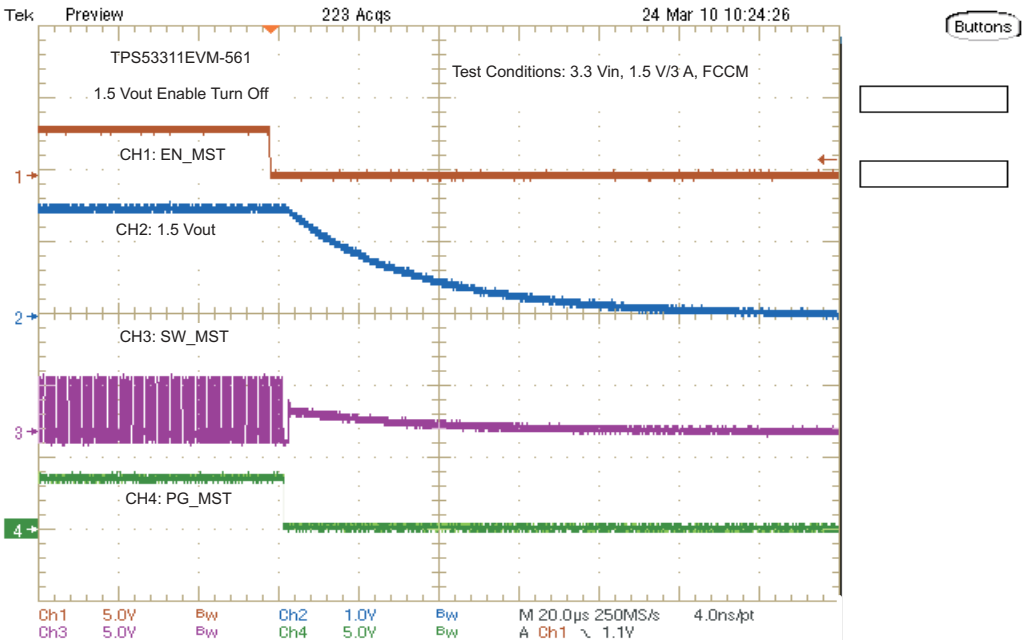


Figure 14. TPS53311EVM-561 Enable Turns Off Waveform, 3.3 Vin, 1.5 V/3 A

7.12 1.5-V Bode Plot

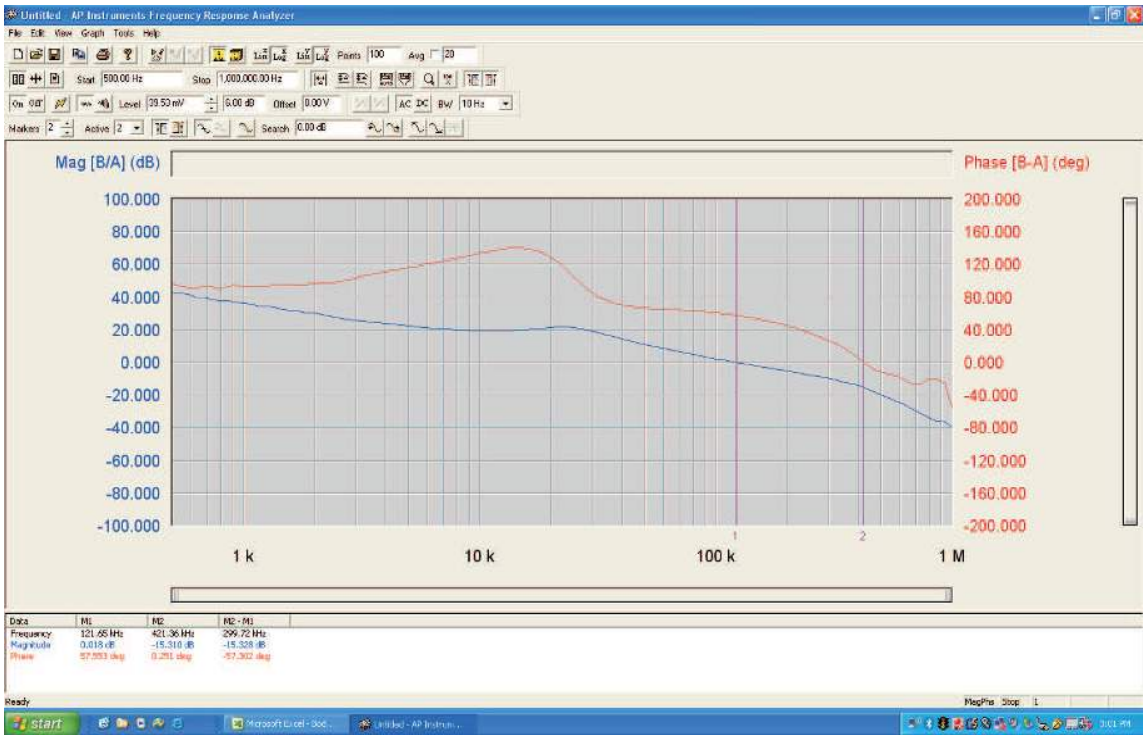


Figure 15. TPS53311EVM-561 Bode Plot, 3.3 Vin, 1.5 V/3 A

7.13 EVM Top Board Thermal Image

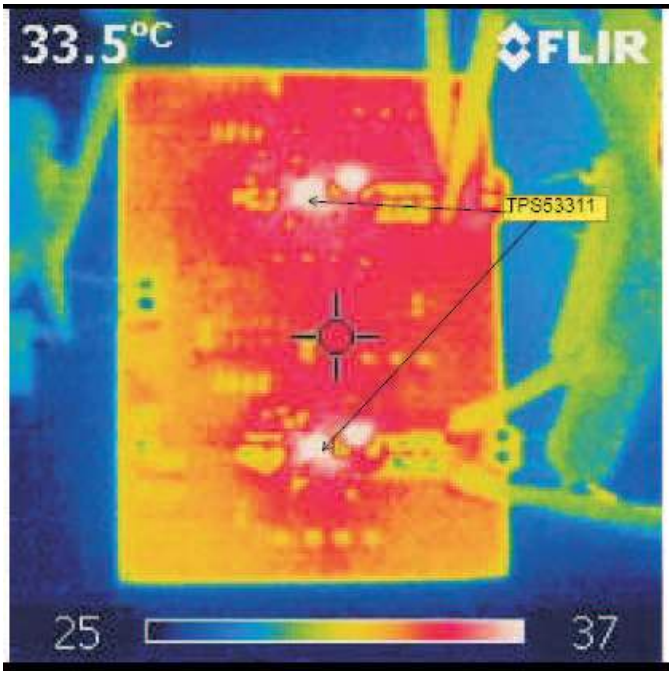


Figure 16. TPS53311EVM-561 Top Side Thermal Image, 3.3 Vin, 1.5 V/3 A, 1.2 V/3 A

8 EVM Assembly Drawings and PCB Layout

Figure 17 through Figure 22) shows the design of the TPS53311EVM-561 printed-circuit board. The EVM has been designed using a 4-layer circuit board with 2-oz copper on outside layers.

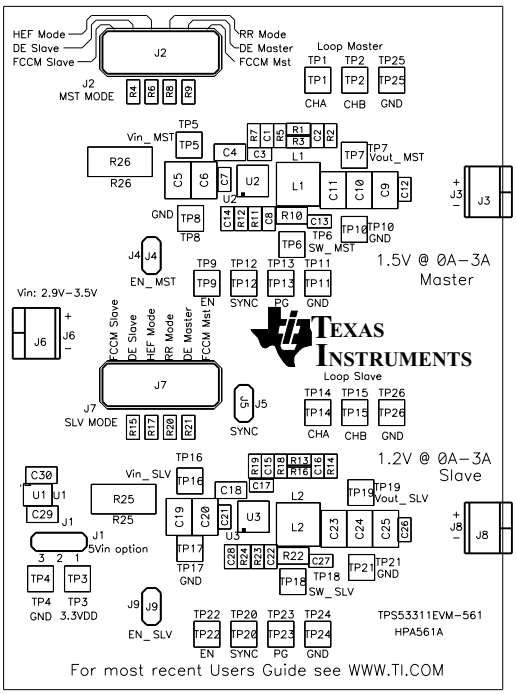


Figure 17. TPS53311EVM-561 Top Layer Assembly Drawing, Top view

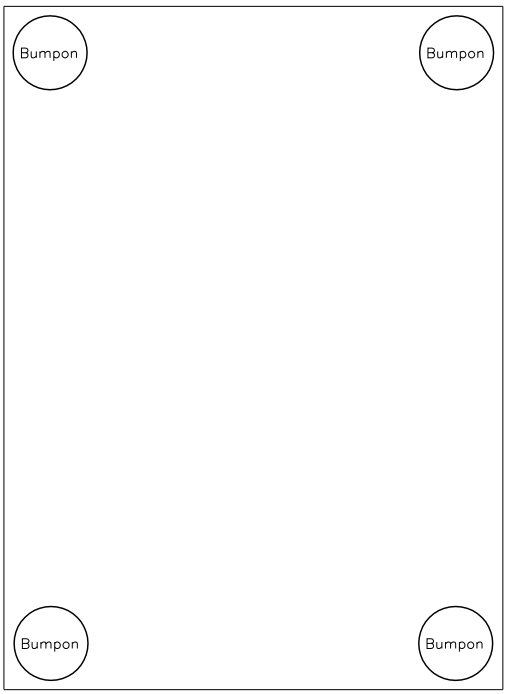


Figure 18. TPS53311EVM-561 Bottom Assembly Drawing, Bottom View

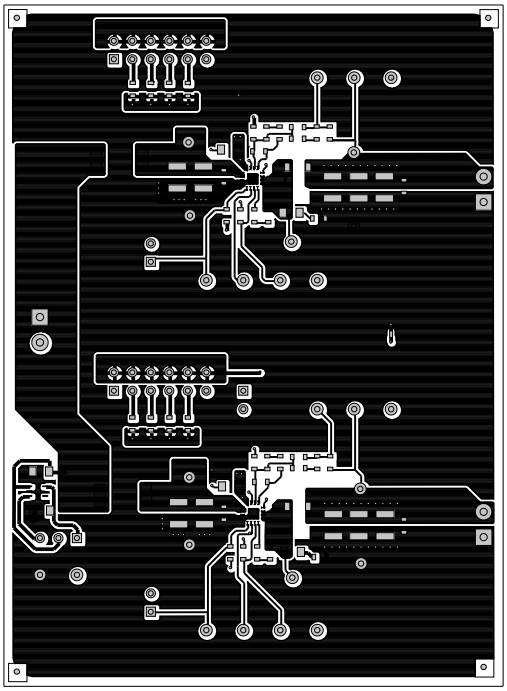


Figure 19. TPS53311EVM-561 Top Copper, Top View

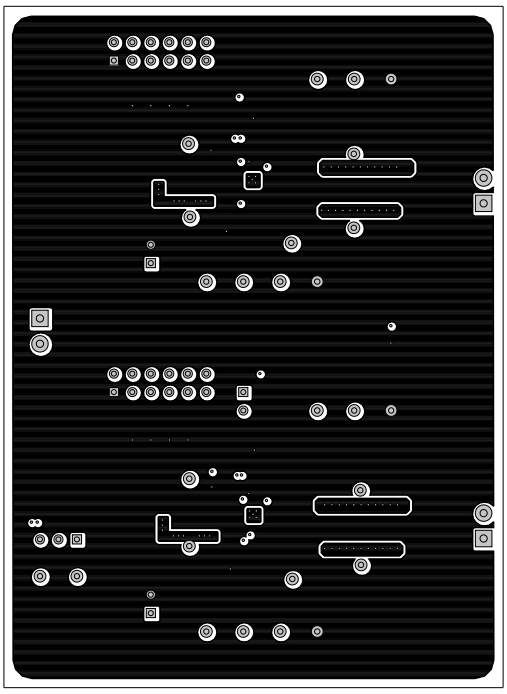


Figure 20. TPS53311EVM-561 Internal Layer 2, Top View

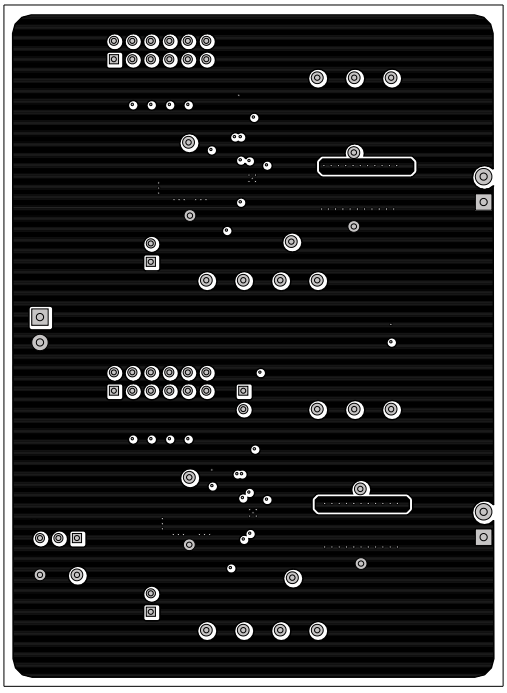


Figure 21. TPS53311EVM-561 Internal Layer 3, Top View

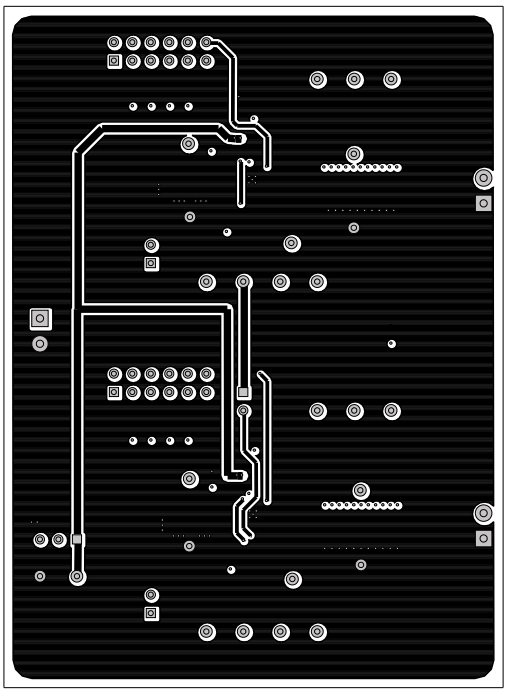


Figure 22. TPS53311EVM-561 Bottom Copper, Top View

9 Bill of Materials

The EVM major components list according to the schematic shown in Figure 1 is listed in Table 9.

Table 9. Bill of Materials

QTY	RefDes	Description	MFR	Part Number
4	C1, C2, C15, C16	Capacitor, Ceramic, 2.2nF, 50V, X7R, 10%, 0603	STD	STD
2	C13, C27	Capacitor, Ceramic, 820pF, 50V, X7R, 10%, 0603	STD	STD
6	C6, C10, C11, C20, C23, C24	Capacitor, Ceramic, 22uF, 16V, X5R, 10%, 1210	STD	STD
2	C3, C17	Capacitor, Ceramic, 100pF, 50V, C0G, 10%, 0603	STD	STD
4	C4, C18, C29, C30	Capacitor, Ceramic, 10uF, 10V, X5R, 10%, 0805	STD	STD
6	C7, C8, C12, C21, C22, C26	Capacitor, Ceramic, 0.1uF, 25V, X7R, 10%, 0603	STD	STD
2	L1, L2	Inductor, SMT, 1uH, 5.6A, 5.4mohm, 5.0x5.0mm	ICE components	IN06142
5	R1, R5, R13, R18, R19	Resistor, Chip, 4.02k, 1/16W, 1%, 0603	STD	STD
2	R10, R22	Resistor, Chip, 3.01, 1/10W, 5%, 0805	STD	STD
2	R11, R23	Resistor, Chip, 0, 1/16W, 5%, 0603	STD	STD
2	R12, R24	Resistor, Chip, 10.0k, 1/16W, 1%, 0603	STD	STD
2	R2, R14	Resistor, Chip, 10, 1/16W, 1%, 0603	STD	STD
2	R25, R26	Resistor, Chip, 0, 1W, 5%, 2512	STD	STD
2	R3, R16	Resistor, Chip, 20, 1/16W, 1%, 0603	STD	STD
2	R4, R15	Resistor, Chip, 24.3k, 1/16W, 1%,0603	STD	STD
2	R6, R17	Resistor, Chip, 57.6k, 1/16W, 1%,0603	STD	STD
1	R7	Resistor, Chip, 2.67k, 1/16W, 1%,0603	STD	STD
2	R8, R20	Resistor, Chip, 105k, 1/16W, 1%, 0603	STD	STD
2	R9, R21	Resistor, Chip, 174k, 1/16W, 1%, 0603	STD	STD
1	U1	IC, 150mA, Low Iq, Wide bandwidth, LDO Linear regulator, SC70	TI	TPS71733DCKR
1	U2, U3	IC, 3A Step-down regulator with integrated switcher, QFN-16	TI	TPS53311RGT

Evaluation Board/Kit Important Notice

Texas Instruments (TI) provides the enclosed product(s) under the following conditions:

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EVM Warnings and Restrictions

It is important to operate this EVM within the input voltage range of 2.9 V to 6 V and the output voltage range of 0.6 V to 0.84 V .

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 40° C. The EVM is designed to operate properly with certain components above 40° C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

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